**UNIT III**

**BIPOLAR JUNCTION TRANSISTOR (BJT) CIRCUITS**

**Topics:** BJT structure and its operation with normal biasing, Transistor characteristics and parameters, DC operating point, Transistor as an amplifier, Transistor as a switch, Enhancement type MOSFET.

**Objectives:** The objective of this unit is to study various types of transistors, their configurations and applications.

**Outcomes:** At the end of this unit, the learner will be able to:

1. Understand the operation of a transistor.

2.  Understand the transistor configurations and their comparison.

3.  State applications of transistor.

4.  Compare BJT and MOSFET.

**Pre-requisites**:Learner should be familiar with the basics of diode and diode circuits before transistorcircuits  
**Introduction:**

**Advantages of Transistors:**

•  Small in size, light weighted.

•  Operate at low voltages.

•  Higher efficiency.

•  Do not require any filament power.

•  Long life.

The  term  transistor  was  derived  from  the  words  “Transfer”  and  “Resistor”.  These two words describe the operation of transistor, which is the transfer of an input signal current from a low resistance circuit to a high resistance circuit. Transistor is a three terminal device. These terminals are Collector, Emitter and Base. The base terminal is called a control terminal. It is called a bipolar transistor because in Bipolar Junction Transistor the conduction takes place due to both the charge carriers i.e. electrons and holes. If the conduction is due to only one type of charge carriers i.e. majority charge carriers, then the transistor is called as “Unipolar” transistor.

**1.1. Types of Transistor and Construction:**   
There are two types of transistors.

|  |  |
| --- | --- |
|  |  |

**1.1.1.  P-N-P Transistors.** PNP transistor is constructed by sandwiching a thin N type semiconductor between two P type semiconductors. The construction and symbol of PNP transistor is shown in fig. 1.1.1(a) and fig. 1.1.1(b) respectively. As shown in symbol of PNP transistor of fig. 1.1.1(b), the emitter current flows into the emitter terminal. The majority  charge  carriers  in  PNP  are holes and minority charge carriers are electrons.

|  |  |
| --- | --- |
| Fig. 1.1.1(a) Construction of PNP Transistor | Fig. 1.1.1(b) symbol of PNP transistor   . |

**1.1.2.  N-P-N Transistors**. NPN transistor is constructed by sandwiching a thin P type semiconductor between two N type semiconductors.  The construction and symbol of NPN transistor is shown in fig. 1.1.2(a) and fig. 1.1.2 (b) respectively. As shown in symbol of NPN transistor of fig. 1.1.2(b),    the emitter current flows out of the emitter terminal.

|  |  |
| --- | --- |
| Fig. 1.1.2(a) Construction of NPN Transistor | Fig. 1.1.2(b) Symbol of NPN transistor |

The majority charge carriers in NPN are electrons and minority charge carriers are holes.

**1.1.3. Common important points about transistor construction:**

•  Base is always thin and lightly doped layer.

•  Collector and Emitter layers are much wider than the base and are heavily doped as compared to base.

•  The Emitter is the most heavily doped layer because it has to emit electrons. Collector has wider space compared to emitter because it is needed to dissipate more heat. •  The  arrow  is  always  placed  on  the  emitter  terminal  and  arrow  direction  indicates  the  direction  of conventional current flow of emitter current. NPN transistors are more popular than the PNP transistors. So we will consider NPN transistor in most of the explanation rather than PNP transistor.

•  As seen from the constructional diagram of transistors, we can see that transistor has two PN junctions, namely Base to Emitter Junction (JBE) or Emitter junction and Collector to Base junction (JCB) or Collector junction.

* PNP and NPN transistors are equivalent to two diodes connected back to back as shown in fig 1.1.3(a) and 1.1.3(b) respectively.

|  |  |
| --- | --- |
| Fig 1.1.3(b): Equivalent for PNP Transistor | Fig 1.1.3(b): Equivalent for NPN Transistor |

2. **Transistor Biasing:**

**2.1. Unbiased Transistor:**

A transistor is said to be unbiased when no external power supply is connected to it. Due to two PN junctions in transistor, depletion regions are formed at the JBE and JCB. The depletion region is not same on the two sides of the junctions as shown in fig. 2.1 for NPN transistor. Depletion region always penetrates more in lightly doped region i.e. base and less penetrates in heavily doped region i.e. collector and emitter.

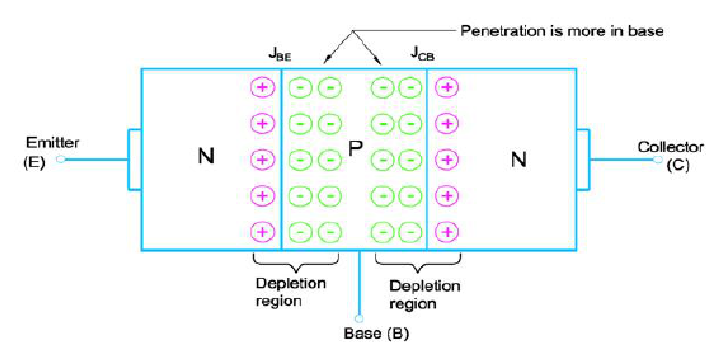


Fig.2.1 Depletion region in an unbiased NPN transistor

**2.2. Biased Transistor:** A transistor is said to be biased when external power supply is connected to it. BJT is capable of operating in three different regions, depending on the biasing. The biasing condition for these three regions of operations is listed in the table 2.1

Table 2.1 Biasing conditions for different regions of operation

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Sr.No | Region of Operation | Base Emitter Junction | Collector Base Junction | Application |
| 1 | Saturation region | Forward Biased | Forward Biased | As a Closed Switch |
| 2 | Cutoff region | Reverse Biased | Reverse Biased | As an Open Switch |
| 3 | Active region | Forward Biased | Reverse Biased | As an Amplifier |

Let us understand as how to bias the transistor in active region. As mentioned in the above table, in order to use transistor as an amplifier it must be operated in active region.

Fig.2.2 shows the biasing for the NPN transistors in the active region. External power supply is connected in such a way that JBE is made forward biased and JCB is  reverse  biased.  Figure also indicates the conventional flow  of currents IB,,IC and IE. From figure, we see that external supply VCC is made larger  than  supply VEE,  to  ensure  that collector to base junction is reverse biased. Note that the polarities for the  PNP  transistor  are  exactly  opposite  to  the  polarity  of  NPN transistor.

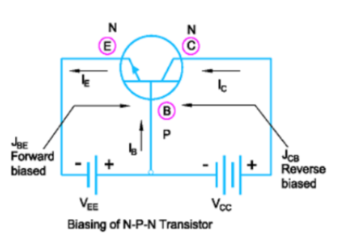


Fig.2.2 NPN transistor biasing in the active region

**3.  Transistor Operation:**

**3.1. Operation of NPN Transistor:**

We will study operation of NPN transistor in the active region. In order to operate transistor in active region, base emitter junction JBE is made forward biased and collector base junction JCB is reverse biased. The external supply is given as shown  in fig.3.1 to  make the transistor to  operate in active region. Due  to this biasing, depletion region for base emitter junction is narrow and is wider for collector base junction

As  the  base  emitter  junction JBE is forward  biased,  it  reduces  the barrier  potential  and  causes  the majority  charge  carriers  i.e. electrons  to  flow  from  n  type emitter to p-type base region. This constitutes the emitter current IE. Few of  the  electrons  entering  into the  base  region  do  not  reach  the collector  region  because recombination  of  electrons  and holes takes place and they flow out of the base terminal as shown in fig. 3.1. As the base region is very thin and lightly doped, very few holes are available for recombination. Due to this only about 2% electrons will flow out of the base. This

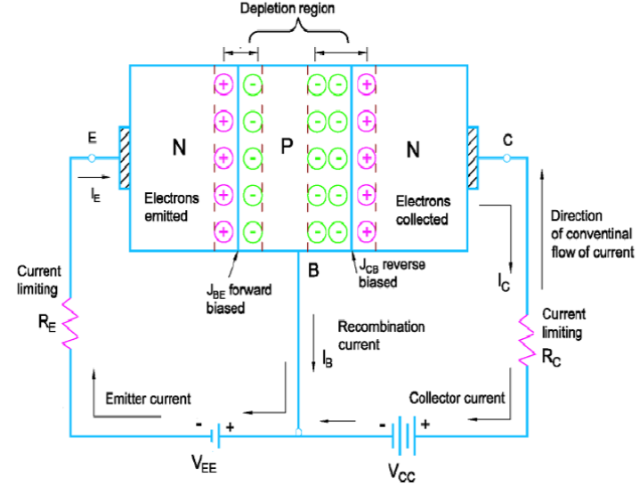


 Fig.3.1.Operation of NPN Transistor constitutes the base current IB.

IB is said to be just 2% of IE. The remaining 98% electrons cross the reverse biased collector junction and reach to the positive terminal of the external supply VCC. This constitutes the collector current IC. The collector current is much larger than the base current. The emitter current is thus the sum of collector current and base current. i.e.IE=IC+IB. IBis very small compared to IC so we can assume that the collector current is nearly equal to the emitter current. i.e. IC≈IE

**3.2. Operation of PNP Transistor:**

PNP  transistor  behaves  exactly  in  the same way as  the NPN  transistor, only difference  is,  the  majority  charge carriers  are  holes  and  minority  charge carriers are electrons. Here, in PNP as shown in fig. 3.2 holes are emitted from the p-type emitter region into the n-type base region.  Base region is thin and lightly doped and so very few electrons are  available  for  recombination. Therefore  about  2%  of  total  emitted holes will flow out of the base terminal and  remaining  98%  are  collected  by collector region.

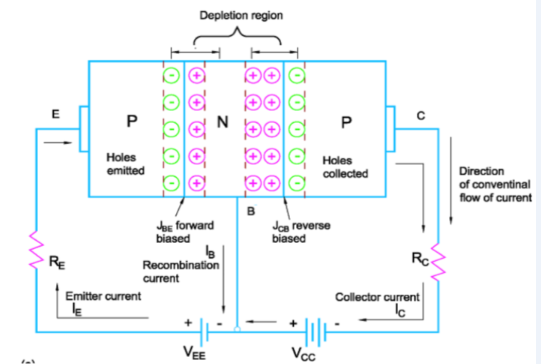


Fig. 3.2.Operation of PNP Transistor

**4.  Transistor Configurations:** In transistor, depending on which terminal is made common between input and output port, there are three possible configurations of the transistor. They are: Common Base (CB) Configuration, Common Emitter (CE) Configuration, and Common Collector (CC) Configuration. We will study these considering the active region of operation of Transistor and considering NPN transistor only , because it is the most popular transistor in the market .Let us start with the CB configuration .

**4.1. Common Base Configuration (CB):** In  common  base  configuration,  base  terminal  is  made  common between  input  port  and  output  port.  The input is applied between emitter  and  base.  So the input voltage  is VBE and  input  current is IE. Output is taken between collector and base. So the output voltage is VCB and output current is IC.

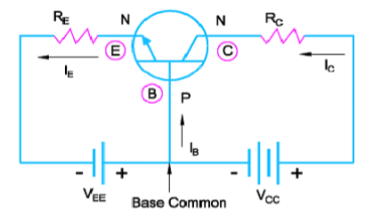


Fig 4.1.1 Common Base Configuration for NPN transistor Components in Collector Current : •  IC(INJ) and ICBO

The collector current IC in common base configuration is given by,

IC= IC(INJ) + ICBO  (4.1.1)

Where, IC(INJ)  is called as injected collector current and is due to the number of electrons crossing the collector base  junction  and ICBO is  reverse  saturation  current flowing  through the  transistor  due  to  minority  carriers between collector and base when the emitter terminal is kept open.

This current flows due to reverse biased collector base junction.

ICBO is negligible as compared to IC(INJ)  and so we can neglect it.

IC= IC(INJ)  ………Practically                 (4.1.2)

IC=ICBO……….. When emitter terminal is kept open           (4.1.3)

These current IC(INJ)and ICBO are indicated in fig. 4.1.2(a) and fig. 4.1.2(b) respectively.

|  |  |
| --- | --- |
| Fig 4.1.2(a) Operation of Normal transistor for IC(INJ) | Fig 4.1.2(b) With Emitter terminal open |

•  **Current amplification factor or current gain(αdc)**:

Current gain is the ratio of output current to  the input current. As seen  just now, we have IC(INJ) is output current and IE is the input current.

So,                       (4.1.4)

As value of IC(INJ) is less than IE, value of will be always less than 1.Depending on the base thickness value of   ranges from 0.95 to 0.995. If thickness of base is large, recombination at base will be more and so smaller is IC and hence smaller the value of . From, equation (4.1.4),

we can write, x IE (4.1.5)

Equation number 4.1.1 reduces to,

                                             (4.1.6)

Neglecting ICBO above equation reduces to,                      (4.1.7)

Current gain =                      (4.1.8)

•  Expression for IB: We have,

Substituting the value of IC, we get,

  +IB

So,

Neglecting ICBO,

we get, (4.1.9)

**4.1.1. Characteristics of Transistor:**

The characteristics of transistor help us to understand its behaviour. Input characteristics is basically a plot of input current verses input voltage and output characteristics is a plot of output current verses output voltage.

**Input and output characteristics of CB configuration:**

|  |  |
| --- | --- |
| **Input characteristics** | **Output characteristics:** |
| Input characteristics of CB configuration is a plot of input  current  IE verses  input  voltage VBE,  keeping output  voltage VCB constant. VBEis  plotted  on  the  X-axis and emitter current IE is plotted on the Y-axis as shown in fig. 4.1.1.1.    Fig 4.1.1.1Input Characteristics  • The input characteristics is similar to the forward V-I characteristics of diode.  • Up to cut in voltage, the emitter current is negligible but  after  cut  in  voltage  it  increases  rapidly  with  a very small increase in the input voltage VBE.  • and  • Change in emitter current is very large compared to  a  small  change  in  input  voltage ) so  the input resistance (ri) is small.  **Early Effect or Base width modulation:**  we  can  observe  that,  the  emitter  current IEincrease slightly with increase in the output voltage VCB. When VCB i.e.  reverse  bias  voltage  increase,  width  of depletion  region  increases  which  in  turn  reduces  the electrical base width. This effect is called Early effect and as the width of base is changing it is called base width modulation | An output characteristic of CB configuration is a plot of  output  current  IC verses  output  voltage VCB, keeping  input  current IE constant. VCBis plotted  on the X-axis and collector current IC is plotted on the Y-axis as shown in fig. 4.1.1.3.  Fig 4.1.1.3 Output Characteristics    **Cutoff region**: Here JBE and JCB , both the  junctions are in reverse biased. The region below the curve for IE=0is called cutoff region. This is  because when input current IE is zero, the  transistor will remain  in off  state  and  is  nothing  but  emitter  terminal  open. ICBO is very small.  **Saturation region:**  Here  JBE and  JCB,  both  the  junctions are in forward biased therefore the saturation region corresponds to negative values of VCBas shown in  fig.  4.1.1.3.  This  is  because,  in  CB  configuration base  is  a  common  terminal  and  so  voltages  are measured  with  respect  to  this  common  point (reference point or ground point). In order to forward bias collector to base junction, collector terminal must be  at  .7V.  Hence  saturation  region  corresponds  to negative values of VCB.  Output  current  IC in  this  region  increases exponentially with increase in VCB . The slope of the output  characteristics  in  this  region  is  large.  i.e.  Ro=  So  the  output  dynamic resistance (ro)has  a  small  value.  This    indicates  that the voltage drop across the transistor VCE is mall in this region.  **Active region:** Here ,output current (IC) is almost equal to the input current (IE) i.e. IC=IE irrespective of the variation in output voltage VCB .This is the reason that transistor is called a “Current controlled “ore “Current operated device and can be used as an “Constant Current Source “application in this region of operation. |

**4.2. Common Emitter Configuration (CE)**

**4.2.1. Introduction**

In common Emitter configuration, emitter terminal is made common between input port and output port. The input is applied between base and emitter. So the input voltage is VBE and input current is IB. Output is taken between collector and emitter. So the output voltage is VCE and output current is IC

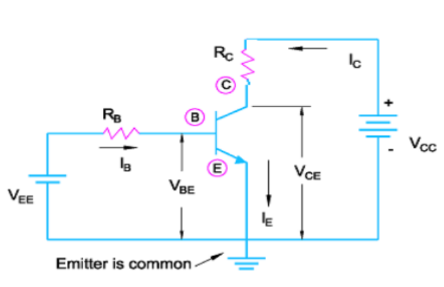


Fig 4.2.1 Common Emitter Configuration for NPN transistor

**Components in Collector Current:**

* **ICEO:**

We will see here , the reverse saturation current in CE configuration and derive its equation.

From equation (4.1.6) ,

i.e

..where  ICEO=(1+βdc)ICBO

From this we can say that ICEO is the reverse saturation current for CE configuration. ICEO is large but very small as compared to βdc IB, so neglecting this ICEO , above equation of IC reduces to,

This βdc is called current amplification factor or current gain for common emitter configuration.

•  **Relationship between αdc and βdc**

**Βdc=, αdc=**  **βdc is much higher than**  because, if then putting this value in above equation we will get .

•  **Important points of ICEO:**

We know that ICEO=(1+βdc)ICBO and value of βdc is much greater than 1, so. ICEO ICBO .

Also we know that , if we substitute IB=0 ,then IC=ICEO.i.e. if base is open, then the collector current is equal to ICEO. It shows that ICEO is a reverse saturation current in CE configuration, which flows from collector to emitter terminal when base is kept open as shown in Fig. 4.2.2.

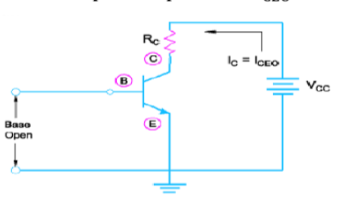


Fig.4.2.2.ICEOWith base terminal open

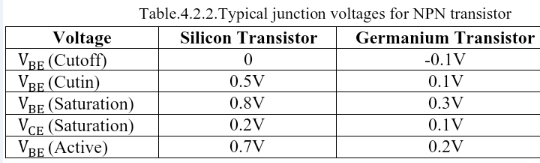
ICEO increases with increase in temperature. ICEO flows in the same direction as that of IC. Thus, IC increases with increases with increase in temperature even if IB is constant. This is known as thermal instability and thus in CE configuration, thermal stabilizing circuit is needed.

**4.2.2. Input and output characteristics of CE configuration:**

|  |  |
| --- | --- |
| **Input characteristics:** Input characteristics of CE configuration is  a plot of input  current  IB verses  input  voltage  VBE,  keeping output  voltage VCE constant. VBE is  plotted  on  the  X-axis  and  base  current IB is  plotted  on  the  Y-axis  as shown in fig. 4.2.2.1.  The input characteristics is similar to the forward V-I characteristics of diode. Up to cut in voltage, the base current is negligible but after cut in voltage it increases rapidly. Here,.    As observed in the characteristics shown  in fig. 4.2.2.1, change in base current() is very large as compared to a small  change in input voltage () so the input resistance( ri) is small in CE configuration but not as small as that of of  CB  configuration.  It means  it  gives medium range of input resistance. As shown  in  Fig.  4.2.2.1.,  we  can  also  observe  the effect  of VCE.  It  shows  that,  at  constant VBE,  IB decreases as VCE increases.    Fig 4.2.2.1. Input Characteristics of transistor in CE configuration    Fig 4.2.2.3 Collector base junction is forward biased. | **Output characteristics** :  An output characteristics of CE configuration is a plot of of  output  current  IC verses  output  voltage VCE, keeping input current IB constant. VCE is plotted on the X-axis and collector current IC  is plotted on the Y-axis as shown in fig. 4.2.2.2.    **Cutoff region:** Here JBE and JCB , both the  junctions are in reverse biased. The region below the curve for IB=0 is called cutoff region. This is because when input current IB=0 is zero, the transistor will remain in off state and is nothing but base terminal open. ICEO is very small but high as compared to ICBO.  **Saturation region:**  Here, both  the junctions are in forward biased.  Therefore  the  Collector to base junction   can  be forward biased if and  only  if VCE drops down to about 0.2V. When this drops down to 0.2V then VBE=0.7 will be  forward bias  the  collector to  base  junction.  This  is  indicated  in  fig.  4.2.2.3. Typically  the  saturation  voltage  of   transistor VCE(sat) is between 0.1 to 0.3volts.  Output current IC in this region increases rapidly with increase in VCBas shown in fig. [4.2.2.2.In](http://4.2.2.2.in/) this region IC  is  is  independent  of  IB and VCE .So,  here  the transistor is considered to be a resistor of very small value and hence used as a switch in this region is large for a small value of VCE  **Active  region:**  In  active  region  base  to  emitter junction  is  forward  biased  and  collector  to  base junction  is  reverse  biased.  Here,  the  output current IC increases  slightly  with  increase  in  output voltage  VCE at  a  constant  base  current.  Here IC is largely dependent on IB. At a fixed value of VCE if IB is increased then IC is substantially increased. This is because IC=β IB  is  possible  in  active  region  of operation. The output resistance in this region is large because ∆IC in  this  region  is  very  small.i.e.  Fig:4.2.2.2. Output Characteristics of transistor in CE configuration |

**Typical junction voltages:**

Table 4.2.2.shows the values of junction voltages for the base to emitter junction and collector to base junction for NPN transistor at 25̊C



**4.3. Common Collector Configuration (CC):**

**4.3.1 Introduction**

In common Collector Configuration, collector terminal is made common between input port and output port. Input is applied between base and collector. So the input voltage is VBC and input current is IB. Output is taken between collector and emitter .So the output voltage is VEC and output current is IE. CC configuration is also known as “Emitter Follower” configuration. Fig 4.3.1. Shows Common collector configuration for NPN transistor

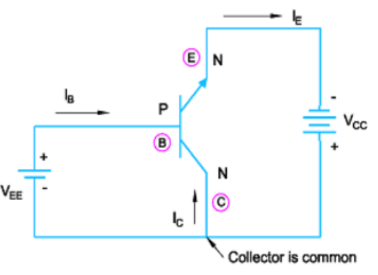


Fig 4.3.1. Common collector configuration for NPN transistor

The common collector configuration is basically same as the common emitter configuration; the only difference is that the load is connected in the emitter terminal rather than in the collector terminal.

**Current relations in CC configuration:**

•   Current gain in CC configuration (γ):

This ratio is called current gain and is denoted by γ (Gamma).

i.e.

From this we conclude that γ(current gain) is a very high value compared to αdc and βdc .

The relation between γ and αdc i.e.

**4.3.2. Input and output characteristics of CC configuration:**

|  |  |
| --- | --- |
| Input characteristics:  Input characteristics of CC configuration is a plot of input  current IB verses  input  voltage VCB,  keeping output voltage VEC constant. VBC is plotted on the X-axis and base current IB is plotted on the Y-axis as shown  in  fig.  4.3.2.  The  characteristics  is  shown for VEC=1V and  at  a  constant  output  voltage  of  VBC=1.5V  Fig 4.3.2 Input Characteristics  Here, the base emitter junction is not forward biased up to VBC=1.5V; so the base current is indicated as zero  up  to VBC=1.5V .  Once  the  base  emitter junction  is  more  and  more forward  biased then the base current increases rapidly as the VBC is increased beyond  1.5V.  In  order  to  forward  bias  the  base emitter junction, it is necessary that the input voltage VBC must be higher than the output voltage VEC.This indicates that the voltage gain in CC configuration is always less than 1. | Output characteristics:  An output characteristic of CC configuration is a plot of output current IE verses output voltage VEC,  keeping input current IB constant. VEC is  plotted  on  the  X-axis and  collector  current IE is  plotted  on  the  Y-axis  as shown in fig. 4.3.3.    Fig 4.3.3 Output Characteristics  From  the  characteristics  it  is  clear  that  output characteristics of CC configuration are similar to those for  CE  configuration.  Only  the  difference  is  that  the saturation region has all positive values as compared to the negative saturation region in CE configuration. The  CC  configuration  is  used  for  the  impedance matching because it has high input impedance and low output impedance. This is exactly opposite to that of CB configuration. |

**4.4. Comparison of Configurations:**

Comparison of all three configurations is indicated in table 4.4.1.

Table 4.4.1Comparison of CB, CE and CC configuration

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Sr.No.** | **Name of the  Parameter** | **CB** | **CE** | **CC** |
| 1 | Common terminal | Base | Emitter | Collector |
| 2 | Input Current | IE | IB | IB |
| 3 | Output Current | IC | IC | IE |
| 4 | Input voltage | VBE | VBE | VBC |
| 5 | Output voltage | VCB | VCE | VCE |
| 6 | Phase shift between Input and output | 0̊ | 180̊ | 0̊ |
| 7 | Current gain notation |  |  |  |
| 8 | Current gain | (Less than 1) | Always High | Very High |
| 9 | Voltage gain | Medium | Medium | Less than unity |
| 10 | Input resistance | Very low (20Ω) | Moderate  (1kΩ) | Very High (500KΩ) |
| 11 | Output resistance | Very high (1MΩ) | High (10KΩ) | Very Low (50Ω) |
| 12 | Applications | As a Preamplifier | Audio Amplifier | For impedance Matching |

We  can  conclude  from  this  comparison  that  CE  configuration  is  the  best  among  three  configurations.  The reason behind this is it has high voltage gain and current gain. Due to high voltage gain and current gain, power gain is also high. CE configuration has moderate values of input resistance and output resistance. So just by connecting transistor in CE stage, automatic impedance matching can takes place.

**5. DC load line:**

DC load line is nothing but biasing the transistor by giving external dc power supply and plotting a load line on the characteristics of CE configuration. Let us now study the procedure to plot this load line under DC biasing and its importance. Consider the common emitter configuration shown in Fig. 5.1.

Applying  KVL  to  the  collector  side  as  indicated  in  Fig.5.1  we  can  write,

VCC-ICRC-VCE=0

Rearranging this equation in terms of IC we get,

IC=

Compare above equation with general equation of a straight line i.e.

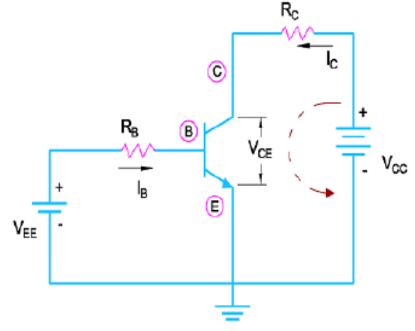


Fig 5.1Common Emitter configuration

Comparison gives, y=IC, x=VCE ,m=and constant C=

This shows that the equation IC= represents a straight line and this straight line is called as DC load line. Here , m is the slope of the line and is nothing but m=,where RC is the collector resistor and output is usually measured at this terminal i.e. collector terminal.

This resistor at   the  output  terminal  is  as  good  as  a    load resistor and so it is called as a LOAD LINE.

If we substitute VCE=0 in equation IC=then we get IC= which is ICmax or point “A” in the plot shown in Fig. 5.2. If we substitute  IC=0 in equation IC= then we get VCE=VCC which is a point “B” in the plot shown in Fig. 5.2.

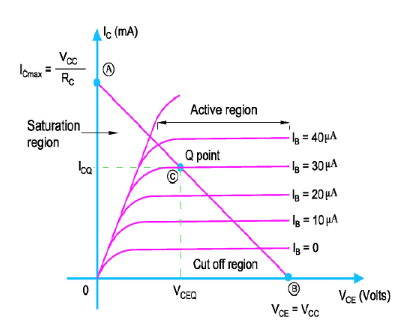


Fig 5.2 DC load line Plotted with Q point

**Quiescent Point (Q Point) or DC operating point:** The term quiescent means quiet, still or inactive. Due to this Q point is also called as “Operating point” or “bias point”. Q point is the point on the DC load line which represents the dc current flowing through a transistor (ICQ)and the  voltage across it (VCEQ) ,  when no  ac signal  is  applied at  the input.  It shows the  dc biasing condition coordinates of Q point i.e. (VCEQ, ICQ). The position of Q point on the DC load line decides the application of the transistor. For Example, if transistor is to be used as an amplifier then Q point should be placed exactly at the centre of the DC load line to avoid any distortion in the amplified output waveform.

**Stability of Q Point:**

The factors which affect the stability of Q point are:

* Change in the value of β dc
* Change in temperature
* Variation in the parameters of one transistor to the other transistor

**6. Biasing Circuits:**

Biasing circuits are used to stabilize the Q point. Basically there are three types of biasing circuits.

They are:

•  Fixed bias circuit

•  Collector to base bias circuit

•  Voltage divider bias circuit or self bias circuit

Out of these biasing circuits, Voltage divider bias circuit or self bias circuit is the best to provide stability of Q point on the DC load line.

**8. Transistor Application:**

These are two major applications of transistor. They are transistor as a switch and transistor as an amplifier. Let us study them one by one.

**8.1. Trasnistor as a switch:**

Transistor can be used as a switch when it is biased to operate in saturation region (ON state) and cut off region (OFF state )

|  |  |
| --- | --- |
| **Transistor in cut off region (OFF state /open Switch)**  When transistor is operated in cut off region both the junctions  are  in  reverse  biased  and  a  very  small reverse saturation current flows through the transistor.  The input voltage Vin is zero as shown in Fig. 8.1(a). So IB=0 and ultimately IC=0.  If we apply a KVL to the collector circuit of Fig. 8.1(a) We get,  Vcc-IcRc-VCE=0  But as Ic=0, VCE=VCC.  This shows that the voltage drop across the transistor i.e.  VCE is  high.  Transistor  offers  a  very  high resistance  to  the  flow  of  current  through  it,  ideally infinite as collector current is zero. i.e. IC = 0 so we can say that in cut off region transistor is equivalent to an open switch or said to be in OFF state as shown in Fig.8.1(b).    Fig 8.1.(a)Cut off region Fig 8.1.(b)Equivalent circuit | **Close switch**  When transistor is operated in saturation region both the junctions  Vin   is  applied  at  the  base  of  the  transistor  as shown in Fig. 8.2(a). Base resistance RB is selected such that a large amount of IB flows.  This will saturate the transistor.  In order to saturate  the  transistor  following condition should be satisfied.  When transistor is saturated, the voltage drops across the transistor i.e.  VCE is very small.  It  offers  a  very  less resistance,  ideally  zero  and  thus  maximum  collector current can flow through it. This indicates that transistor acts  as  a  closed  switch  or  is  said  to  be  in  ON  state  as shown in Fig. 8.2(b)    Fig 8.2.(a)Saturation region Fig 8.1.(b)Equivalent circuit |

**Important Points to be noted:**

•  When the input is low (0 Volts), the transistor is OFF, acts as an open switch and output voltage VCE=VCC. •  When  the  input  is  high,  the  transistor  is  ON, acts  as  a  close  switch  and  output  voltage VCE=VCE(sat)≈0V.

•  Input and output voltage indicates that output of the transistor is 180̊ out of phase with the input. As transistor is  connected in  CE configuration  we  can say that  there  is  a phase  shift  of  180̊ between  input  and  output  voltage  in  CE configuration.

•  Ideally if input applied is a square wave then output will be a inverted square wave.

•  Practically switching between ON state to OFF state or OFF state to ON state does not take place instantly so some delays are introduced and are indicated as shown in Fig. 8.3

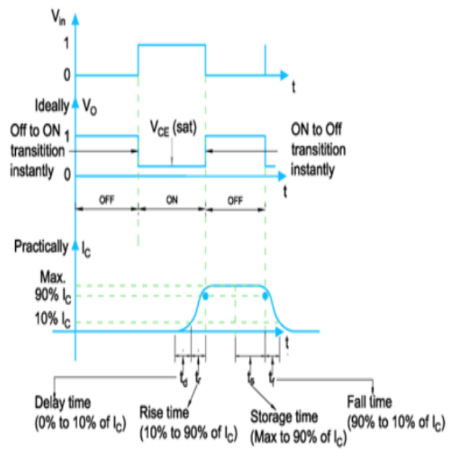


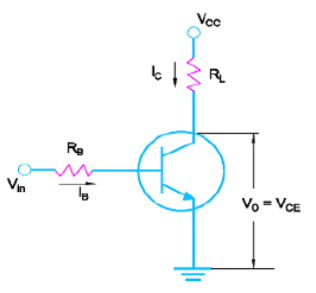
Fig. 8.3 Input and Output waveforms for Transistor switching

**8.2. Transistor as an amplifier:**

Amplification is a process of increasing or magnifying the strength of the input

**8.2.1. Transistor as a voltage amplifier:**

A voltage amplifier is basically designed to amplify the input voltage. Referring the simplified circuit of a BJT as shown in Fig.8.2.1,



The transistor is connected in CE configuration.  The  output  voltage  is  measured  at  the  collector  with  respect  to ground. VO=VCE.

If there is a small change in input voltage Vin then base current IB also changes and is represented by,

As input current IB changes, the corresponding collector current changes and is          Fig. 8.2.1 Simplified circuit of BJT     given by,

The corresponding change in output voltage Vo is given by,

Substituting the value of ∆IC we get,  Rearranging properly,

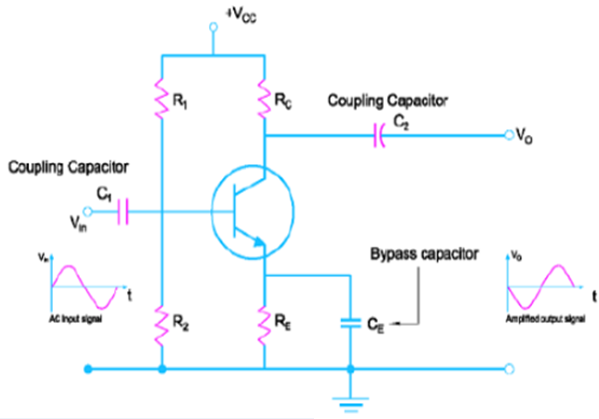
This equation indicates that for a small change in Vin we get a large change in Vo by a multiplication factor of  and voltage amplification takes place. Hence BJT can be used as a voltage amplifier.

**8.2.2. Transistor as a current amplifier:**

Transistor can be used as a current amplifier only in CE and CC configuration. Because we know that,   Current gain in CE configuration is = and current gain in CC configuration is =.

As is much larger than 1, we can say that current gain in CE and CC configuration is large. So transistor connected in CE and CC configuration can be used as a current amplifier. Transistor can’t be used as a current amplifier in CB configuration, because the current gain αdc is less than unity.

**8.2.3. Single stage RC coupled CE amplifier:** The  circuit  diagram  of  single  stage  RC  coupled  CE amplifier is shown in Fig. 8.2.3.1.



The capacitors C1 and C2 are called  as  coupling  capacitors.  The  load  resistor  is coupled to the amplifier through the coupling capacitor, this amplifier is called as RC coupled amplifier. As the transistor is connected in CE configuration it is called as CE amplifier.

Self biasing and active region of operation of transistor is provided to the circuit using R1,R2 and RE.

The coupling capacitor C1 is used couple the ac input voltage Vin to the base of the transistor .It is used to block dc component at the input. The output coupling capacitor C2 is used to couple the amplifier output to the load resistance or to the next stage of the amplifier. It is used to pass only AC part of the amplified signal to the load. The capacitor CE is connected in parallel with the emitter resistor RE and is called as emitter bypass capacitor. This capacitor offers a very low reactance to the amplified AC signal so the emitter resistor RE gets bypassed through CE

for only AC signals. This will increase the voltage gain of the amplifier. We have already studied how the BJT provides voltage amplification in CE configuration at the last point under 8.2.1.

**Selection of Q point:**

The criteria for selecting Q point to operate the transistor as an amplifier is: •  The Q point should not be too close to the saturation region.

•  The Q point should not be too close to the cutoff region.

•  The Q point should be located at the center of the DC load line. This will ensure that the amplified signal is an exact replication of the input signal. The first two criteria should be satisfied in order to avoid any waveform distortion in the amplified output signal.

Fig. 8.2.3.2 (a),Fig. 8.2.3.2 (b) and Fig. 8.2.3.2 (c) are indicated for the three criteria mentioned above i.e. effect on the output due to shifting of Q point too close to the saturation region is indicated in Fig. 8.2.3.2 (a).Here, as seen from the figure the negative part of the output voltage waveform gets clipped off. The effect on the output due to shifting of Q point too close to the cutoff region is indicated in Fig. 8.2.3.2 (b). As seen from the figure the positive part of the output voltage waveform gets clipped off. The exact replication of the input signal at the output i.e. proper amplification is indicated in Fig 8.2.3.2.(c)

|  |  |  |
| --- | --- | --- |
| (a) Effect of Q point close to the saturation region | (b) Effect of Q point close to the Cut off region | (a) Proper amplification |