Copperbelt University

School of Information and Communications Technology

Bachelor of Science in Computer Engineering

2020 Sessional Examinations

September / October

CS270: Introduction to Computer Engineering

Instructions to Candidates:

1. Time allowed is THREE (3) hours
2. This paper contains SEVEN (7) questions
3. You are required to answer FIVE (5) questions. In Section A, Questions One and Two are compulsory. Choose THREE (3) questions from Section B
4. Questions One and Two each carries TWENTY-SIX (26) marks. In Section B, each question carries SIXTEEN (16) marks
5. Neat and clearly written work is encouraged

Section A: Practical Questions, answer ALL **(Total: 52 Marks)**

Instructions:
In this Section, you are given two practical Questions. Use these instructions to answer the Questions.

Assume you are given one of the software such as: Logisim, Eagle and Circuit Wizard, build complete circuits and answer the questions given below:

QUESTION 1. **(Total: 26 marks)**

(a) Briefly, discuss the principles behind the concept of register with parallel load. [2 marks]

(b) As a Computer Engineer, a Company has hired you to design a register with parallel load. Using the appropriate apparatus, on your answer sheet, design the requested register by clearly showing the appropriate gates and other relevant components. [10 marks]

(c) On the provided answer sheet, dry run the execution of the register with parallel load you have developed on Question 1 (b), particularly on the given input situations: [14 marks]

(i) Load = 0; Clock (clk) = 1 or on; and Clear (clr) = 0 or off
(ii) Load = 0; Clock (clk) = 1 or on; and Clear (clr) = 0 or off
(iii) Load = 1; Clock (clk) = 0 or on; and Clear (clr) = 0 or off
(iv) Load = 1; Clock (clk) = 1 or on; and Clear (clr) = 0 or off
(v) Load = 1; Clock (clk) = 1 or on; and Clear (clr) = 1 or on
(vi) Continue explaining of what happens after the execution in (v).

QUESTION 2. **(Total: 26 marks)**

(a) In reference to the shift registers, describe the concept of serial in/serial out (SISO) shift register. [2 marks]

(b) The School of ICT at CBU would like to use the serial in/serial out (SISO) shift register for their tutorial class. As a person with such skills and using the right apparatus, on your answer sheet, design and build SISO shift register. On the created or developed register, clearly label all the relevant components. [10 marks]

(c) In item (b) having designed the serial in/serial out (SISO) shift register, on the provided hard copy of your answer sheet, demonstrate the execution of SISO shift register in relation to the given input situations. [14 marks]

(i) Serial Data Input = 0; Clock (clk) = 1 or on

(ii) Serial Data Input = 1; Clock (clk) = 1 or on

(iii) Serial Data Input = 0; Clock (clk) = 0 or off

(iv) Serial Data Input = 1; Clock (clk) = 0 or off

Section B: Answer any Three (3) questions from this Section **[Total: 48 marks]**

QUESTION 3. **(Total: 16 marks)**

(a) Briefly, explain why the demultiplexer is called a data distributor? [2marks]

(b) Using any real life example of your choice, demonstrate a typical application of demultiplexer. [4 marks]

(c) A demultiplexer sends a single input to multiple outputs, depending on the select lines. Design and construct a 1-to-8 demultiplexer and label all the relevant components. [10 marks]

QUESTION 4. **(Total: 16 marks)**

(a) In reference to integrated circuit, discuss the significance of packing more electronic components onto a chip. [3 marks]

(b) What is the significance of the semiconductor devices in connection with the evolution of integrated circuit? [4 marks]

(c) Briefly, discuss the history and the process of the large scale integration (LSI) circuit. [4 marks]

(d) Identify and discuss at least the five disadvantages of the integrated circuits. [5 marks]

QUESTION 5. **(Total: 16 marks)**

(a) Define the concepts of datapath. [3 marks]

(b) In reference to the computer processor, distinguish between brain and brawn. [4 marks]

(c) Using a clearly labelled diagram, illustrate in detail the implementation overview of the datapath. [9 marks]

QUESTION 6. **(Total: 16 marks)**

(a) Discuss in detail the functions of an enabler input on a multiplexer chip. [3 marks]

(b) In reference to multiplexer, define the concept of strobe. [2marks]

(c) Explain as to why the multiplexer circuit can be classified and used as parallel to serial converter. [3marks]

(d) Using a clearly labelled diagram, design a 4-to-1 multiplexer using transmission gates. [8 marks]

QUESTION 7. **(Total: 16 marks)**

(a) Briefly, describe the concept of binary decoder. [2marks]

(b) Discuss in detail, what control signals that may be necessary to operate a 1-line-to-16 line decoder? [4 marks]

(c) What is the distinction between a NEXT state decoder and a flip-flop? [3 marks]

(d) How can the active condition (HIGH or LOW) or the decoder output be determined from the logic symbol? [4 marks]

(e) Discuss the first step in the design of memory decoder. [3 marks]