1. Description

1.1. Project

Project Name	rubik
Board Name	NUCLEO-F411RE
Generated with:	STM32CubeMX 5.6.0
Date	03/20/2020

1.2. MCU

| MCU Series	STM32F4
MCU Line	STM32F411
MCU name	STM32F411RETx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration
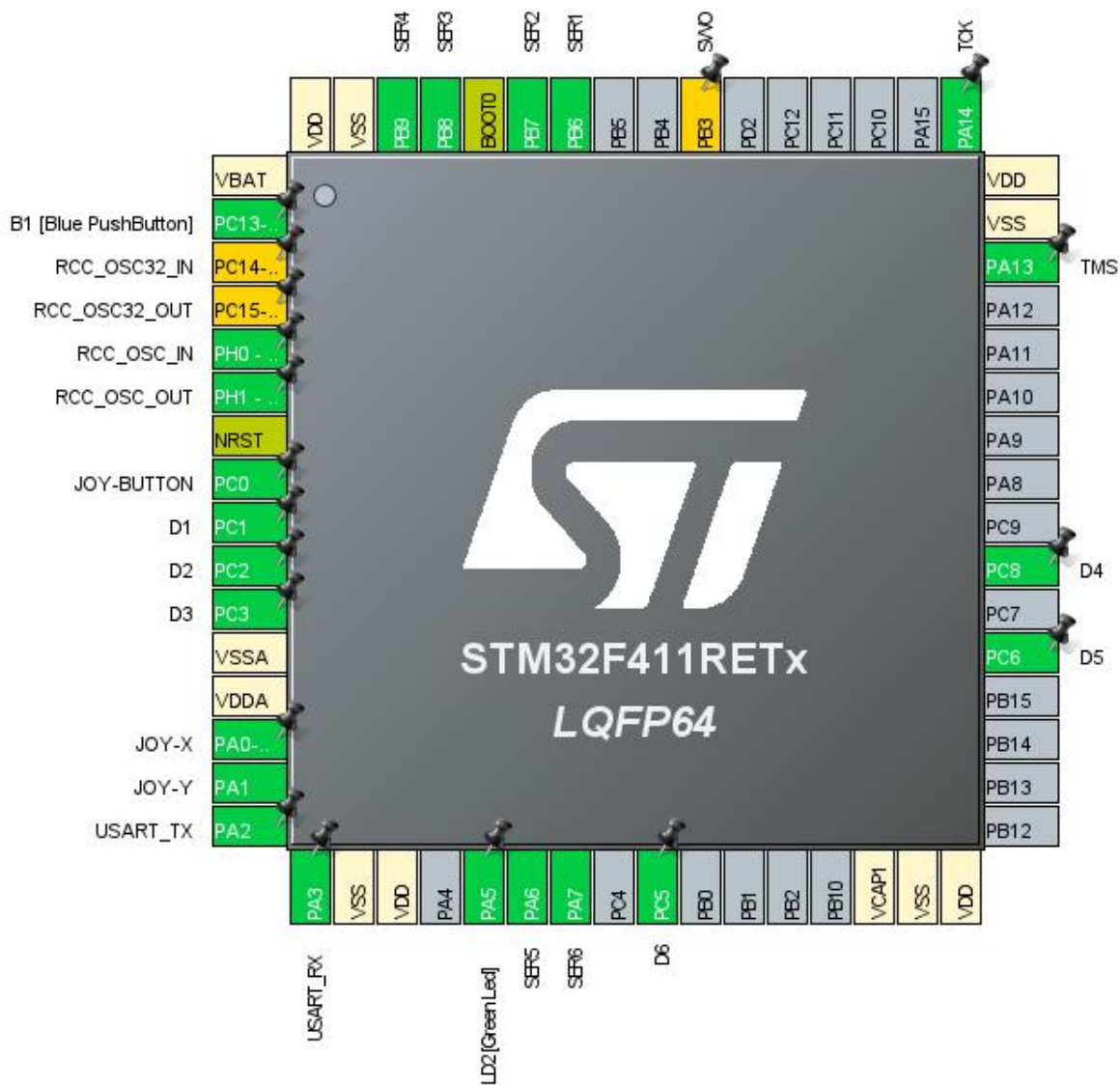
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13-ANTI_TAMP	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN *	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT *	I/O	RCC_OSC32_OUT	
5	PH0 - OSC_IN	I/O	RCC_OSC_IN	
6	PH1 - OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0 **	I/O	GPIO_Input	JOY-BUTTON
9	PC1 **	I/O	GPIO_Output	D1
10	PC2 **	I/O	GPIO_Output	D2
11	PC3 **	I/O	GPIO_Output	D3
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	ADC1_IN0	JOY-X
15	PA1	I/O	ADC1_IN1	JOY-Y
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
21	PA5 **	I/O	GPIO_Output	LD2 [Green Led]
22	PA6	I/O	TIM3_CH1	SER5
23	PA7	I/O	TIM3_CH2	SER6
25	PC5 **	I/O	GPIO_Output	D6
30	VCAP1	Power		
31	VSS	Power		
32	VDD	Power		
37	PC6 **	I/O	GPIO_Output	D5
39	PC8 **	I/O	GPIO_Output	D4
46	PA13	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	TCK
55	PB3 *	I/O	SYS_JTDO-SWO	SWO
58	PB6	I/O	TIM4_CH1	SER1
59	PB7	I/O	TIM4_CH2	SER2
60	BOOT0	Boot		

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
61	PB8	I/O	TIM4_CH3	SER3
62	PB9	I/O	TIM4_CH4	SER4
63	VSS	Power		
64	VDD	Power		

** The pin is affected with an I/O function

 * The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration
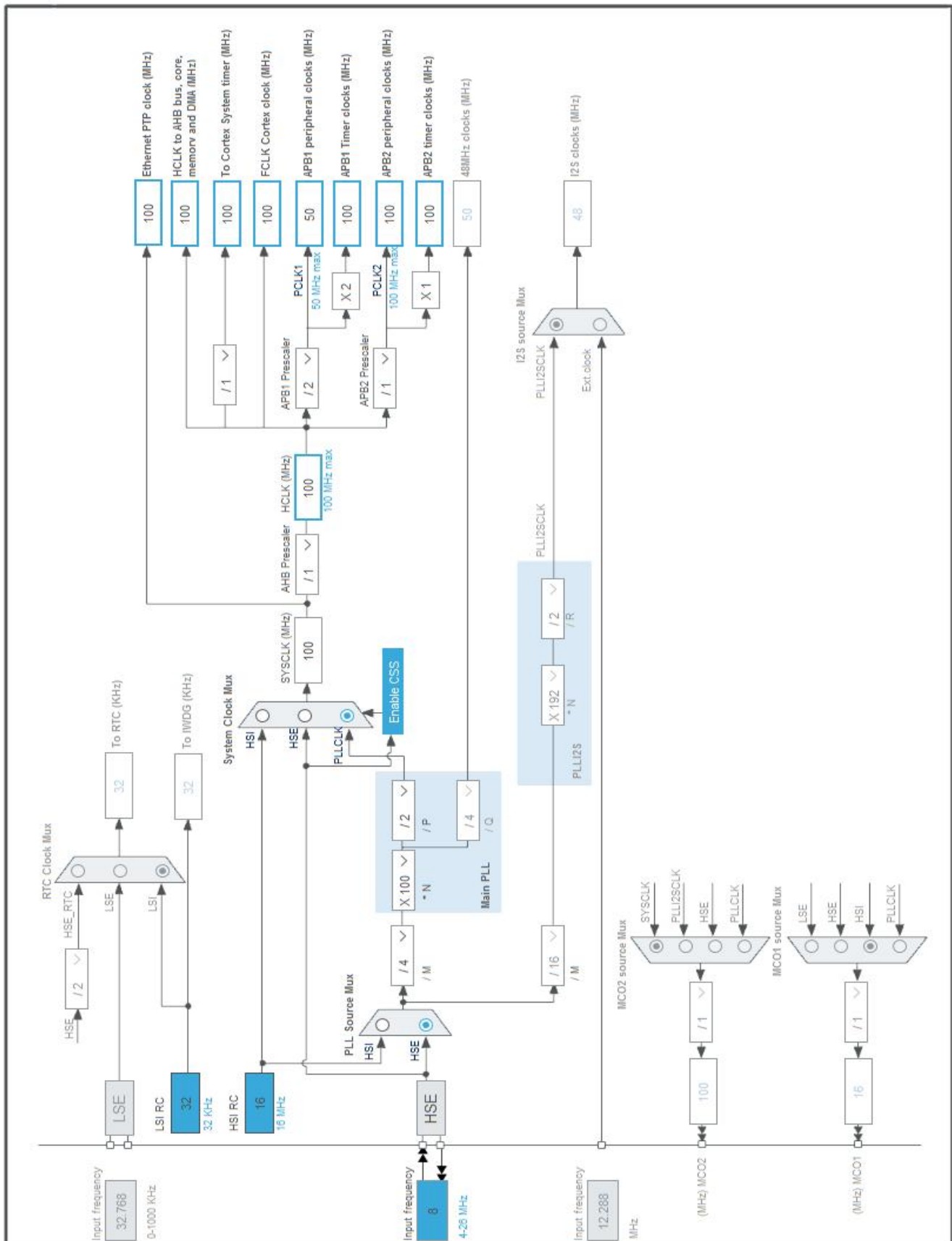
5. Software Project

5.1. Project Settings

Name	Value
Project Name	rubik
Project Folder	C:\Users\MF\STM32CubeIDE\workspace_1.3.0\rubik
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.25.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F411
MCU	STM32F411RETx
Datasheet	026289_Rev6

6.2. Parameter Selection

Temperature	25
Vdd	3.6

6.3. Battery Selection

|	
Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.6	3.6
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	FLASH/ART/PREFETCH	n/a
CPU Frequency	100 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LPLV Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	22.5 mA	10 µA
Duration	0.1 ms	0.9 ms
DMIPS	125.0	0.0
Ta Max	101.19	105
Category	In DS Table	In DS Table

6.5. RESULTS

Sequence Time	1 ms	Average Current	2.26 mA
Battery Life	2 months, 1 day, 18 hours	Average DMIPS	125.0 DMIPS

6.6. Chart

Consumption Profile by Step
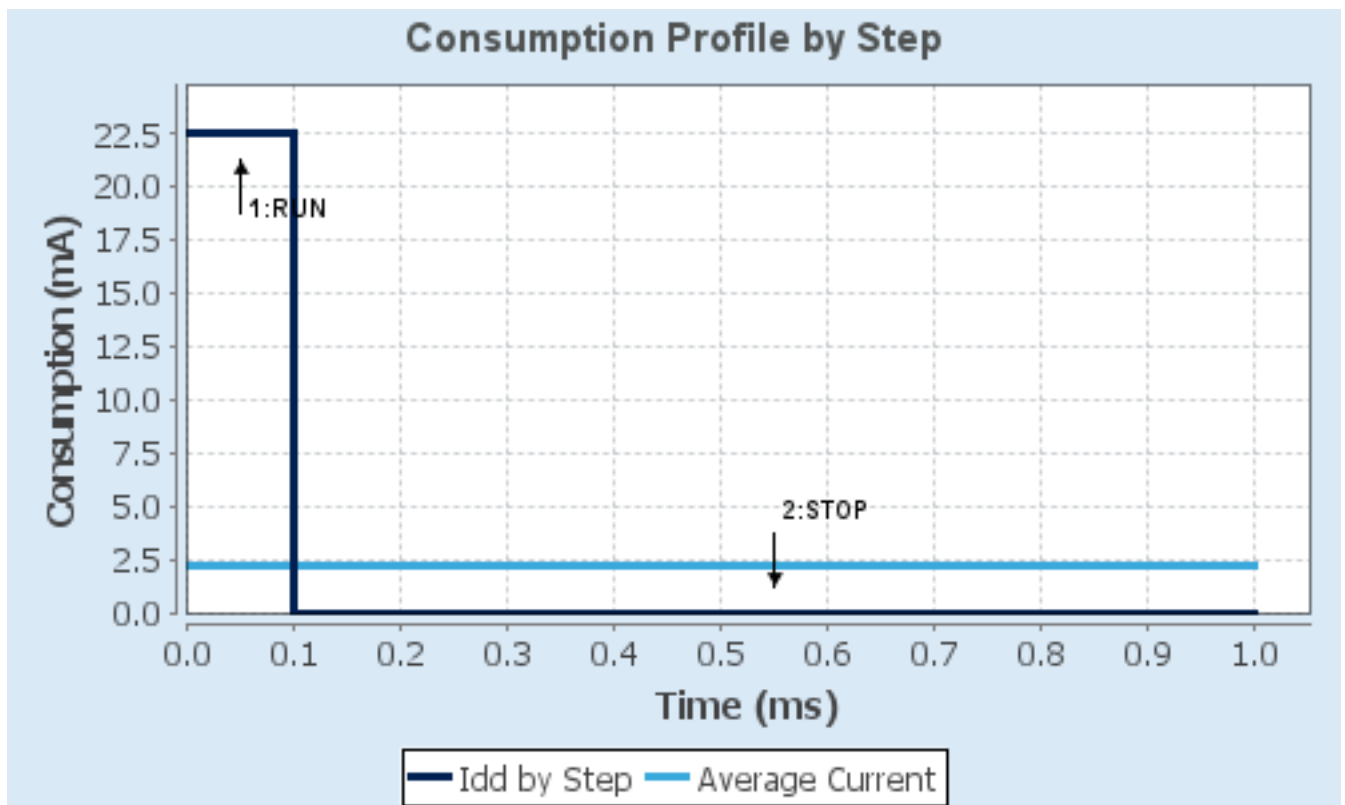
7. IPs and Middleware Configuration

7.1. ADC1

mode: IN0

mode: IN1

7.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel 1 ***
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. GPIO

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled

Data Cache	Enabled
Flash Latency(WS)	3 WS (4 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.4. SYS

Debug: Serial Wire
Timebase Source: SysTick

7.5. TIM3

Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**999 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable

Fast Mode	Disable
CH Polarity	High

7.6. TIM4

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**999 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.7. USART2

Mode: Asynchronous

7.7.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	JOY-X
	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	JOY-Y
RCC	PH0 - OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1 - OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
TIM3	PA6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	SER5
	PA7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	SER6
TIM4	PB6	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	SER1
	PB7	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	SER2
	PB8	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	SER3
	PB9	TIM4_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	SER4
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	USART_TX
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	USART_RX
Single Mapped Signals	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	SWO
GPIO	PC13-ANTI_TAMP	GPIO_EXTI13	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PC0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	JOY-BUTTON
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D1
	PC2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D2
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D3
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Green Led]
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D6
	PC6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D5

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D4

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
USART2 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
FPU global interrupt	unused		

* User modified value

9. Predefined Views - Category view : Current

10. Software Pack Report