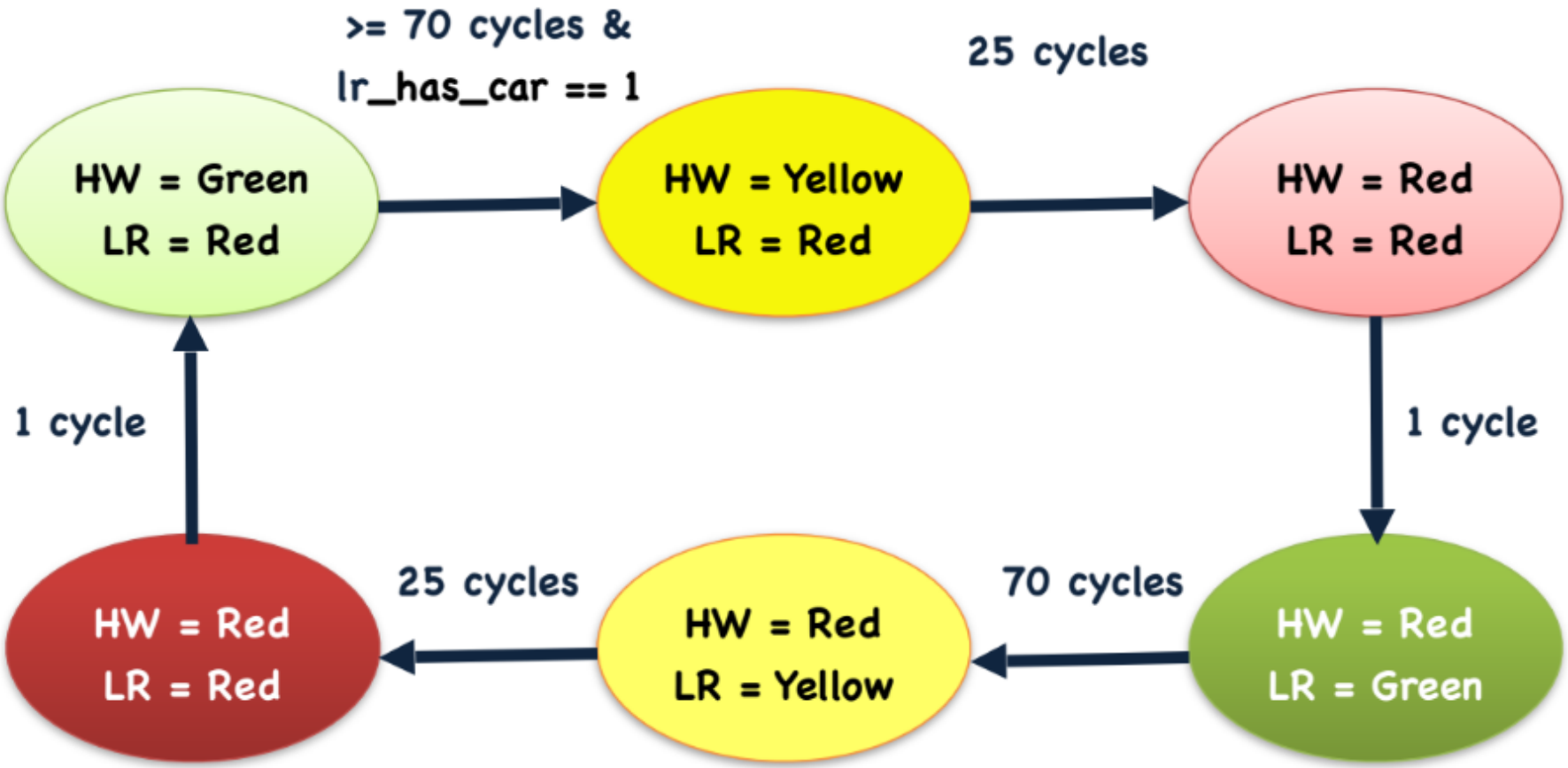
Verilog Advanced Question 2

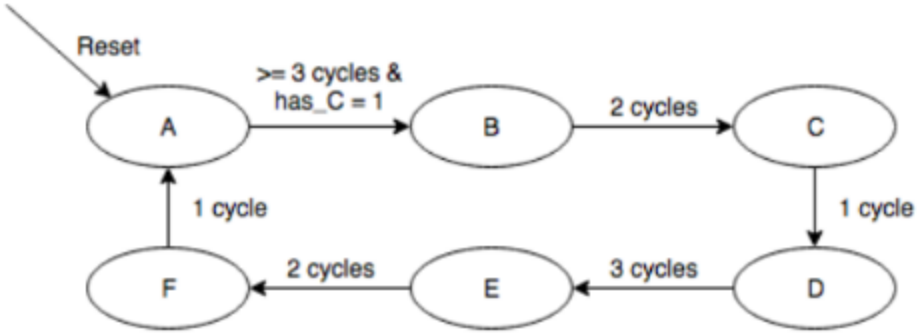
- **Traffic light controller** for a highway (**HW**) and local road (**LR**) intersection
- **HW** has higher priority and should be green as long as possible
- **LR** has a sensor to detect cars on it. When a car is sensed, LR turns green shortly
- Green light is **at least 70** clock cycles and yellow light is **25** clock cycles
- **Input**: **clk**, **rst_n**, **lr_has_car**; **Output**: **hw_light[2:0]**, **lr_light[2:0]**
  - **hw_light** & **lr_light**: bits [2:0] represent **Green**, **Yellow**, and **Red**, respectively

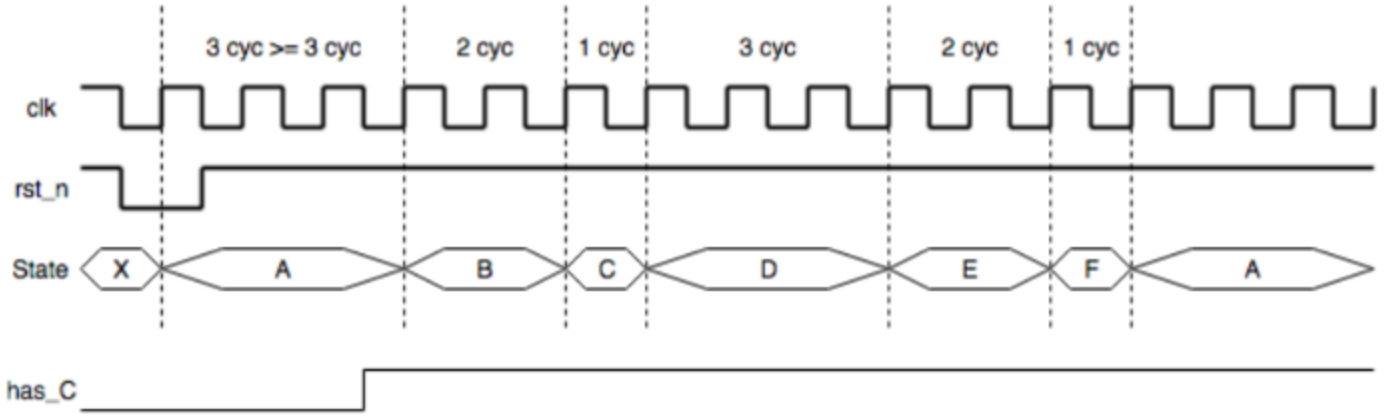
Verilog Advanced Question 2 (Con't)

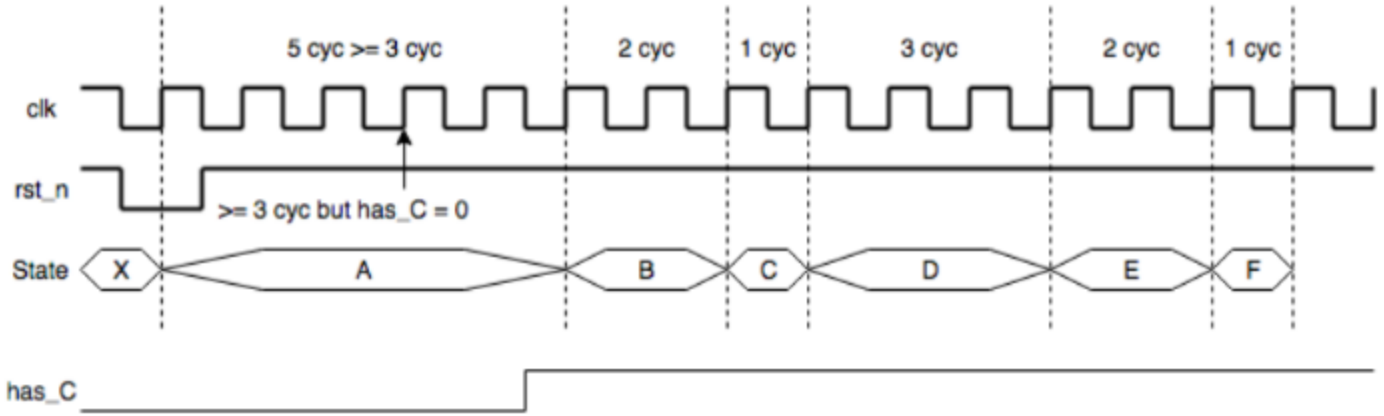
- **Traffic light controller** Finite State Machine
- **Please complete the FSM in your report** (some arrows are removed intentionally)



Verilog Advanced Question 2 (Con't)







- **A Traffic light controller "example"** timing diagram is illustrated on the left
- **Please make sure that your state transitions follows the timing digram correctly**