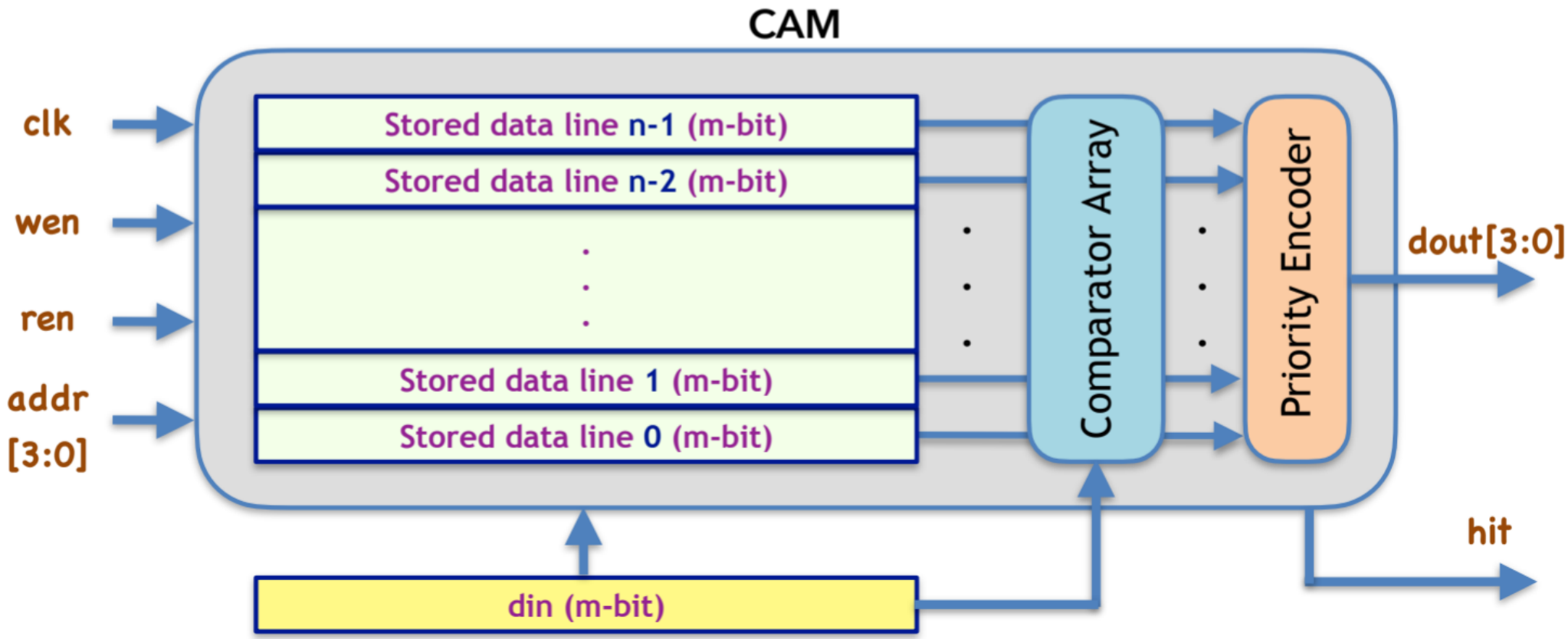
Verilog Advanced Question 1

- **Content-addressable memory (CAM) design**
  - Design a CAM that stores **n** sets of **m**-bit data lines **(n = 16, m = 8)**
  - Input: **clk, wen, ren, addr[3:0], din[m-1:0]**
  - Output: **dout[3:0], hit**



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- When **wen == 1'b1**, write **din** to CAM[**addr**] and set **dout** to **4'b0** and **hit** to **1'b0**
- When **ren == 1'b1**:
  - If there is only one matching data in the CAM, set **dout** to the matching data's address and set **hit** to **1'b1**
  - If there are multiple matches in the CAM, set **dout** to the **smallest address among them** and set **hit** to **1'b1**.
  - If there is no match in the CAM, set **dout** to **4'b0** and set **hit** to **1'b0**
- When both **wen** and **ren** are **1'b1**, **perform read operation only and ignore the write request**
- When both ren and wen are 1b'0, set **dout** to 4'b0 and set **hit** to 1'b0
- Please refer to the next page for example waveform

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