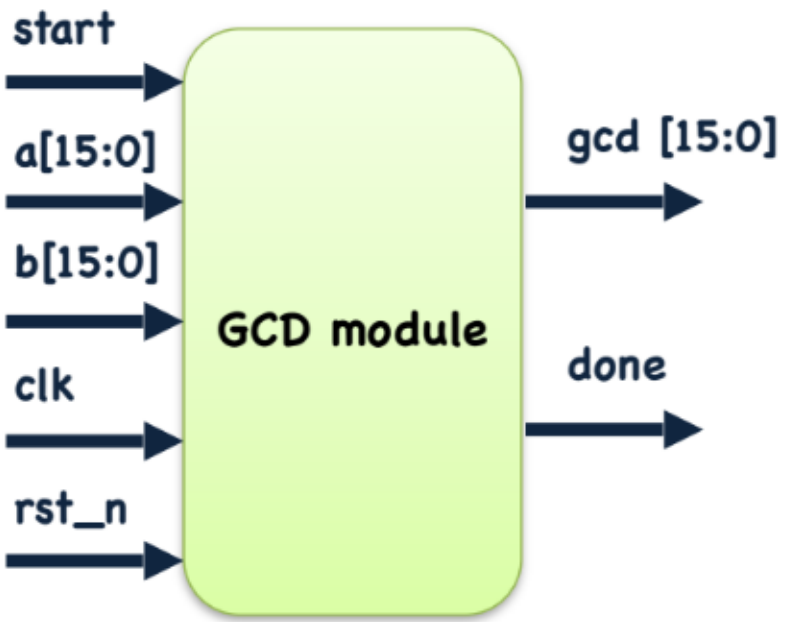
Verilog Advanced Question 3

- **Greatest common divisor**
- Calculate the greatest common divisor of two numbers **a** and **b**
- Top level block diagram and pseudo code are as follows
  - You **shall not** use **loop statements and modulus (%)** in your Verilog codes



GCD pseudo code

```
Function gcd (a, b)
begin
    if (a == 0)
        return b;
    while (b != 0)
    // Do the following operation once per clock cycle
    begin
        if (a > b)
            a = a - b;
        else
            b = b - a;
    end
    return a;
end
```

Verilog Advanced Question 3 (Cont'd)

- Three states are used: **WAIT**, **CAL**, and **FINISH**
- **WAIT state**
  - Wait for **start == 1'b1** (**one cycle**) to begin the operation (**and fetch the inputs**)
  - The values of **a** and **b** may change during operation. Be sure to fetch and buffer them when the state changes from **WAIT** to **CAL**
  - When **rst_n == 1'b0**, reset the module to the **WAIT state**
- **CAL state**
  - Perform the **subtraction operations once per cycle**
- **FINISH state**
  - Output the **gcd** result for **two cycles**
  - **done** == **1'b1** for **two cycles**