



# IP2368 Register Description

# IP2368 Register Description Doc**Document**

### Version/revision history

releases	dates	revision	Proposed/revise
			d by
V1.00	2021-10-25	Initial release	IT360
V1.60	2022-05-16	Revision of	IT360
		typography and	7 1 -
		instructions	
V1.61	2022-07-13	Increase VSYS	IT360
		power mail	
		Memory High 8-	
		bit	

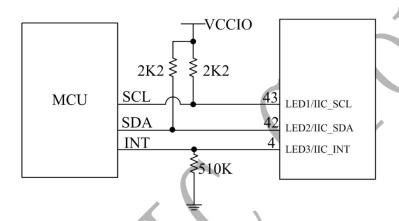


# Description Document

### 1 Typical Application Notes

#### **1.1 I2C** Connection Method

IP2368 can be used as a slave device, MCU can read or set the voltage, current, power and other information of IP2368 through I2C interface, IP2368 I2C connection is as follows:



#### **1.2 I2C** Notes

- The I2C device address of IP2368 is 0xEA for write and 0xEB for read, if other address is required, it can be customized;
- The I2C communication voltage of IP2368 is 3.3V. If the MCU side is 5V, you need to add a level converter chip to switch to 3.3V;
- ➤ IP2368 INT application description: IP2368 will wake up when it detects INT is high when it sleeps, after waking up, IP2368 actively pulls up INT, and after 100ms, MCU can carry out I2C communication and read/write operation of registers; before IP2368 enters hibernation, it will switch to input high-resistance to detect the INT status, if it is high level, MCU is considered that If it is high, the MCU will think that the IP2368 is not allowed to enter hibernation; if it is low, the IP2368 will enter hibernation; the MCU will stop accessing the IC within 16ms after detecting that the INT is low;
- ➤ The I2C of IP2368 supports up to 250k communication frequency. Considering the clock deviation, it is recommended to use 100k-200k for the I2C communication clock of MCU;
- If you want to modify the value of a certain register in IP2368, you need to read out the value of the corresponding register first, and then write the calculated value into the register after performing the sum or operation on the Bit that needs to be modified, and you can't modify the value of other registers that are not open. The default value of the register is based on



the value read, and the default value may be different for **Description** 

- ▶ IP2368 I2C communication is real-time data, after receiving the request, you need to enter the interrupt for data preparation, the preparation time is longer, so the MCU needs to judge whether it receives ACK and increase the delay time by 50us after sending the address in I2C communication (refer to the I2C application example); it is recommended to read by single byte, 100k I2C communication frequency, and increase the delay time by 1ms between each byte;
- At the end of I2C read data, after reading the last byte, must give NACK signal, otherwise IP2368 will think that it is still continuing to read data, the next clock will continue to output the next data, resulting in failure to receive the STOP signal, and finally read error;



- Reserved registers must not be written to or changed from the **Persister Number**, or else unintended results will occur. The operation of the register must be carried out according to read-modify-write, only modify the bit to be used, not modify the value of other unused bit;
- ➤ This document is only for IP2368\_I2C\_COUT/IP2368\_I2C\_NACT models, other models are invalid;

#### **1.3 I2C** Application Examples

After the INT pin of IP2368 is continuously high for 100ms, MCU can carry out I2C communication, initialize the registers first (modify the registers only when you need to modify the special functions, if you don't need to modify them, you can not write the registers); then read the internal information of IP2368 (battery level, charging and discharging status, key status); finally, carry out the operation of the special requirements (such as special indicator, charging and discharging management, fast charging request management); MCU needs to stop accessing I2C within 16ms after detecting the INT pin is low. Then read the internal information of IP2368 (power level, charging/discharging status, key status); finally, perform special operations (e.g. special indicator, charging/discharging management, fast charging request management); after the MCU detects that the INT is low, the MCU needs to stop accessing the I2C within 16ms.

#### Example:

Write data to 0x05 register 0x5A



Figure 1 I2C Write 0x05

#### Read back data from 0x05 register

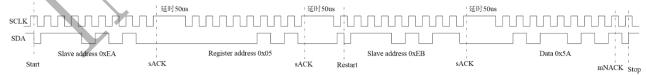
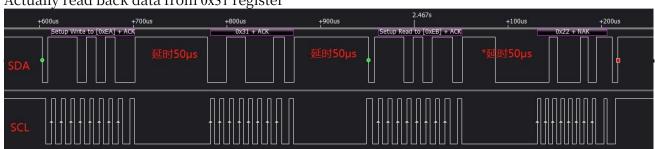


Figure 2 I2C Read 0x05

Actually read back data from 0x31 register





# IP2368 Register Description Document

Figure 3I2C Read 0x31

### Description Document

# 2 Register List:

# 2.1 Readable/Writable Operation Registers

# **SYS\_CTLO** (charge enable register)

Bit(s)	Name	Description	R/W	RESET
7	En_LOADOTP	Power-on wake-up reset register value enable	R/W	1
		0: Do not reset register values		
		1: Reset register values		
		This bit is not recommended to be changed to 0. If	) 7	
		it needs to be changed, the software needs to		
		periodically		
		Reset register default value, e.g. after VINOk VBUOk		
		signal trigger		
6	En_RESETMCU	MCU Reset Register	R/W	0
		Write 1: reset the register to the default value, the		
		bit will be restored automatically after reset.		
		Reset to 0		
5	En_INT_low	When there is an abnormality, INT is pulled down	R/W	0
		by 2MS to indicate that there is an abnormality in		
		the MCU.		
		1: Enable		
	•	0: disable		
4	En_Vbus_SinkDPd	C Port Input DM DP Fast Charge Enable	R/W	1
	M	1: Enable		
		0: disable		
3	En _Vbus_SinkPd	C Port Input Pd Fast Charge Enable	R/W	1
		1: Enable		
		0: disable		
2	En_Vbus_SinkSCP	C Port Input SCP Fast Charge Enable	R/W	1
		1: Enable		
		0: disable		
1	En_Vbus_Sinkctrl	C port MOS input enable	R/W	1
		1: Enable, turn on C port MOS		
		0: disable, disable C port MOS		
SYS_CT	L1n(Series sec	t <b>ionsetting</b> ,g <b>batter(yetype</b> ;g <b>currtent set</b> turned off)	tingwno	de)1
		1: Enable		
12C Addr	ess OXEA Regist	er.address = 0x01		
Bit(s)	Name	Description	R/W	RESET
7:4	Reserved			
3	En_BATmode_set	Set battery type enable (battery type by	R/W	0
		register 0x01[2]) 1: Enable, allow to set		
		battery type		
		0: disable, do not allow setting battery type		



2	Set_BATmode	Battery type setting  0: lithium iron phosphate battery, single cellmen trickle constant current voltage 2.5V, full voltage 3.6V or so 1: Ordinary lithium batteries, single cell trickle current voltage 3.0V, full voltage 4.2V or so	onr/w t	1
1	En_lsetmode_set	Select current setting mode enable  1: Enable, current setting mode is allowed to be selected 0: disable, current setting mode is not allowed to be selected	R/W	0
0	Set_Isetmode	Select current setting mode (current and power register 0x03 [6:0]) 0: Iset sets the battery side current. 1: Iset sets the power at the input.	R/W	1

# **SYS\_CTL2** (Vset full voltage setting)

I2C Address OXEA Register address = 0x02

Bit(s)	Name	Description	R/W	RESET
7	En_Vset_set	Set full voltage enable	R/W	0
		1: Enable, allows setting of full voltage		
		0: disable, full voltage setting is not allowed		
6:0	Vset	Full voltage setting		00 1010
		Lithium iron phosphate battery mode		
		(0x01[2]=0), single cell full voltage		
		Vset=N*10+3500mV (max. 3.7V)		
		In normal Li-ion battery mode (0x01[2]=1), single		
		cell full voltage		
		Vset=N*10+4000mV (up to 4.4V)		

# **SYS\_CTL3** (lset charging power or current setting)

Bit(s)	Name	Description	R/W	RESET
7	En_lset_set	Set charging power or current enable	R/W	0
		1: Enable, allows to set the charging power or		
		current		
		0: disable, does not allow setting charging power or		
		current		
6:0	Iset	Battery-side current or power setting	R/W	0111100
		When set to battery-side current (0x01[0]=0), the		
		battery-side current		
		Iset=N*100mA (5A maximum)		
		When set to charge input power mode		
		(0x01[0]=1), the set charge power		
V1.61	http://www.injoin	icRomak=N*1W (chargin/gramax. 100W) Copyright (	2022, Injo	nic Corp.

# **SYS\_CTL4** (battery capacity setting)

# Description Document

I2C Address OXEA Register address = 0x04

Bit(s)	Name	Description	R/W	RESET
7	En_FCAP_set	Set battery capacity function enable	R/W	0
		1: Enable, allows setting the battery capacity 0: disable, does not allow setting battery capacity		
6:0	Fcap	Battery Capacity FCAP= N*200mAh	R/W	0101000

### **SYS\_CTL6** (current power level)

I2C Address OXEA Register address = 0x06

Bit(s)	Name	Description	R/W	RESET
7:0	Cap_Now	Current power level (read/write)	R/W	х
		Cap_Now=N		

# SYS\_CTL7 (trickle charge current, threshold and charge timeout settings)

Bit(s)	Name	Description	R/W	RESET
7:4	Itk	Trickle charge current setting (maximum trickle	R/W	0100
		charge current 400ma)		
		Itk=N*50mA		
3:2	Vtk	Trickle-to-constant-current charging voltage	R/W	10
		threshold for a single battery		
		When set to lithium iron phosphate mode		
		(0x01[2]=0)		
		00: 2.3V		
	1	01: 2.4V		
		10: 2.5V		
		11: 2.6V		
		When set to normal lithium battery mode		
		(0x01[2]=1)		
		00: 2.8V		
		01: 2.9V		
		10: 3.0V		
		11: 3.1V		
1:0	Charge_OT	Charge Timeout Setting	R/W	10
		00: disable, no charge timeout		
		01: 24h		
		10:36h		
		11:48h		



# SYS\_CTL8 (Stop Charge Flow and Recharge Threshold Setting) Description Document

I2C Address OXEA Register address = 0x08

Bit(s)	Name	Description	R/W	RESET
7:4	Istop	Stop Charge Current Setting Istop=N*50mA	R/W	0010
3:2	Vrch	recharge threshold 00: No re-charging function after full charge 01: VTRGT - N*0.05 10: VTRGT - N*0.1 11: VTRGT - N*0.2 VTRGT Charge Voltage N Battery series connection	R/W	10
1:0	Reserved			

# **SYS\_CTL9** (standby enable and low power voltage setting)

I2C Address OXEA Register address = 0x09

Bit(s)	Name	Description	R/W	RESET
7	En_Standby	standby enable	R/W	1
		1: Enabling		
		0: not enabled		
6	En_BATlow_Set	Battery low voltage setting enable (battery	R/W	0
		voltage setting register 0x0A) 0: disable		
		1: Enable		
5	En_BAT_Low	Turn off the battery low power shutdown	R/W	0
		function		
		0: disable		
		1: Enable		
4:0	Reserved			
	'\			1

# **SYS\_CTL10** (battery low voltage setting)

Bit(s)	Name	Description	R/W	RESET
7:5	Set_BATlow	Battery low voltage setting	R/W	010
		000:Lithium battery 2.80V*N/Lithium iron		
		battery 2.3V*N		
		001:Lithium battery 2.90V*N/Lithium iron		
		battery 2.4V*N		
		010:Li-ion Battery 3.00V*N/Li-Fe Battery 2.5V*N		
		011:Lithium Battery 3.10V*N/Lithium Iron		
		Battery 2.6V*N		
		100:Lithium battery 3.20V*N/Lithium iron		
		battery z.7v*N		
V1.61	http://www.injoinic.o	oM/Battery series <b>contac</b> Copyright	© 2022, Injo	inic Corp.
4:0	Reserved			

### **SYS\_CTL11** (output enable register)

# Description Document

I2C Address OXEA Register address = OxOB

Bit(s)	Name	Description	R/W	RESET
7	En_Dc-Dc_Output	Discharge output enable (no output when turned	R/W	1
		off)		
		1: Enabling		
		0: not enabled		
6	En_Vbus_Src_DP	C Port Output DP/DM Fast Charge Enable	R/W	1
	dM	1: Enable		
		0: disable		
5	En _Vbus_SrcPd	C Port Output Pd Fast Charge Enable	R/W	1
		1: Enable		
		0: disable	) 7	
4	En _Vbus_SrcSCP	C port output SCP fast charge enable	R/W	1
		1: Enable		
		0: disable		
3:0	Reserved			

# **SYS\_CTL12** (output maximum power selection register)

I2C Address OXEA Register address = 0x0C

Bit(s)	Name	Description	R/W	RESET
7:5	Vbus_Src_Power	Vbus1 Output power selection:	R/W	101
		000: 20W		
		001: 25W		
		010: 30W		
		011: 45W		
		100: 60W		
		101: 100W		
4:0	Reserved			

100W requires the addition of Emark recognition circuitry.

# TypeC\_CTL8 (TYPE-C mode control register)

Bit(s)	Name	Description	R/W	RESET
7:6	Vbus_Mode_Set	Vbus CC Mode Selection	R/W	0
		00: UFP		
		01: DFP		
		11: DRP		
5:0	Reserved			



# TypeC\_CTL9 (Output Pdo Current Setting Register) Description Document

Bit(s)	Name	Description	R/W	RESET
7	En_5VPdo_3A/2.4A	5VPdo Current Setting	R/W	1
		1: 3A		
		0: 2.4A		
6	En Pps2Pdo Iset	Pps2 Pdo Current Setting Enable	R/W	0
	' _	1: Enable 0:	,	
		disable		
		*The output power and overcurrent are based		
		on the set Pdo current after enabling, and the		
		overcurrent is based on the set Pdo current, and the overcurrent is based on the set Pdo current.		
			) >	
	5 0 40 1 1	Current is 1.1 times the set Pdo current.	5/14/	
5	En_Pps1Pdo_lset	Pps1 Pdo Current Setting Enable	R/W	0
		1: Enable 0: disable		
		*The output power and overcurrent are based		
		on the set Pdo current after enabling, and the		
		overcurrent is based on the set Pdo current, and		
		the overcurrent is based on the set Pdo current.		
		Current is 1.1 times the set Pdo current.		
4	En_20VPdo_Iset	20VPdo Current Setting Enable	R/W	0
		1: Enable 0:		
		disable		
		*The output power and overcurrent are based		
		on the set Pdo current after enabling, and the		
	·	overcurrent is based on the set Pdo current, and the overcurrent is based on the set Pdo current.		
		Current is 1.1 times the set Pdo current.		
3	En_15VPdo_Iset	15VPdo Current Setting Enable	R/W	0
3	EII_13VPdo_iset	1: Enable 0:	I IN/ VV	U
		disable o.		
		*The output power and overcurrent are based		
		on the set Pdo current after enabling, and the		
		overcurrent is based on the set Pdo current, and		
		the overcurrent is based on the set Pdo current.		
		Current is 1.1 times the set Pdo current.		
2	En_12VPdo_Iset	12VPdo Current Setting Enable	R/W	0
		1: Enable 0:		
		disable *The output power and overcurrent are based		
	_	on the set Pdo current after enabling, and the		
		overcurrent is based on the set Pdo current, and		
		the overcurrent is based on the set Pdo current.		
		Current is 1.1 times the set Pdo current.		
1	En_9VPdo_Iset	9VPdo Current Setting Enable	R/W	0
-	_= 33_330	1: Enable 0:	""	
		disable		
		*The output power and overcurrent are based		
		on the set Pdo current after enabling, and the		
		overcurrent is based on the set Pdo current, and		
		the overcurrent is based on the set Pdo current.		
1/400-1	F. FAID-WALL III III	Current is 1.1 times the set Pdo current.	@ 2033/ I*	inia Or
V1 <b>0</b> 61	En_snvupqowlsoftinjoinic.	8	© 2022/, Injo	inic wrp.
		1: Enable		
		0: disable		

#### TypeC\_CTL10 (5VPdo Current Setting Register)

# Description Document

I2C Address OXEA Register address = 0x24

Bit(s)	Name	Description	R/W	RESET
7:0	5VPdo_lset	5VPdo Current Setting	R/W	0x96
		5VPdo=20mA*N (Default 3A,Max=3A)		

#### TypeC\_CTL11 (9VPdo Current Setting Register)

I2C Address OXEA Register address = 0x25

Bit(s)	Name	Description	R/W	RESET
7:0	9VPdo_Iset	9VPdo Current Setting	R/W	0x96
		9VPdo=20mA*N (Default 3A,Max=3A)		

#### TypeC\_CTL12 (12VPdo Current Setting Register)

I2C Address OXEA Register address = 0x26

Bit(s)	Name	Description	R/W	RESET
7:0	12VPdo_lset	12VPdo Current Setting	R/W	0x96
		12VPdo=20mA*N (Default 3A,Max=3A)		

### TypeC\_CTL13 (15VPdo Current Setting Register)

I2C Address OXEA Register address = 0x27

Bit(s)	Name	Description	R/W	RESET
7:0	15VPdo_Iset	15VPdo Current Setting	R/W	0x96
		15VPdo=20mA*N (Default 3A,Max=3A)		

#### TypeC\_CTL14 (20VPdo Current Setting Register)

Bit(s)	Name	Description	R/W	RESET
7:0	20VPdo_lset	20VPdo Current Setting	R/W	0xFA
		20VPdo=20mA*N (Default 5A, need to recognize to		
		the		
		emark,Max=5A) did not recognize emark as 3A.		



# TypeC\_CTL23 (Pps1 Pdo Current Setting Register Document

I2C Address OXEA Register address = 0x29

Bit(s)	Name	Description	R/W	RESET
7:0	Pps1Pdo_Iset	Pps1 Pdo Current Setting	R/W	0x3C
		Pps1 Pdo=50mA*N (Default 5A, need to recognize		
		to the		
		emark,Max=5A) did not recognize emark as 3A.		

### TypeC\_CTL24 (Pps2 Pdo Current Setting Register)

I2C Address OXEA Register address = 0x2A

Bit(s)	Name	Description	R/W	RESET
7:0	Pps2Pdo_Iset	Pps2 Pdo Current Setting	R/W	0x3C
		Pps2 Pdo=50mA*N (Default 5A, need to recognize		
		to the		
		emark, Max=5A) did not recognize emark as 3A.		

### TypeC\_CTL17 (Output Pdo Setting Register)

Bit(s)	Name	Description	R/W	RESET
7	Reserved		R/W	R
6	En_Src_Pps2Pdo	Pps2 Pdo enable 1:	R/W	1
		Enable 0: disable		
		* No Pps2 Pdo after disable.		
5	En_Src_Pps1Pdo	Pps1 Pdo enable 1:	R/W	1
	4	Enable 0: disable		
		$*\overline{\mathrm{No}}$ Pps1 Pdo after disable.		
4	En_Src_20VPdo	20VPdo	R/W	1
		enable 1:	-	
	1 70	Enable 0:		
		disable		
		* No 20V Pdo after disable 15VPdo	- 6	_
3	En_Src_15VPdo	enable 1:	R/W	1
		Enable 0:		
	•	disable		
		* No 15V Pdo after disable		
2	En_Src_12VPdo	12VPdo	R/W	1
_	211_516_1211 46	enable 1:	'',''	
		Enable 0:		
		disable		
		* No 12V Pdo after disable		
1	En_Src_9VPdo	9VPdo enable	R/W	1
		1: Enable		
		0: disable		



		* No 9V Pdo after disable	Description	
0	Reserved		Document R/W	R





# 2.2 Read-only status indication register

#### Description Document

### **SOC\_CAP\_DATA** (cell charge data register)

I2C Address OXEA Register Address = 0X30

Bit(s)	Name	Description	R/W
7:0	Soc_Cap	Cell percentage charge data (%)	R
		Soc_Cap=N	

### STATE\_CTLO (Charge Status Control Register)

I2C Address OXEA Register address = 0X31

12C Address UXEA Register address = UX31			
Bit(s)	Name	Description	R/W
7:6	Reserved		R
5	CHG_En	Charge Flag Bit	R
		1: Charging status (VbusOk even if charging	
		status)	
		0: Non-charging state	
4	CHG_End	Filled Status Flag Bit	R
		1: Charging is full	
		0: Charge is not full	
3	Output_En	Discharge status flag bit	
		1: Discharge state and the output port has been	R
		opened without any abnormality	
		0: Discharge status output is not turned on or	
		there is discharge abnormality	
2:0	Chg_state	Chg_state	R
		000:	
		standby	
		001: Trickle	
		010: Constant current charging	
		011: Constant voltage charging	
		100: Charging pending (including cases where	
STATE_C	T <b>11</b> (Charge St	charging is not turned on, etc.) atus Control Register)	
		110: Charge timeout	

Bit(s)	Name	Description	R/W
7:6	Chg_State	Chg_state 00: 5V input charging 01: High voltage input fast charging	R
5:0	Reserved		R



# STATE\_CTL2 (Input Pd Status Control Register)

#### Description Document

I2C Address OXEA Register address = OX33

Bit(s)	Name	Description	R/W
7	Vbus_Ok	Vbus_Ok	R
		1: Vbus powered	
		0: Vbus no power	
6	Vbus_Ov	Vbus_Ov	R
		1: Vbus input overvoltage	
		0: No overvoltage on Vbus input	
5:3	Reserved		
2:0	Chg_Vbus	Charging Voltage	R
		111: 20V Charging	
		110: 15V charging	
		101: 12V Charging	
		100: 9V charging	
		011: 7V charging	
		010: 5V Charging	

### **TypeC\_STATE** (system status indication register)

Bit(s)	Name	Description	R/W
7	Sink_Ok	TypeC Sink Input Connection Flag Bit 1: Effective	R
		0: Invalid	
6	Src_Ok	TypeC Src Output Connection Flag Bit  1: Effective  0: Invalid	R
5	Src_Pd_Ok	Src_Pd_Ok Output connection flag bit 1: Effective 0: Invalid	R
4	Sink_Pd_Ok	Sink_Pd_Ok Input connection flag bit  1: Effective  0: Invalid	R
3	Vbus_Sink_Qc_Ok	Input fast charging valid flag bits Qc5V and Pd5V are not counted as fast charging Ok 1: Valid  0: Invalid	R
2	Vbus_Src_Qc_Ok	Output fast charging valid flag bits Qc5V and Pd5V are not counted as fast charging Ok 1: Valid 0: Invalid	R
1:0	Reserved		



# MOS\_STATE (input MOS status indication register) Description Document

I2C Address OXEA Register address = OX35

Bit(s)	Name	Description	R/W
7	Reserved		R
6	Vbus_Mos_State	Vbus port input MOS status 0: Closed 1: Open state	R
5:0	Reserved		R

# **STATE\_CTL3** (system overcurrent indication register)

I2C Address OXEA Register address = 0X38

Bit(s)       Name       Description       R/W         7:6       Reserved       R         5       Vsys_Oc       Vsys output overcurrent flag bit, need to be written 1 clear 0 1: Vsys output has triggered overcurrent signal overcurrent signal triggered at Vsys output When the first short-circuit signal is detected, write 1 to clear 0 and then read it again. If more than two consecutive overcurrent signals are detected within 600ms, it is recognized. Valid for overcurrent signal         4       Vsys_Scdt       Vsys output short-circuit flag bit, need to write 1 to clear 0 1: Vsys output has triggered at Vsys output short-circuit signal triggered at Vsys output When the first short-circuit signal is detected, write 1 to clear 0 in the first short-circuit signal is detected, write 1 to clear 0 in the first short-circuit signal is detected, write 1 to clear 0 in the first short-circuit signal is detected, write 1 to clear 0 in the first short-circuit signal is detected, write 1 to clear 0 in the first short-circuit signal is detected, write 1 to clear 0 in the first short-circuit signal is detected, write 1 to clear 0 in the first short-circuit signal is detected, write 1 to clear 0 in the first short-circuit signal is detected, write 1 to clear 0 in the first short-circuit signal is detected, write 1 to clear 0 in the first short-circuit signal is detected, write 1 to clear 0 in the first short-circuit signal is detected, write 1 to clear 0 in the first short-circuit signal is detected, write 1 to clear 0 in the first short-circuit signal is detected, write 1 to clear 0 in the first short-circuit signal is detected, write 1 to clear 0 in the first short-circuit signal is detected, write 1 to clear 0 in the first short-circuit signal is detected, write 1 to clear 0 in the first short-circuit signal is detected, write 1 to clear 0	12C Addres	S UXEA REGIS	ter address = UX38	
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7:0 BATVADC[7:0] BATVADC Low 8bit of data R	12C Addres	s OXEA Register		
2·0   Poconyod · · ·     P	Bit(s)	Name		R/W
Voltage of VBATPIN	<del>7:8</del>	BATVADC[7:0]	BATVADE Low 8bit of data	R
	3.0	Neserveu	Voltage of VBATPIN	n.

### BATVADC\_DAT1 (VBAT voltage register)

Bit(s)	Name	Description	R/W
7:0	BATVADC[15:8]	BATVADC High 8bit of data	R



Voltage of VBATPIN	Description
VBAT=BATVADC (mV)	Document

#### **VsysVADC\_DAT0** (**Vsys** voltage register)

I2C Address OXEA Register Address = 0X52

Bit(s)	Name	Description	R/W
7:0	VsysVADC[7:0]	Vsys Low 8bit of voltage data	R
		Voltage at VsysPIN	

#### VsysVADC\_DAT1 (Vsys voltage register)

Send I2C address OXEA Register address = OX53

Bit(s)	Name	Description	R/W
7:0	VsysVADC[15:8]	Vsys Voltage data of high 8bit VsysPIN voltage Vsys= VsysVADC (mV)	R

#### IVbus\_Sink\_IADC\_DAT0 (input current register)

I2C Address OXEA Register Address = OX54

Bit(s)	Name	Description	R/W
7:0	IVbus ADC[7:0]	Low 8bit of charge input current data	R
		Current at Vbus input	

#### IVbus\_Sink\_IADC\_DAT1 (input current register)

Send I2C address OXEA Register address = OX55

Bit(s)	Name	Description	R/W
7:0	IVbusADC[15:8]	High 8bit of charge input	R
		current data Current at	
		Vbus input lin=IVbusADC	
When char	ging, the current is	s (to A) $ m d$ in 0X54 and 0x55. 0x31 $ m register$ bit5 is the charge flag $ m d$	oit.

# ${\bf IVbus\_Src\_IADC\_DATO}\ (output\ current\ register)$

Bit(s)	Name	Description	R/W
7:0	IVbus ADC[7:0]	Lower 8 bits of discharge output current data	R



Current at Vbus output Description

#### **Document**

#### IVbus\_Src\_IADC\_DAT1 (output current register)

Send I2C address OXEA Register address = OX57

Bit(s)	Name	Description	R/W
7:0	IVbusADC[15:8]	Discharge output	R
		current data of the high	
		8bit Vbus output current	
When disch	arging, the currer	ntl <b>outHVbdsADC(mA)</b> d 0x57. 0x31 register bit5 is the discharge	flag bit.

#### **IBATIADC\_DATO** (**BAT** side current register)

I2C Address OXEA Register Address = 0x6E

Bit(s)	Name	Description	R/W
7:0	IBATIADC[7:0]	Cell end current IBATIADC data low 8bit	R

#### **IBATIADC\_DAT1** (BAT side current register)

I2C Address OXEA Register Address = 0x6F

Bit(s)	Name	Description	R/W
7:0	IBATIADC[15:8]	Cell end current High 8bit of BATIADC data IBAT=IBATIADC(mA)	R

#### ISYS\_IADC\_DATO (IVsys side current register)

I2C Address OXEA Register Address = 0x70

	- 6		
Bit(s)	Name	Description	R/W
7:0	ISYSIADC[7:0]	IVsys end current VsysIADC data low 8bit	R

### IVsys\_IADC\_DAT1 (IVsys side current register)

120 11441 6	12e Hadress With Register Hadress W/1				
Bit(s)	Name	Description	R/W		
7:0	IVsysIADC[15:8]	IVsys end current VsysIADC data high 8bit IVsys = VsysIADC(mA)	R		

#### Vsys\_POW\_DATO (Vsys side power register)

# Description Document

I2C Address OXEA Register Address = 0X74

Bit(s)	Name	Description	R/W
7:0	Vsys_POW_ADC [7:0]	Lower 8 bits of Vsys-side power ADC data	R

#### Vsys\_POW \_DAT1 (Vsys side power register)

I2C Address OXEA Register Address = 0X75

Bit(s)	Name	Description	R/W
7:0	Vsys_POW_ADC[1 5:8]	Vsys-side power ADC data, medium 8bit	R

# Vsys\_POW \_DAT2 (Vsys side power register)

I2C Address OXEA Register Address = 0X76

Bit(s)	Name	Description	R/W
7:0	Vsys_POW_ADC[2 3:16]	High 8bit of Vsys end power ADC data Vsys_POW= Vsys_POW_ADC(mW)	R

#### INTC\_IADC \_DATO (NTC output current register)

I2C Address OXEA Register Address = 0X77

Bit(s)	Name	Description	R/W
7	NTC_IADC_DAT	0:Output 20uA	R
		1:Output 80uA	
6:0	Reserved		

#### **VGPIOO\_NTC\_DATO** (**VGPIOO\_NTC\_ADC** voltage register)

I2C Address OXEA Register Address = 0X78

Bit(s)	Name	Description	R/W
7:0	VGPIO0_DAT0 [7:0]	Low 8bit of VGPIO0_ADC data	R

### **VGPIOO\_NTC\_DAT1** (**VGPIOO\_NTC\_ADC** voltage register)

Bit(s)	Name	Description	R/W



7:0	vgpio0_dat1	High 8bit of VGPIO0_ADC data	Description	R
	[15:8]	VGPIO0_DAT= VGPIO0_ADC (mV) (0~	3.3V) Document	

#### **VGPIO1\_Iset\_DAT0** (**VGPIO1\_Iset\_ADC** voltage register)

I2C Address OXEA Register Address = OX7A

Bit(s)	Name	Description	R/W
7:0	VGPIO1_DAT0 [7:0]	Low 8bit of VGPIO1_ADC data	R

#### VGPIO1\_Iset\_DAT1 (VGPIO1\_Iset\_ADC voltage register)

I2C Address OXEA Register Address = OX7B

Bit(s)	Name	Description	R/W
7:0	vgpio1_dat1	High 8bit of VGPIO1_ADC data	R
	[15:8]	VGPIO1_DAT= VGPIO1_ADC (mV) (0~3.3V)	

#### VGPIO2\_Vset\_DAT0 (VGPIO2\_Vset\_ADC voltage register)

I2C Address OXEA Register Address = OX7C

Bit(s)	Name	Description	R/W
7:0	VGPIO2_DAT0 [7:0]	Low 8bit of VGPIO2_ADC data	R

#### VGPIO2\_Vset\_DAT1 (VGPIO2\_Vset\_ADC voltage register)

I2C Address OXEA Register Address = OX7D

Bit(s)	Name	Description	R/W
7:0	vgpio2_dat1	High 8bit of VGPIO2_ADC data	R
	[15:8]	VGPIO2_DAT= VGPIO2_ADC (mV) (0~3.3V)	

#### **VGPIO3\_FCAP\_DAT0** (**VGPIO3\_FCAP\_ADC** voltage register)

I2C Address OXEA Register Address = OX7E

Bit(s)	Name	Description	R/W
7:0	VGPIO3_DAT0 [7:0]	Low 8bit of VGPIO3_ADC data	R



# VGPIO3\_FCAP\_DAT1 (VGPIO3\_FCAP\_ADC voltage register) Description Document

#### I2C Address OXEA Register Address = OX7F

Bit(s)	Name	Description	R/W
7:0	v gpio3_dat1	High 8bit of VGPIO3_ADC data	R
	[15:8]	VGPIO3_DAT= VGPIO3_ADC (mV) (0~3.3V)	

#### VGPIO4\_BATNUM\_DATO (VGPIO4\_BATNUM\_ADC voltage register)

#### I2C Address OXEA Register Address = 0X80

Bit(s)	Name	Description	_	R/W
7:0	VGPIO4_DAT0 [7:0]	Low 8bit of VGPIO4_ADC data	7	R

#### VGPIO4\_BATNUM\_DAT1 (VGPIO4\_BATNUM\_ADC voltage register)

Bit(s)	Name	Description	R/W
7:0	v gpio4_dat1	High 8bit of VGPIO4_ADC data	R
	[15:8]	VGPIO3_DAT= VGPIO3_ADC (mV) (0~3.3V)	



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