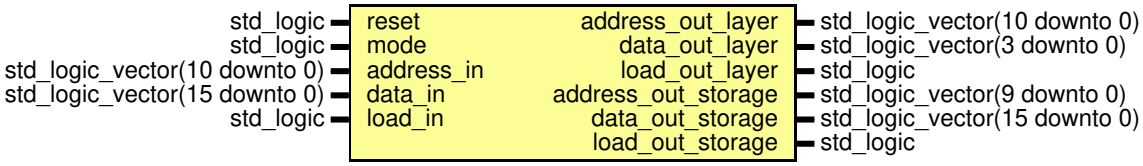
Top Level Resolver

- **File:** top_level_resolver.vhdl
- **Author:** Fabian Franz (fabian.franz0596@gmail.com)
- **Version:** 0.1
- **Date:** 06.2021

Diagram



Description

This module implement the data and address handling switch between the layer modules and the storage module.

Generics and ports

Table 1.1 Generics

Table 1.2 Ports

Port name	Direction	Type	Description
reset	in	std_logic	global reset
mode	in	std_logic	select the direction
address_in	in	std_logic_vector(10 downto 0)	the address of data storage
data_in	in	std_logic_vector(15 downto 0)	the actual data to store
load_in	in	std_logic	triggers the storage
address_out_layer	out	std_logic_vector(10 downto 0)	address casting, mode='1'
data_out_layer	out	std_logic_vector(3 downto 0)	data forwarding
load_out_layer	out	std_logic	triggers storage
address_out_storage	out	std_logic_vector(9 downto 0)	address casting, mode='0'
data_out_storage	out	std_logic_vector(15 downto 0)	data forwarding
load_out_storage	out	std_logic	triggers storage

Processes

- **behaviour**: ***(reset, mode, address_in, data_in, load_in)***