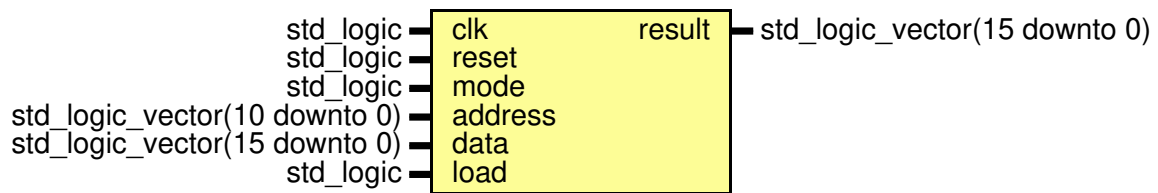


Top Level Entity

- **File:** top_level_entity.vhdl
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- **Version:** 0.1
- **Date:** 14.06.2021

Diagram



Description

This module has the purpose to put all modules of the perceptron project together.

Generics and ports

Table 1.1 Generics

Table 1.2 Ports

Port name	Direction	Type	Description
clk	in	std_logic	global clock signal
reset	in	std_logic	global reset signal
mode	in	std_logic	select the direction '0' = layer, '1' = storage
address	in	std_logic_vector(10 downto 0)	the address of data storage in the layer or storage branch
data	in	std_logic_vector(15 downto 0)	the actual data to store
load	in	std_logic	triggers the storage
result	out	std_logic_vector(15 downto 0)	the result from the last layer

Signals, constants and types

Signals

Name	Type	Description
address_int_layer	std_logic_vector(10 downto 0)	connect adress line of "Top Level Resolver" and "Layer Resolver"
data_int_layer	std_logic_vector(3 downto 0)	connect data line of "Top Level Resolver" and "Layer Resolver"
load_int_layer	std_logic	connect load line of "Top Level Resolver" and "Layer Resolver"
address_int_storage	std_logic_vector(9 downto 0)	connect address line of "Top Level Resolver" and "Storage"
data_int_storage	std_logic_vector(15 downto 0)	connect data line of "Top Level Resolver" and "Storage"
load_int_storage	std_logic	connect load line of "Top Level Resolver" and "Storage"
storage_to_first_layer	std_logic_vector(15 downto 0)	connect the storage output with the first layer

layer_axon_arr	arr_16_times_16	connect axon ports between layer and layer resolver
address_layer_arr	arr_16_times_7	connect address ports between layer and layer resolver
data_layer_arr	arr_16_times_4	connect data ports between layer and layer resolver
load_layer	std_logic_vector (15 downto 0)	connect load signal between layer and layer resolver

Types

Name	Type	Description
arr_16_times_16		
arr_16_times_7		
arr_16_times_4		

Instantiations

- **tlr_inst**: top_level_resolver
- **storage_inst**: storage