layer_resolver

- **File:** pereptron.vhdl
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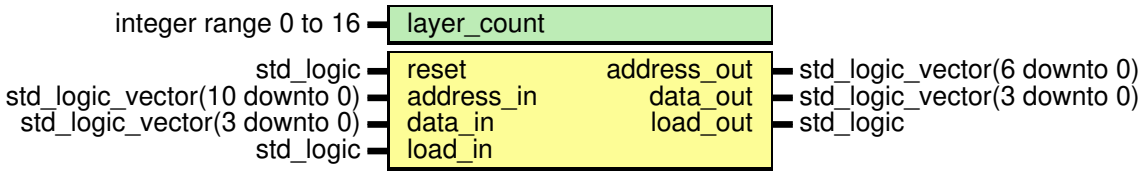
Diagram



Description

This module is designed for resolving the signals in every
single layer of the multilayer perceptron.
The address resolving is based on the "layer_count" variable, which
determine the number of every single layer in the whole multilayer perceptron.
Based on this number, the address is forwarded by a 7-Bit bus to the
single perceptrons in the layer.

Generics and ports

Table 1.1 Generics

Generic name	Type	Value	Description
layer_count	integer range 0 to 16		identifier for the current layer

Table 1.2 Ports

Port name	Direction	Type	Description
reset	in	std_logic	reset to default output values
address_in	in	std_logic_vector(10 downto 0)	input address from "Top Level Resolver"
data_in	in	std_logic_vector(3 downto 0)	input data from "Top Level resolver"
load_in	in	std_logic	load input from "Top Level Resolver"
address_out	out	std_logic_vector(6 downto 0)	addressing the sensitivity and activation value in the "Perceptron"
data_out	out	std_logic_vector(3 downto 0)	the actual value for sensitivity and activation in the "Perceptron"
load_out	out	std_logic	triggers the storage in the "Perceptron"

Processes

- **behaviour**: ***(address_in, reset, load_in, data_in)***