Perceptron

- **File:** pereptron.vhdl
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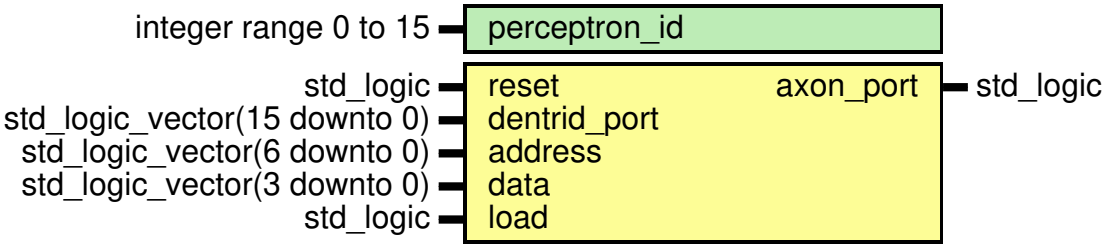
Diagram



Description

This module describes the actual behaviour of the combinatorical perceptron. The perceptron is capable of holding the values for input sensitivity and the output activation.

Generics and ports

Table 1.1 Generics

Generic name	Type	Value	Description
perceptron_id	integer range 0 to 15		the ID of the perceptron in the specific layer

Table 1.2 Ports

Port name	Direction	Type	Description
reset	in	std_logic	reset inputs and outputs of the entity to default values
dentrid_port	in	std_logic_vector(15 downto 0)	input from previous layer
axon_port	out	std_logic	output to next layer
address	in	std_logic_vector(6 downto 0)	current address for parameter manipulation
data	in	std_logic_vector(3 downto 0)	value of the addressed parameter
load	in	std_logic	signal to actually store the addressed parameter value

Signals, constants and types

Signals

Name	Type	Description
activation_value	unsigned (3 downto 0)	threshold parameter for input count until output is set to one
sensitivity_value	unsigned (15 downto 0)	determine whis inputs are activated and counted.
sens_1	unsigned (3 downto 0)	

sens_2	unsigned (7 downto 4)	
sens_3	unsigned (11 downto 8)	
sens_4	unsigned (15 downto 12)	

Processes

- **behaviour**: ***(load, reset, dentrid_port, address, data)***