Perceptron Storage

- **File:** storage.vhdl
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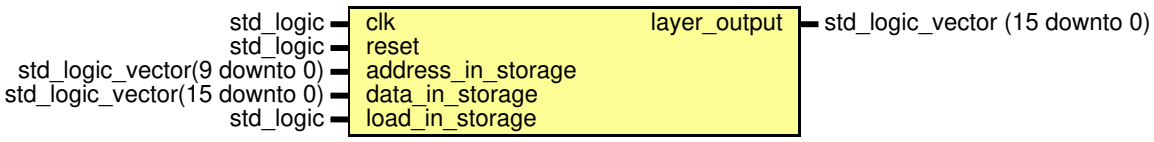
Diagram



Description

This module implement the storage of 1024 16Bit Values and output them on each clock iteration.

Generics and ports

Table 1.1 Generics

Table 1.2 Ports

Port name	Direction	Type	Description
clk	in	std_logic	clock for iteration over storage values
reset	in	std_logic	reset to set default values
address_in_storage	in	std_logic_vector(9 downto 0)	address where tha value have to be stored
data_in_storage	in	std_logic_vector(15 downto 0)	actual data which have to be stored
load_in_storage	in	std_logic	trigger the storage
layer_output	out	std_logic_vector (15 downto 0)	output to the first layer

Signals, constants and types

Signals

Name	Type	Description
stored_value	arr_1024_times_16	

Types

Name	Type	Description
arr_1024_times_16		the one dimensional array of stored values

Processes

- **behaviour**: ***(load_in_storage, clk, reset)***