The 8255 Programmable Peripheral Interface (PPI)

Intel Peripheral Controller Chips

- Intel has developed several peripheral controller chips designed to support the 80x86 processor family such as:
  - the 8255A Programmable Peripheral Interface (PPI),
  - the 8259 Programmable Interrupt Controller (PIC),
  - the 8253/54 Programmable Interval Timer (PIT), and
  - the 8237 Programmable DMA Controller.
- The objective is to provide a complete I/O interface in one chip.

Basic Description of the 8255

- The 8255 is a general-purpose parallel I/O interfacing device designed for use in Intel microcomputer systems.
- Its function is to interface peripheral equipment to the microcomputer data bus.
- The functional configuration of the 8255 is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Basic Description of the 8255

- The 8255 provides **24 I/O lines** which may be individually programmed in **2 groups** of 12 I/O lines and used in **3** major **modes of operation**.
- These 24 I/O lines organized as **three 8-bit I/O ports** labeled **A**, **B**, and **C**.
- The chip interfaces directly to the data bus of the processor, allowing its function to be programmed;
- That is, in one application a port may appear as an output, but in another, by reprogramming it, as an input.

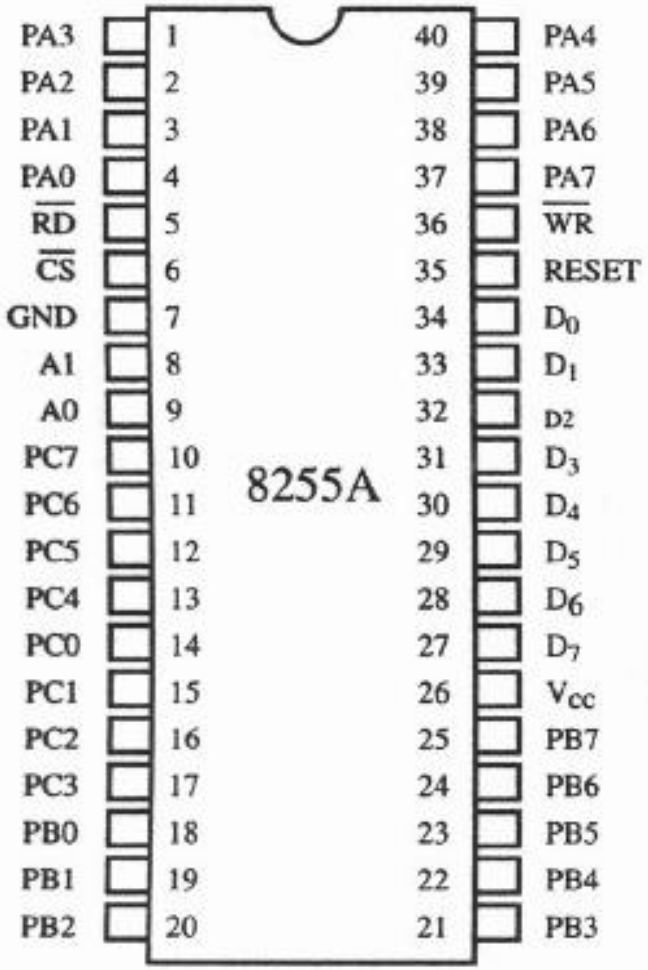
Basic Description of the 8255

- Each of the ports, **A** or **B**, can be programmed as an **8-bit input** or **output** port.
- Port **C** can be **divided in half**, with the topmost or bottommmost four bits programmed as inputs or outputs.
- Individual bits of a particular port cannot be programmed.

Pin Configuration of the 8255

- The pin configuration of the 8255 is shown in Figure 1.
  - **GND**: System ground
  - **VCC**: System power
  - **RESET**: A high on this input clears the control register and all ports are set to the input mode.
  - **PA_{7-0}**: Port A bits
  - **PB_{7-0}**: Port B bits
  - **PC_{7-0}**: Port C bits
  - **D_{7-0}**: A bi-directional, tri-state data bus lines, connected to the system data bus.
  - **RD'**: A read input control, that is low during CPU read operations.
  - **WR'**: A write input control, that is low during CPU write operations.
  - **CS'**: A chip select control. A low on this input enables the 8255 to respond to RD' and WR' signals. RD' and WR' are ignored otherwise.
  - **A_{1-0}**: Address lines which in conjunction with RD' and WR', control the selection of one of the three ports or the control word registers as shown in Table 1.

Pin Configuration



Pin Names

D_7–D_0	Data Bus (Bidirectional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A0, A1	Port Address
PA7–PA0	Port A (bit)
PB7–PB0	Port B (bit)
PC7–PC0	Port C (bit)
V_{CC}	+5V
GND	0V

Figure 1: Pin configuration of the 8255

Table 1: Selection of 8255 ports using address lines.

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
					Input operation (READ)
0	0	0	1	0	Port A → data bus
0	1	0	1	0	Port B → data bus
1	0	0	1	0	Port C → data bus
					Output operation (WRITE)
0	0	1	0	0	Data bus → port A
0	1	1	0	0	Data bus → port B
1	0	1	0	0	Data bus → port C
1	1	1	0	0	Data bus → control
					Disable function
X	X	X	X	1	Data bus tristate
1	1	0	1	0	Illegal condition
X	X	1	1	0	Data bus tristate

Block Diagram of the 8255

- The block diagram of the 8255 is shown in Figure 2.
- Data Bus Buffer:
  - This **3-state bidirectional 8-bit buffer** is used to interface the 8255 to the system data bus.
  - Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU.
  - Control words and status information are also transferred through the data bus buffer.
- Read/Write and Control Logic:
  - The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words.
  - It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

Block Diagram of the 8255

- Group A and Group B Controls:
  - The functional configuration of each port is programmed by the **systems software**.
  - The CPU **outputs** a **control word** to the 8255.
  - The **control word** contains information such as **mode**, **bit set**, **bit reset**, etc., that initializes the functional configuration of the 82C55A.
  - Each of the Control blocks (**Group A** and **Group B**) accepts **commands** from the read/write control logic, receives **control words** from the internal data bus and issues the proper commands to its associated ports.
    - Control **Group A** - Port A and Port C upper (C_7-C_4)
    - Control **Group B** - Port B and Port C lower (C_3-C_0)
  - The control word register can be both **written** and **read** as shown in Table 1.

Block Diagram of the 8255

- Ports A, B, and C:
  - The 8255 contains **three 8-bit ports** (**A**, **B**, and **C**).
  - All can be configured in a wide variety of functional characteristics by the system software.

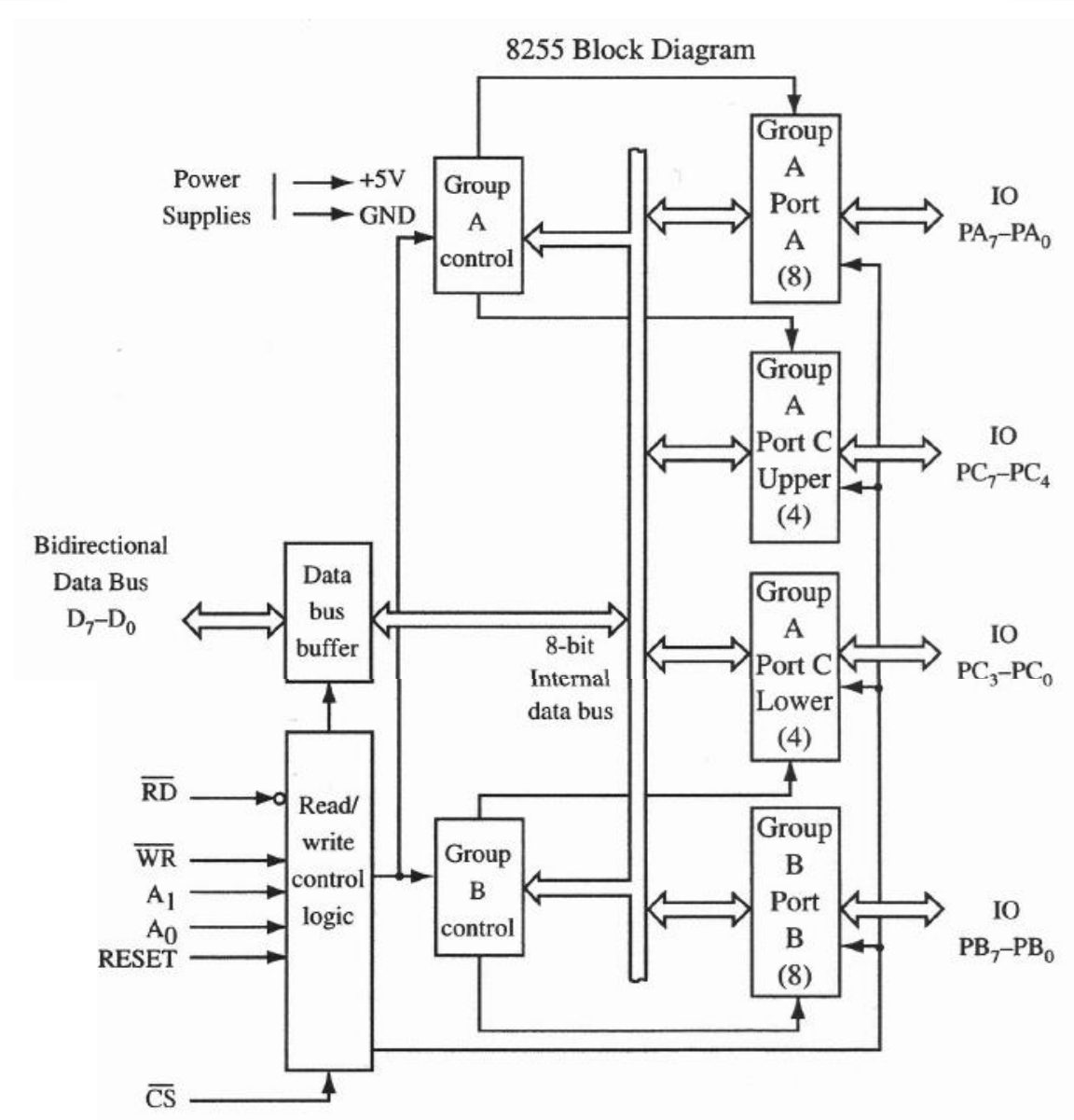


Figure 2: Block diagram of the 8255

Interfacing the 8255 to the 8086 Processor

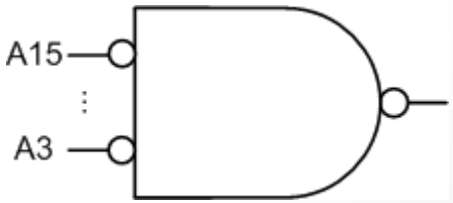
- **Example 1:**Show how to interface an 8255 chip to the low byte of the 8086 (D0-D7). Assume the following I/O address ports are used.

Step (1): Design the address decoding

A_{15}-A_{12}	A_{11}-A_8	A_7-A_4	A_3	A_2	A_1	A_0
0000	0000	0000	0	0	0	0
0000	0000	0000	0	0	1	0
0000	0000	0000	0	1	0	0
0000	0000	0000	0	1	1	0
Chip Select (CS')				Port Select (A_1 A_0)		Enable Even Byte (D0-D7)

Port Name	**Port Address**
Port A	00H
Port B	02H
Port C	04H
Control	06H

Step(2): Design control logic (IOW' & IOR')



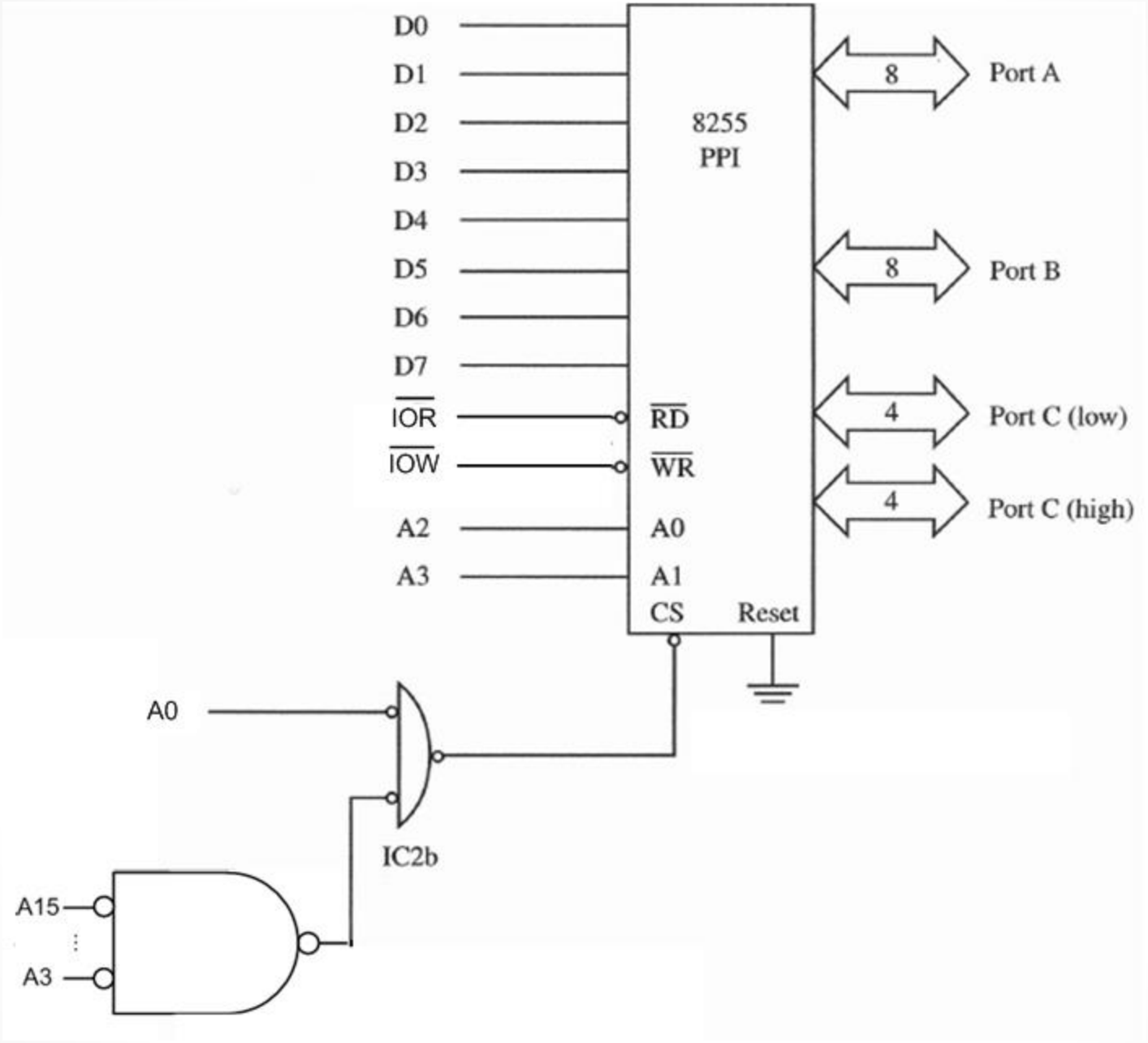


Figure 3: Interface of the 8255 in Example 1

Programming the 8255

- There are three basic modes of operation that can be selected by the system software:
  - **Mode 0:** Basic input/output
  - **Mode 1:** Strobed Input/output
  - **Mode 2:** Bi-directional Bus

Programming the 8255

- When the reset input of the 8255 goes "high" all ports will be set to the input mode with all 24 port lines held at a logic "one" level.
- After the reset is removed the 8255 can remain in the input mode with no additional initialization required.
- During the execution of the system program, any of the other modes may be selected by using a single output instruction.
- The modes for Port A and Port B can be separately defined, while Port C is divided into two portions.

Programming the 8255

- Figure 4 shows the format of the control byte used to program the 8255.
- There are two types of control bytes:
  - (a) When **bit 7 = 0**, a bit set/reset operation is indicated;
  - (b) When **bit 7 = 1**, any of the modes 0, 1, or 2 can be programmed.
- The ports in Group A can be programmed for any of modes 0, 1, or 2.
- The ports in Group B can only be programmed for modes 0 or 1.

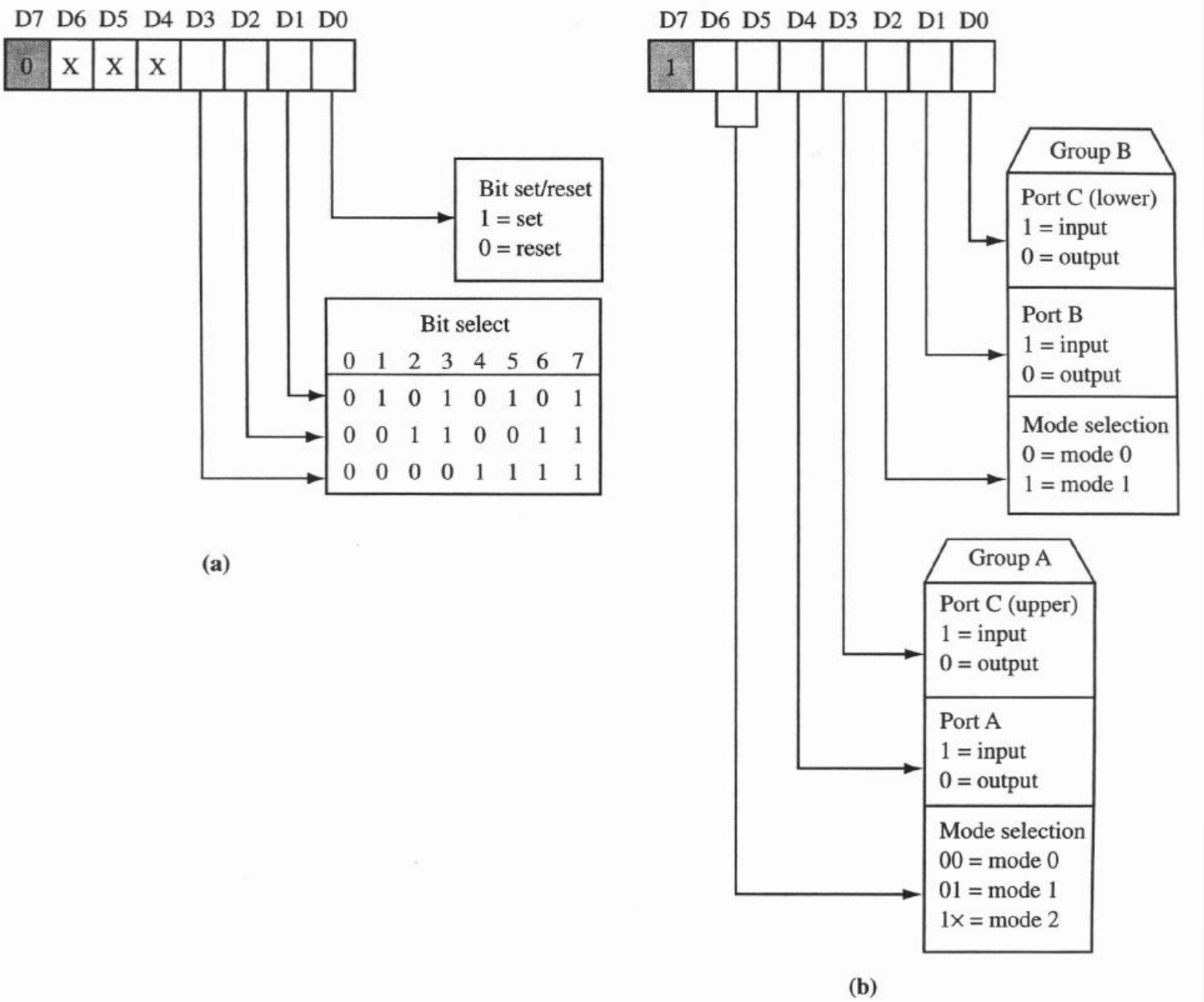


Figure 4: The format of the control byte of the 8255.

Programming the 8255

- **Example 2:** Write the 80x86 initialization routine required to program the 8255 in Figure 5 for mode 0, with port A as an output and ports B and C inputs
  - The control word is formed as:
    - 1 00 0 1 0 1 1 = 8BH
  - The program is as follows:
    - MOV AL,8BH ;Control byte to AL
    - OUT 6,AL ;Write to control port

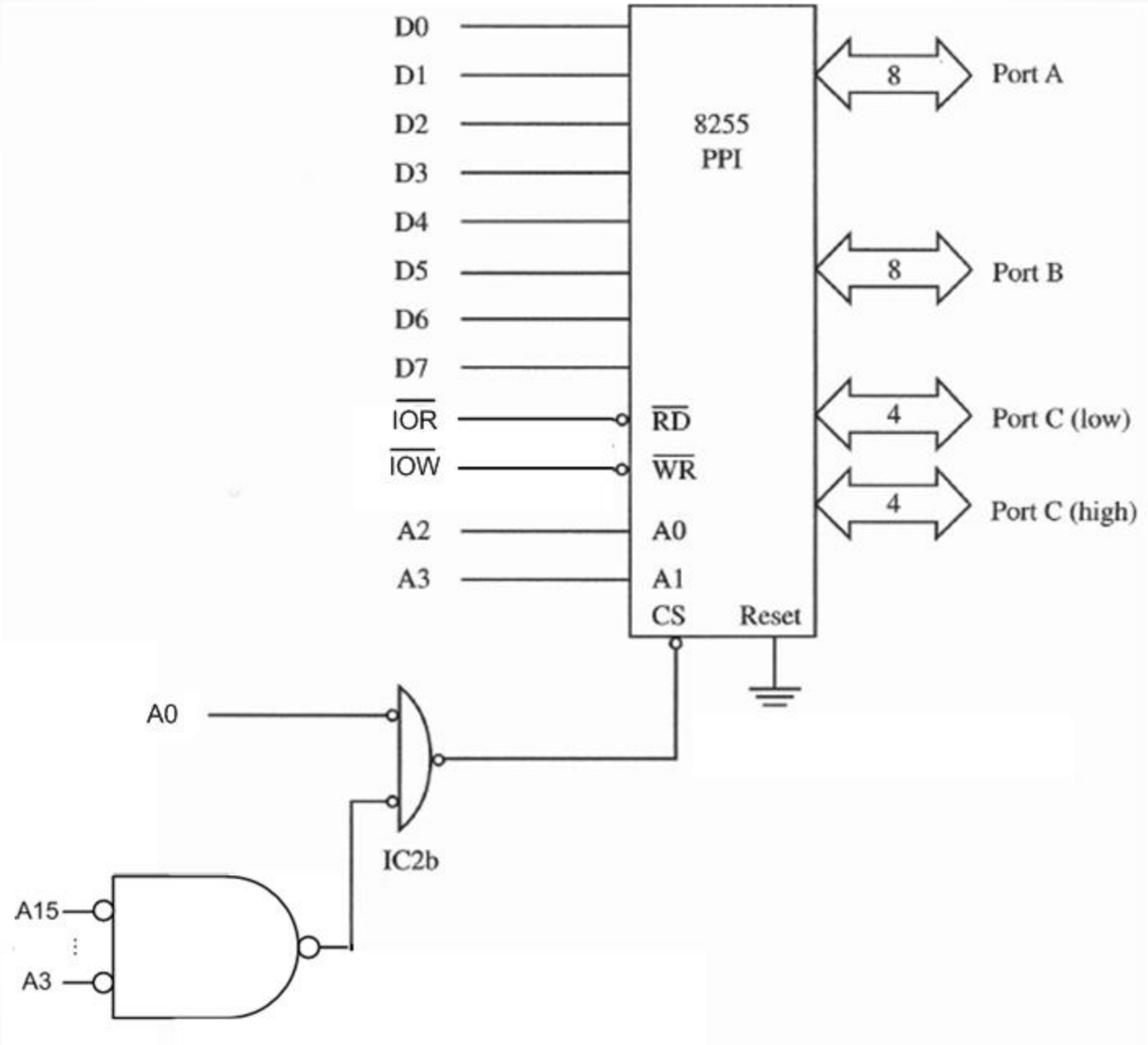


Figure 5: Circuit design of Example 2.

Programming the 8255

- **Example 3:** Write an 80x86 program to input a byte from port B of the PPI chip in pervious example and output this byte to port A of the same chip. Assume the chip has been programmed as in the previous example.

  - The program requires two instructions.
    - IN AL, 2 ; Get data from port B
    - OUT 0,AL ; Output the data to port A

Operating Modes of the 8255

- The 8255A can be programmed in three modes (0, 1, 2) as shown in Figure 6:
  - **Mode 0 (Basic I/O):** three simple I/O ports.
    - Ports A and B operate as either inputs or outputs.
    - Port C is divided into two 4-bit groups either of which can be operated as inputs or outputs.
  - **Mode 1 (Strobed I/O):** two hand shaking I/O ports.
    - Ports A and B operate as either inputs or outputs as in mode 0
    - Port C is used for handshaking and control.
  - **Mode 2 (Strobed Bidirectional I/O):** a bidirectional I/O port with five hand shaking signals.
    - Port A is bidirectional (both input and output).
    - Port C is used for handshaking.
    - Port B is not used.
- These modes can also be intermixed. For example, port A can be programmed to operate in mode 2, while port B operates in mode 0.

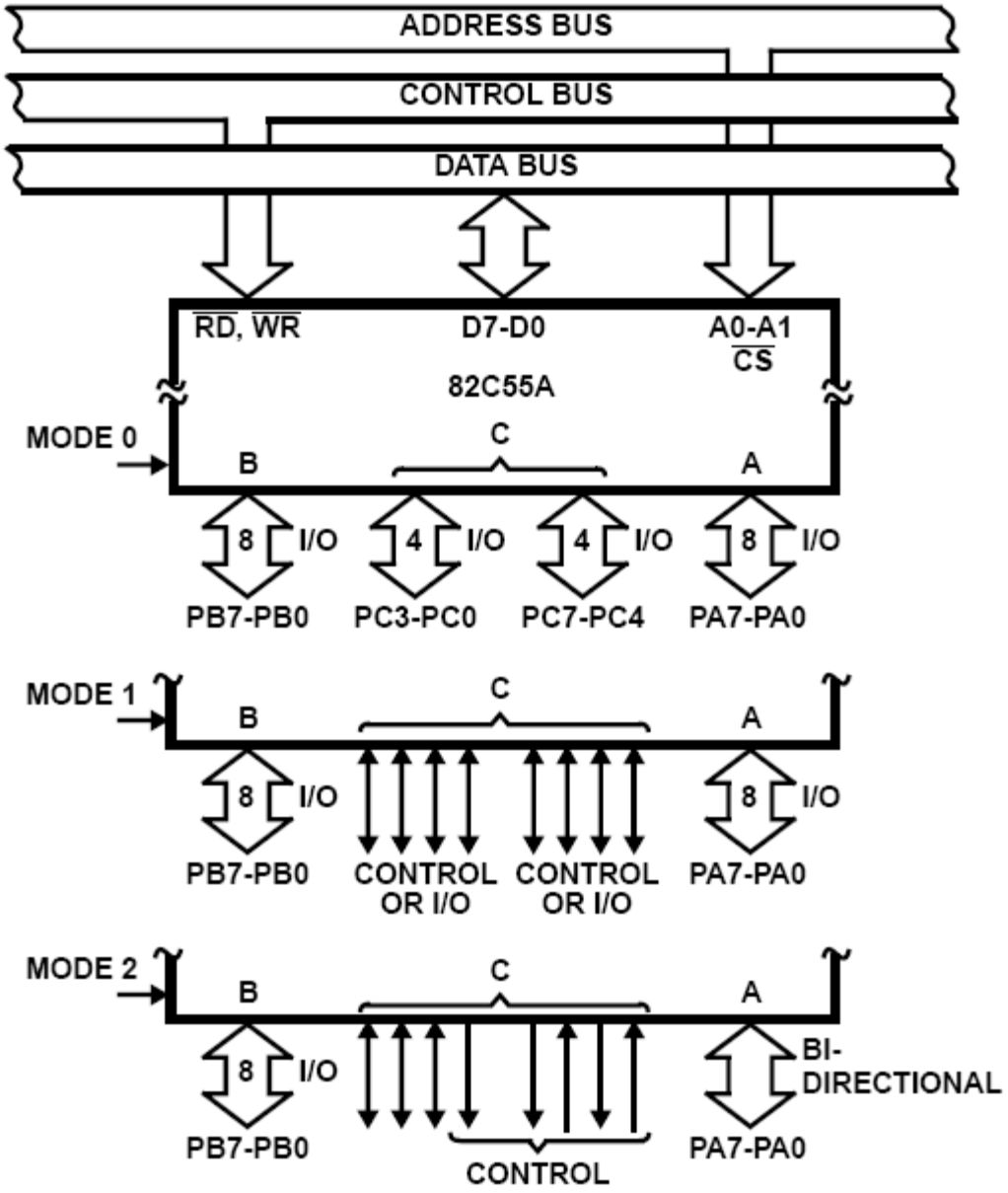


Figure 6: The three basic modes of the 8255.

Operating Modes of the 8255

Mode 0 (Basic Input / Output)

- This mode provides simple input and output operations for each of the three ports.
- No handshaking is required, data is simply written to or read from a specific port.
- The basic features of this mode are:
  - Two 8-bit ports and two 4-bit ports
  - Any Port can be input or output
  - Outputs are latched
  - Input are not latched
  - 16 different input / output configurations possible as shown in Table 2.

Table 2: Mode 0 port definition.

A		B		GROUP A			GROUP B	
D4	D3	D1	D0	PORT A	PORT C (Upper)	#	PORT B	PORT C (Lower)
0	0	0	0	Output	Output	0	Output	Output
0	0	0	1	Output	Output	1	Output	Input
0	0	1	0	Output	Output	2	Input	Output
0	0	1	1	Output	Output	3	Input	Input
0	1	0	0	Output	Input	4	Output	Output
0	1	0	1	Output	Input	5	Output	Input
0	1	1	0	Output	Input	6	Input	Output
0	1	1	1	Output	Input	7	Input	Input
1	0	0	0	Input	Output	8	Output	Output
1	0	0	1	Input	Output	9	Output	Input
1	0	1	0	Input	Output	10	Input	Output
1	0	1	1	Input	Output	11	Input	Input
1	1	0	0	Input	Input	12	Output	Output
1	1	0	1	Input	Input	13	Output	Input
1	1	1	0	Input	Input	14	Input	Output
1	1	1	1	Input	Input	15	Input	Input

Operating Modes of the 8255

Mode 1 (Strobed Input / Output)

- This mode provides a means for transferring I/O data to or from a specified port in conjunction with strobes or “hand shaking” signals.
- In this mode, port A and port B use the lines on port C to generate or accept these “hand shaking” signals.
- The basic features of this mode are:
  - Two Groups (Group A and Group B).
  - Each group contains one 8-bit port and one 4-bit control/data port.
  - The 8-bit data port can be either input or output.
  - Both inputs and outputs are latched.
  - The 4-bit port is used for control and status of the 8-bit port.

Operating Modes of the 8255

Mode 1 (Strobed Input / Output)

- Figure 7 shows the control signals for input configuration.
- **STB (Strobe Input)**
  - A “low” on this input loads data into the input latch.
- **IBF (Input Buffer Full F/F)**
  - A “high” on this output indicates that the data has been loaded into the input latch.
  - IBF is set by STB’ input being low and is reset by the rising edge of the RD’ input.
- **INTR (Interrupt Request)**
  - A “high” on this output can be used to interrupt the CPU when and input device is requesting service.
  - INTR is set by the condition: STB is a “one”, IBF is a “one” and INTE is a “one”.
  - It is reset by the falling edge of RD.
  - This procedure allows an input device to request service from the CPU by simply strobing its data into the port.
- **INTE A:** Controlled by bit set/reset of PC4.
- **INTE B:** Controlled by bit set/reset of PC2.

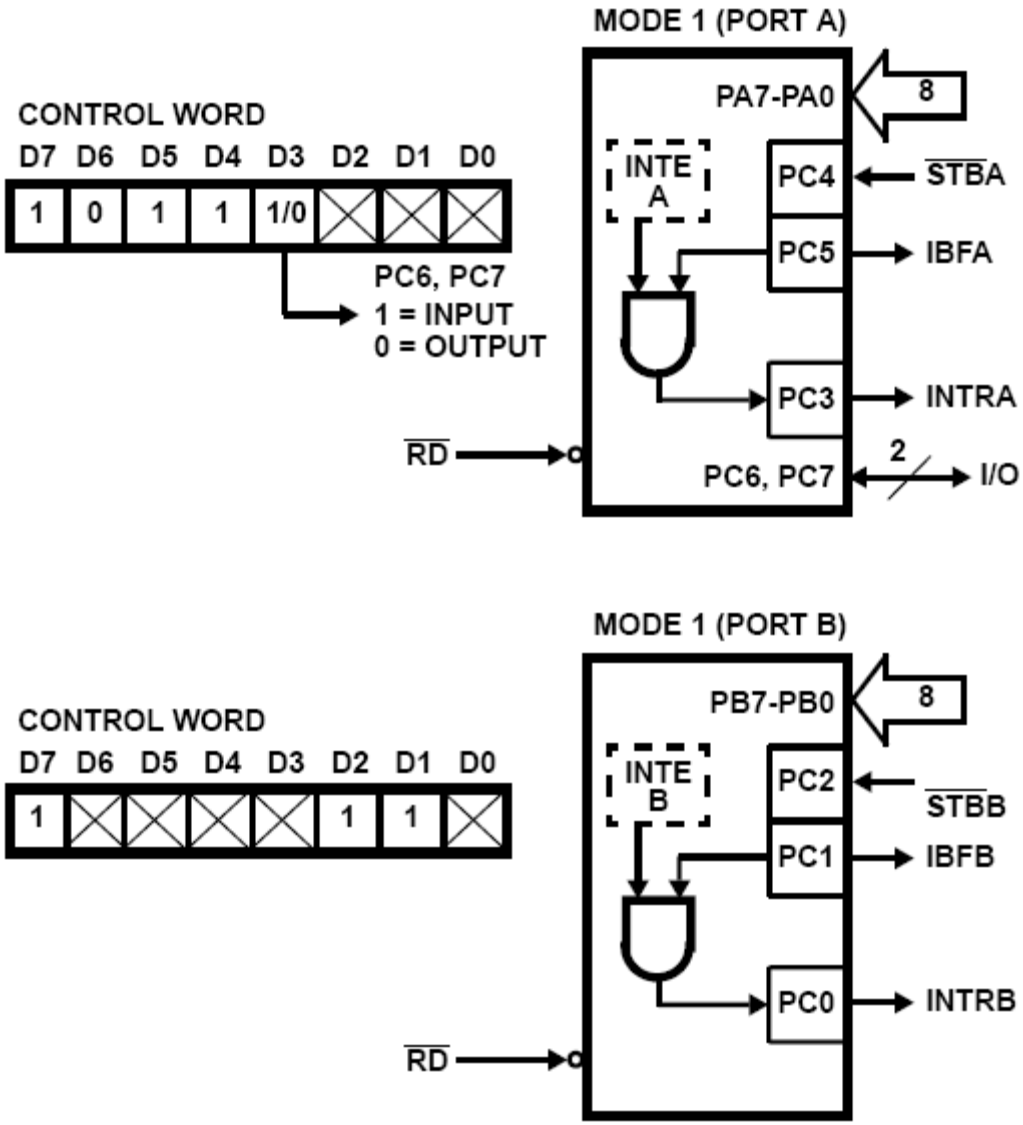


Figure 7: Mode 1 input.

Operating Modes of the 8255

Mode 1 (Strobed Input / Output)

- Figure 8 shows the control signals for output configuration.
- **OBF - Output Buffer Full F/F:**
  - The OBF' output will go "low" to indicate that the CPU has written data out to be specified port.
  - The OBF' F/F will be set by the rising edge of the WR input and reset by ACK input being low.
- **ACK - Acknowledge Input):**
  - A "low" on this input informs the 82C55A that the data from Port A or Port B is ready to be accepted.
  - A response from the peripheral device indicating that it is ready to accept data
- **INTR - (Interrupt Request):**
  - A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU.
  - INTR is set when ACK is a "one", OBF is a "one" and INTE is a "one".
  - It is reset by the falling edge of WR.
- **INTE A:** Controlled by bit set/reset of PC6.
- **INTE B:** Controlled by bit set/reset of PC2.

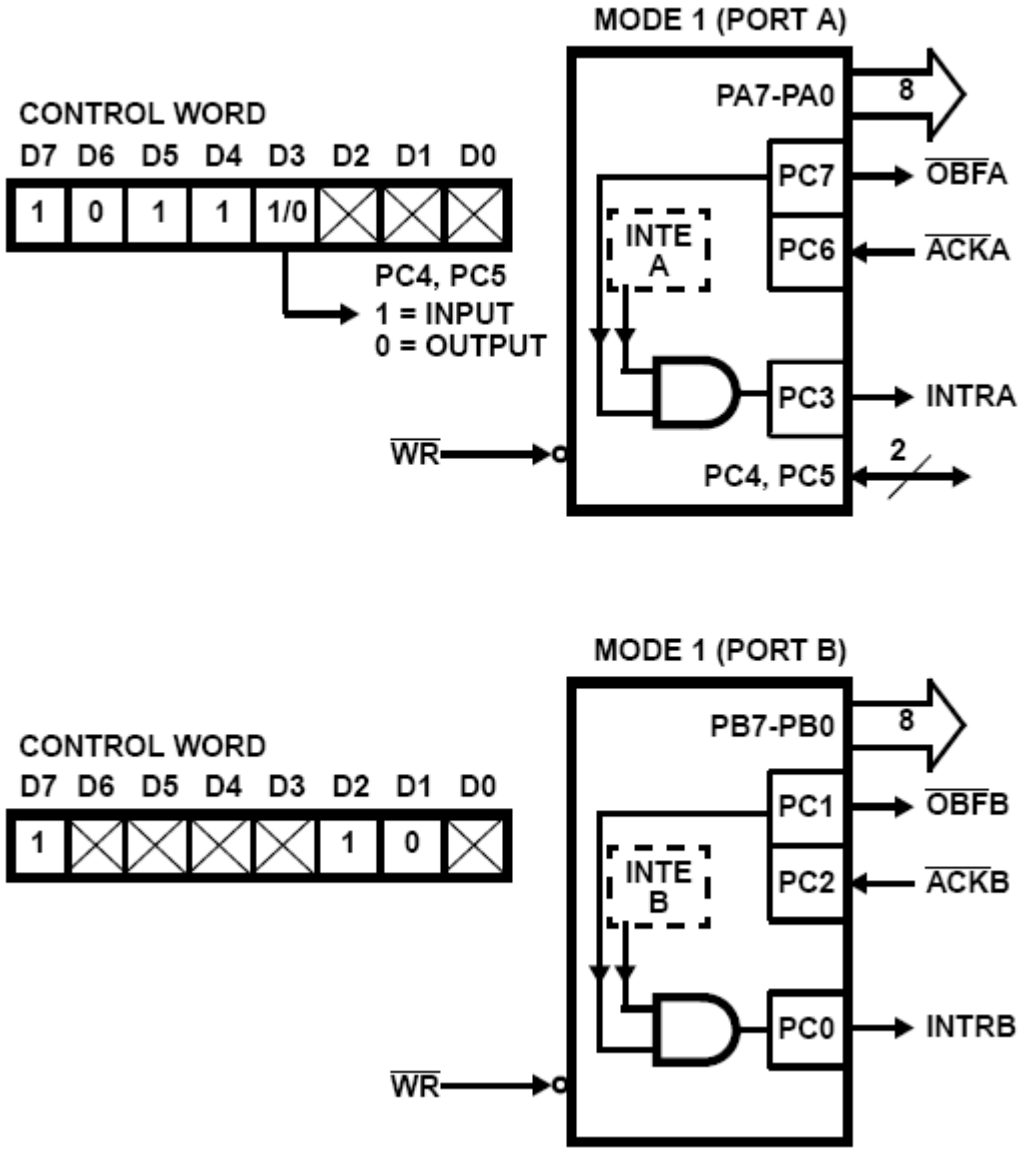


Figure 8: Mode 1 output.

Operating Modes of the 8255

Mode 2 (Strobed Bidirectional Input / Output)

- This mode provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O).
- In this mode, port A uses the lines on port C to generate or accept these “hand shaking” signals.
- The basic features of this mode are:
  - Used in Group A only.
  - One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C)
  - Both inputs and outputs are latched.
  - The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A)

Operating Modes of the 8255

Mode 2 (Strobed Bidirectional Input / Output)

- Figure 9 shows the control signals for mode 2 configurations.
- Input Operations:
  - **STB' -** (Strobe Input)**:** A "low" on this input loads data into the input latch.
  - **IBF** - (Input Buffer Full F/F)**:** A "high" on this output indicates that data has been loaded into the input latch.
  - **INTE 2** - (The INTE flip-flop associated with IBF)**:** Controlled by bit set/reset of PC4.
  - **INTR -** (Interrupt Request)**:** A high on this output can be used to interrupt the CPU for both input or output operations.

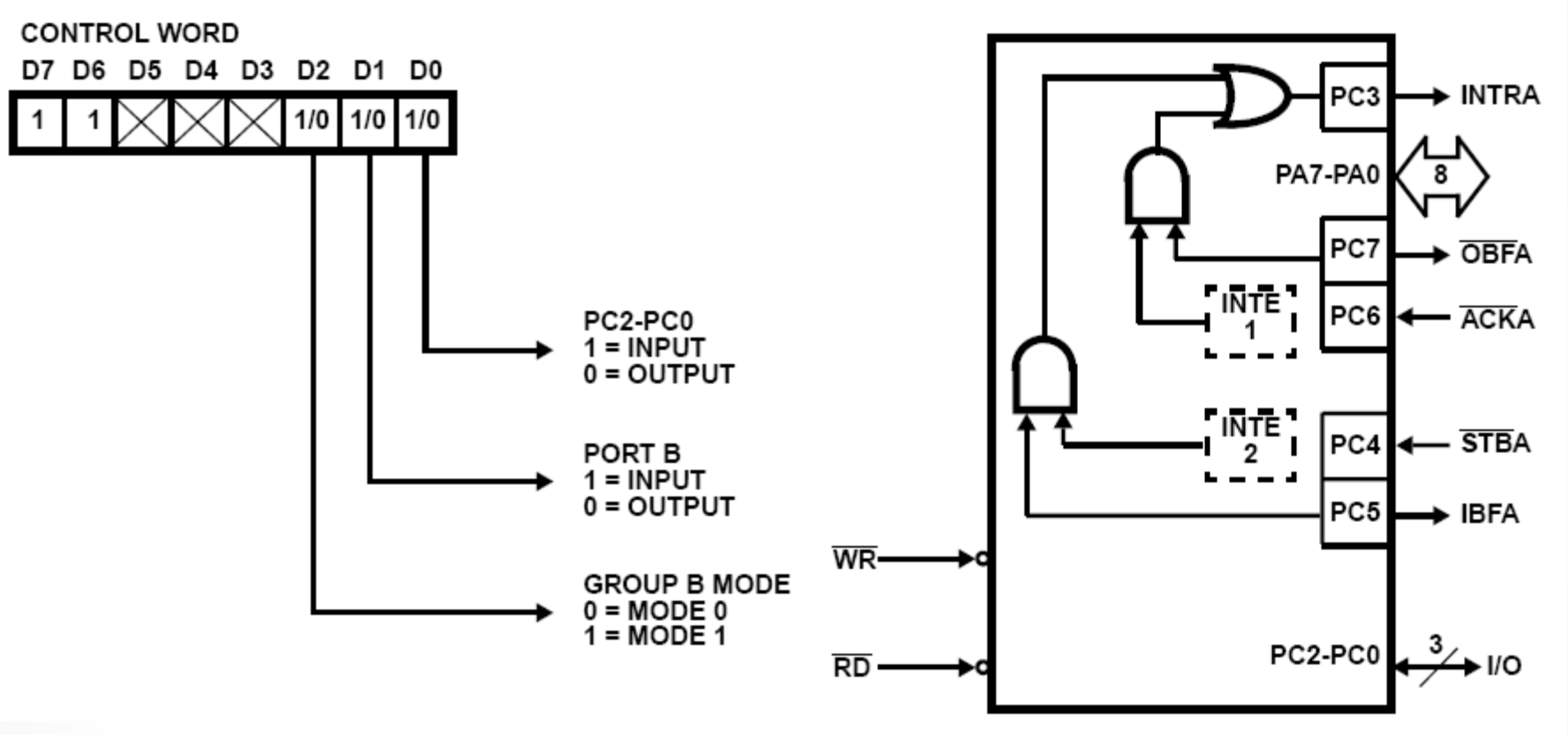


Figure 9: Mode 2 control signals.

Operating Modes of the 8255

Mode 2 (Strobed Bidirectional Input / Output)

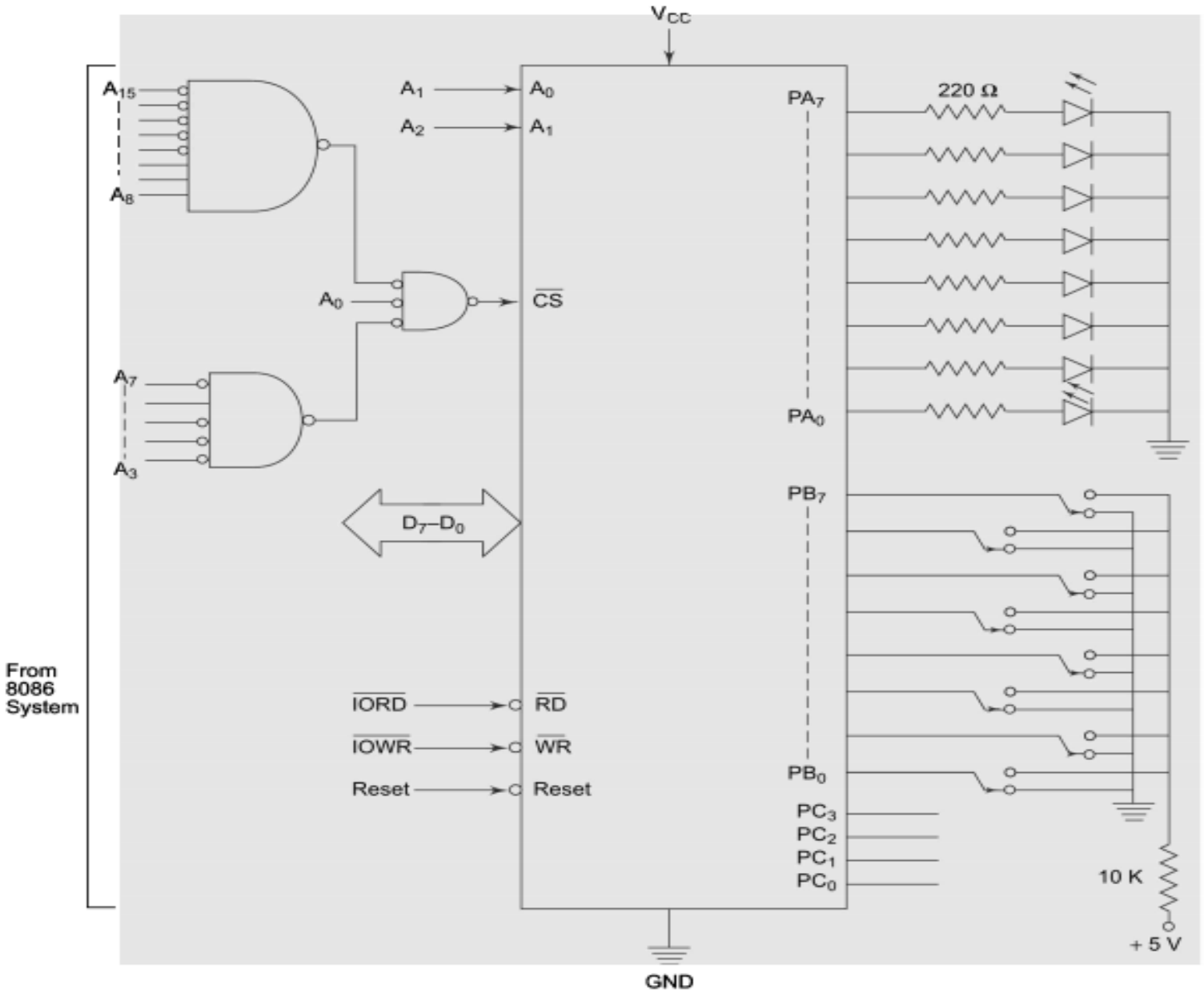
- Input Operations:
  - **STB' -** (Strobe Input)**:** A "low" on this input loads data into the input latch.
  - **IBF** - (Input Buffer Full F/F)**:** A "high" on this output indicates that data has been loaded into the input latch.
  - **INTE 2** - (The INTE flip-flop associated with IBF)**:** Controlled by bit set/reset of PC4.
  - **INTR -** (Interrupt Request)**:** A high on this output can be used to interrupt the CPU for both input or output operations.
- Output Operations:
  - **OBF'** - (Output Buffer Full): The OBF output will go "low" to indicate that the CPU has written data out to port A.
  - **ACK'** - (Acknowledge): A "low" on this input enables the three-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.
  - **INTE 1** - (The INTE flip-flop associated with OBF): Controlled by bit set/reset of PC4.

Example 1: Interface an 8255 chip with 8086 to work as an I/O port. Initialize port A as output port, Port B as I/P port and Port C as O/P port. Port A address should be 0740H. Write an ALP to sense switch positions SW0–SW7 connected at port B. The sensed pattern is to be displayed on port A, to which 8 LED's are connected, while port C lower displays number of on switches out of the total eight switches ?

Example 2: Interface a 4 X4 keypad with 8086 using 8255,

and write an ALP for detecting a key closure and return the key code in AL.

Example 3:Interface an 8255 with 8086 at 80H as an I/O address of Port A. Interface 7 segment displays with the 8255. Write an ALP to display 0-9 over the 7 segment displays continuously as per their positions starting with 0 at the least significant position ? Note the 7 segment will be cathode type


V_{CC}
A_{15}
A_8
A_7
A_3
A_1
A_2
A_0
A_1
A_0
$\overline{CS}$
D_7–D_0
$\overline{IORD}$
$\overline{IOWR}$
Reset
$\overline{RD}$
$\overline{WR}$
Reset
From 8086 System
PA_7
PA_0
PB_7
PB_0
PC_3
PC_2
PC_1
PC_0
220 Ω
10 K
+ 5 V
GND

Tank you

Good luck