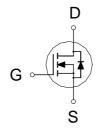
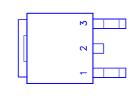
N-Channel Logic Level Enhancement Mode Field Effect Transistor

P3055LDG TO-252 (DPAK) Lead-Free

PRODUCT SUMMARY

$V_{(BR)DSS}$	R _{DS(ON)}	I _D		
25	50m	12A		





1. GATE

2. DRAIN

3. SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST C	SYMBOL	LIMITS	UNITS	
Gate-Source Voltage	V_{GS}	±20	V	
Continuous Dusin Comment	T _C = 25 °C		12	
Continuous Drain Current	T _C = 100 °C	- I _D	8	Α
Pulsed Drain Current ¹	I _{DM}	45		
Avalanche Energy	L = 0.1mH	E _{AS}	60	
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	3	— mJ
Power Dissipation	T _C = 25 °C	Б	48	W
	T _C = 100 °C	P _D	20	VV
Operating Junction & Storage Temperature Range		T_{j},T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 sec.)		T _L	275	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{ hetaJC}$		3	
Junction-to-Ambient	$R_{ heta JA}$		75	°C/W
Case-to-Heatsink	$R_{ heta CS}$	1		

¹Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS (T_C = 25 °C. Unless Otherwise Noted)

LEEGTRICAL GHARACTERISTICS	ECTRICAL CHARACTERISTICS (T _C = 25 °C, Unless Otherwise Noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
TANAMETER	OTHIBOL	TEST CONDITIONS	MIN	TYP	MAX	OIVII
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	25			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu A$	8.0	1.2	2.5	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			±250	nA
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 20V, V_{GS} = 0V$			25	^
Zelo Gate Voltage Diam Guilent		$V_{DS} = 20V, V_{GS} = 0V, T_{J} = 125 ^{\circ}C$			250	μΑ

 $^{^{2}}$ Duty cycle $\leq 1\%$

NIKO-SEM

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On-State Drain Current ¹	I _{D(ON)}	$V_{DS} = 10V, V_{GS} = 10V$	12			Α
Drain-Source On-State	D	$V_{GS} = 5V, I_D = 12A$		70	120	m
Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 12A$		50	90	111
Forward Transconductance ¹	g _{fs}	$V_{DS} = 15V, I_{D} = 12A$		16		S
		DYNAMIC				
Input Capacitance	C _{iss}			450		
Output Capacitance	C _{oss}	$V_{GS} = 0V, V_{DS} = 15V, f = 1MHz$		200		pF
Reverse Transfer Capacitance	C_{rss}			60		
Total Gate Charge ²	Q_g			15		
Gate-Source Charge ²	Q_{gs}	$V_{DS} = 0.5V_{(BR)DSS}, V_{GS} = 10V,$		2.0		nC
Gate-Drain Charge ²	Q_{gd}	$I_D = 6A$		7.0		
Turn-On Delay Time ²	t _{d(on)}			6.0		
Rise Time ²	t _r	$V_{DS} = 15V, R_{L} = 1$		6.0		nS
Turn-Off Delay Time ²	t _{d(off)}	$I_D \cong 12A, \ V_{GS} = 10V, \ R_{GS} = 2.5$		20		110
Fall Time ²	t _f			5.0		
SOURCE-DRAIN [DIODE RATI	NGS AND CHARACTERISTICS (T _C	= 25 °(C)		
Continuous Current	Is				12	۸
Pulsed Current ³	I _{SM}				20	Α
Forward Voltage ¹	V _{SD}	$I_F = I_S$, $V_{GS} = 0V$			1.5	V
Reverse Recovery Time	t _{rr}			30		nS
Peak Reverse Recovery Current	I _{RM(REC)}	$I_F = I_S$, $dI_F/dt = 100A / \mu S$		15		Α
Reverse Recovery Charge	Q _{rr}			0.043		μС

¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

REMARK: THE PRODUCT MARKED WITH "P3055LDG", DATE CODE or LOT #

Orders for parts with Lead-Free plating can be placed using the PXXXXXXG parts name.

²Independent of operating temperature.
³Pulse width limited by maximum junction temperature.

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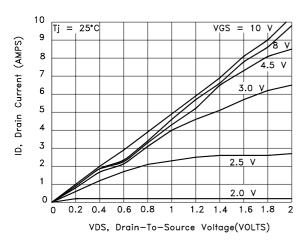


Fig.1 On-Resistance Variation with Temperature

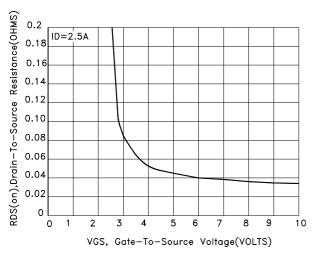


Fig.3 On-Resistance versus Gate-To-Source Voltage

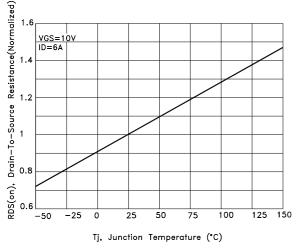


Fig.5 On-Rresistance Variation with Temperature

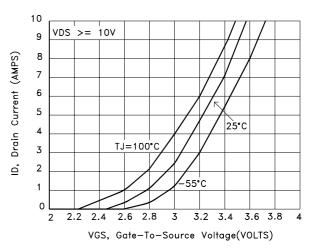


Fig.2 Transfer Characteristics

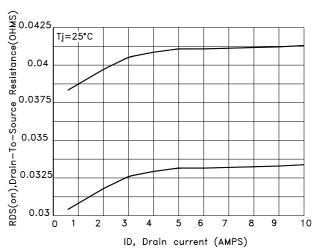
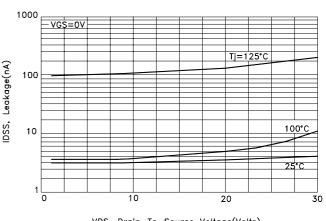


Fig.4 On-Resistance versus Drain Current and Gate Voltage



VDS, Drain-To-Source Voltage(Volts)

Fig.6 Drain-To-Source Leakage Current versus Voltage

TO-252 (DPAK) MECHANICAL DATA

Dimension	mm			Discouries	mm		
	Min.	Тур.	Max.	Dimension	Min.	Тур.	Max.
Α	9.35		10.4	Н	0.89		2.03
В	2.2		2.4	1	6.35		6.80
С	0.45		0.6	J	5.2		5.5
D	0.89		1.5	K	0.6		1
Е	0.45		0.69	L	0.5		0.9
F	0.03		0.23	M	3.96	4.57	5.18
G	5.2		6.2	N			

