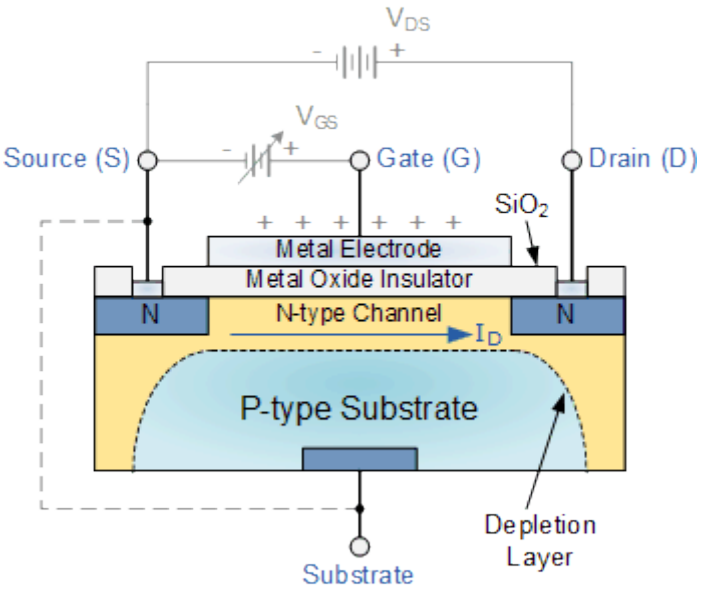
MOSFET and logic Gates

1. The MOSFET

1.1. Basic MOSFET Structure and Symbol



MOSFET's operate the same as JFET's but have a gate terminal that is electrically isolated from the conductive channel.

As well as the Junction Field Effect Transistor (JFET), there is another type of Field Effect Transistor available whose Gate input is electrically insulated from the main current carrying channel. The MOSFET is a type of semiconductor device called an **Insulated Gate Field Effect Transistor (IGFET)**.

The most common type of insulated gate FET which is used in many different types of electronic circuits is called the **Metal Oxide Semiconductor Field Effect Transistor** or **MOSFET** for short.

The **IGFET** or **MOSFET** is a voltage controlled field effect transistor that differs from a JFET in that it has a "Metal Oxide" Gate electrode which is electrically insulated from the main semiconductor n-channel or p-channel by a very thin layer of insulating material usually silicon dioxide, commonly known as glass.

This ultra thin insulated metal gate electrode can be thought of as one plate of a capacitor. The isolation of the controlling Gate makes the input resistance of the **MOSFET** extremely high way up in the Mega-ohms (MΩ) region thereby making it almost infinite.

As the Gate terminal is electrically isolated from the main current carrying channel between the drain and source, "NO current flows into the gate" and just like the JFET, the MOSFET also acts like a voltage controlled resistor where the current flowing through the main channel between the Drain and Source is proportional to the input voltage.

MOSFETs are three terminal devices with a Gate, Drain and Source and both P-channel (PMOS) and N-channel (NMOS) MOSFETs are available. The MOSFETs are available in two basic forms:

- Depletion Type: the transistor requires the Gate-Source voltage, (V_{GS}) to switch the device "OFF". The depletion mode MOSFET is equivalent to a "Normally Closed" switch.
- Enhancement Type: the transistor requires a Gate-Source voltage, (V_{GS}) to switch the device "ON". The enhancement mode MOSFET is equivalent to a "Normally Open" switch.

The basic construction for both configurations of MOSFETs are shown below.

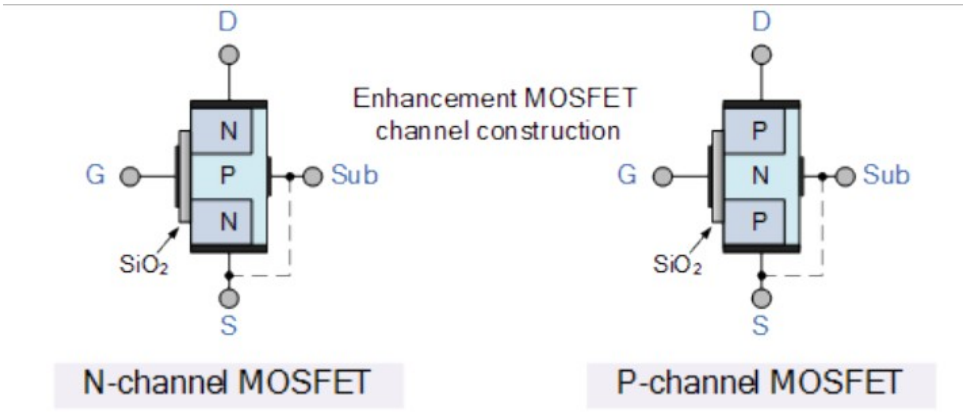


Figure 1: MOSFET basic construction

The MOSFET symbols above show an additional terminal called the Substrate and is not normally used as either an input or an output connection but instead it is used for grounding the substrate. It connects to the main semiconductive channel through a diode junction to the body or metal tab of the MOSFET.

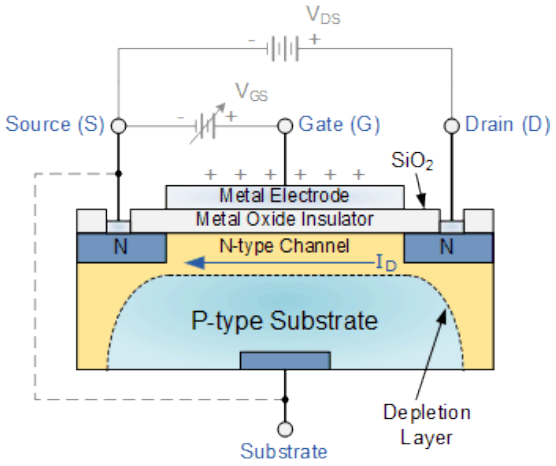
Usually in discrete type MOSFETs, this substrate lead is connected internally to the source terminal. When this is the case, as in enhancement types it is omitted from the symbol for clarification.

The line in the MOSFET symbol between the drain (D) and source (S) connections represents the transistors semiconductive channel.

- If this channel line is a solid unbroken line then it represents a "Depletion" (normally-ON) type MOSFET as drain current can flow with zero gate biasing potential.
- If the channel line is shown as a dotted or broken line, then it represents an "Enhancement" (normally-OFF) type MOSFET as zero drain current flows with zero gate potential.

The direction of the arrow pointing to this channel line indicates whether the conductive channel is a P-type or an N-type semiconductor device.

1.2. Basic MOSFET Structure and Symbol



Both the Depletion and Enhancement type MOSFETs use an electrical field produced by a gate voltage to alter the flow of charge carriers (electrons for n-channel or holes for P-channel) through the semiconductive drain-source channel. The gate electrode is placed on top of a very thin insulating layer and there are a pair of small n-type regions just under the drain and source electrodes.

The gate of a junction field effect transistor, JFET must be biased in such a way as to reverse-bias the pn-junction. With an insulated gate MOSFET device no such limitations apply so it is possible to bias the gate of a MOSFET in either polarity, positive (+ve) or negative (-ve).

This makes the MOSFET device especially **valuable as electronic switches or to make logic gates** because with no bias they are normally non-conducting and this high gate input resistance means that very little or no control current is needed as MOSFETs are voltage controlled devices. Both the p-channel and the n-channel MOSFETs are available in two basic forms, the **Enhancement** type and the **Depletion** type.

1.3. Depletion-mode MOSFET

The **Depletion-mode MOSFET**, which is less common than the enhancement mode types is normally switched “ON” (conducting) without the application of a gate bias voltage. That is the channel conducts when $V_{GS} = 0$ making it a “normally-closed” device.

The circuit symbol for a depletion MOS transistor uses a solid channel line to signify a normally closed conductive channel.

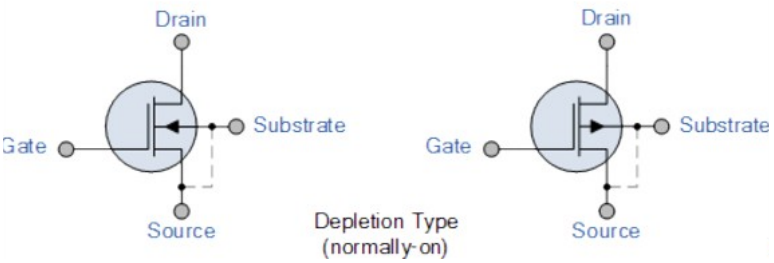
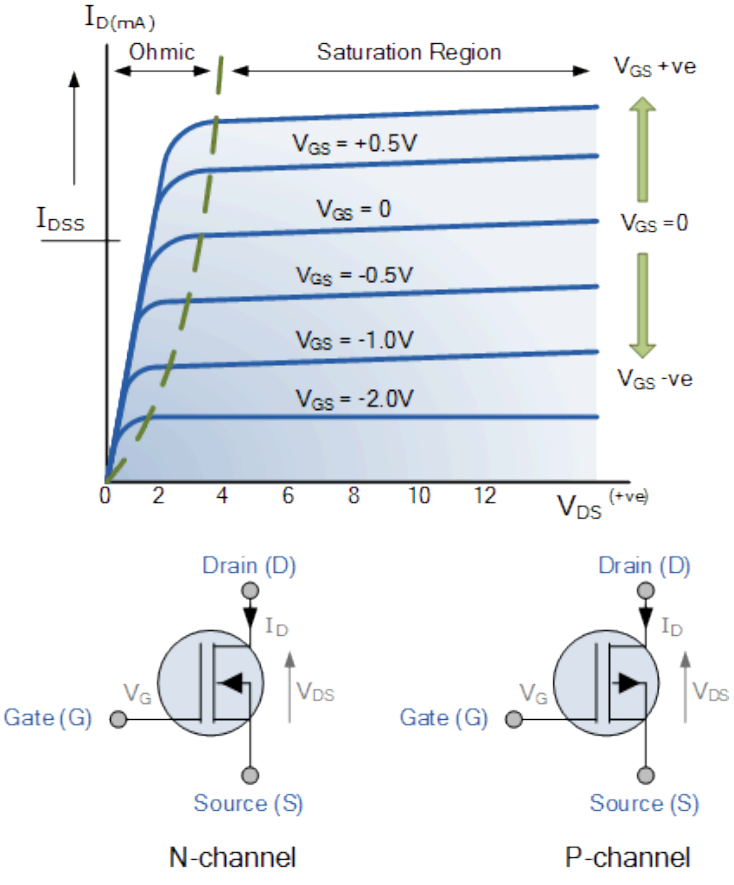


Figure 2: N-Channel *P-Channel*

For the n-channel depletion MOS transistor, a negative gate-source voltage, $-V_{GS}$ will deplete (hence its name) the conductive channel of its free electrons switching the transistor “OFF”. Likewise for a p-channel depletion MOS transistor a positive gate-source voltage, $+V_{GS}$ will deplete the channel of its free holes turning it “OFF”.

In other words, for an n-channel depletion mode MOSFET: $+V_{GS}$ means more electrons and more current. While a $-V_{GS}$ means less electrons and less current. The opposite is also true for the p-channel types. Then the depletion mode MOSFET is equivalent to a “normally-closed” switch.

1.3.1. Depletion-mode N-Channel Circuit Symbols



The depletion-mode MOSFET is constructed in a similar way to their JFET transistor counterparts were the drain-source channel is inherently conductive with the electrons and holes already present within the n-type or p-type channel. This doping of the channel produces a conducting path of low resistance between the Drain and Source with zero Gate bias.

1.4. Enhancement-mode MOSFET

The more common **Enhancement-mode MOSFET** or eMOSFET, is the reverse of the depletion-mode type. Here the conducting channel is lightly doped or even undoped making it non-conductive. This results in the device being normally "OFF" (non-conducting) when the gate bias voltage, V_{GS} is equal to zero.

The circuit symbol for an enhancement MOS transistor uses a broken channel line to signify a normally open non-conducting channel.

Figure 3: N-Channel *P-Channel*

For the n-channel enhancement MOS transistor a drain current will only flow when a gate voltage (V_{GS}) is applied to the gate terminal greater than the threshold voltage (V_{TH}) level in which conductance takes place making it a transconductance device.

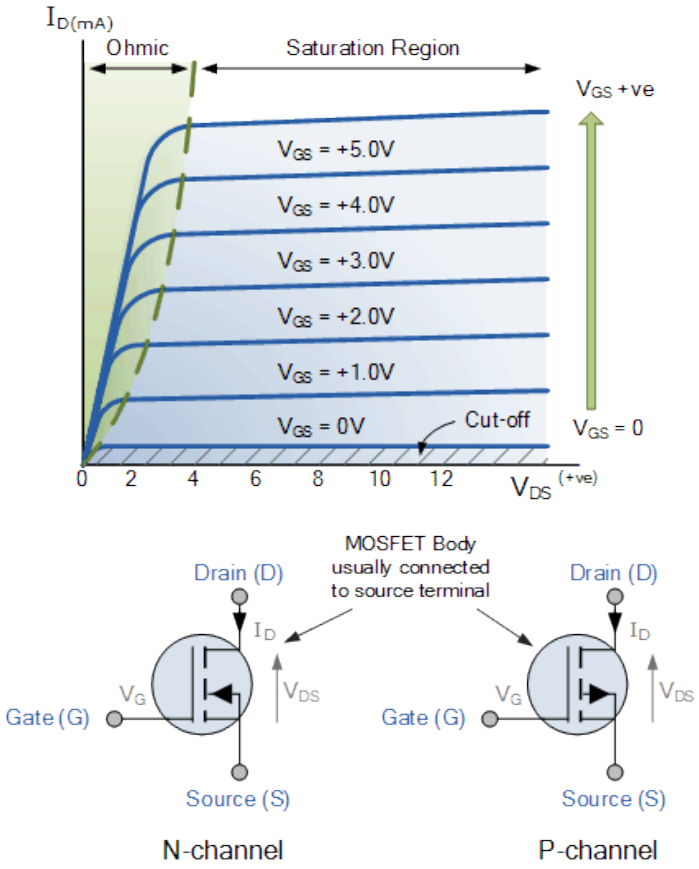
The application of a positive (+ve) gate voltage to an n-type eMOSFET attracts more electrons towards the oxide layer around the gate thereby increasing or enhancing (hence its name) the thickness of the channel allowing more current to flow. This is why this kind of transistor is called an enhancement mode device as the application of a gate voltage enhances the channel.

Increasing this positive gate voltage will cause the channel resistance to decrease further causing an increase in the drain current, I_D through the channel.

In other words, for an n-channel enhancement mode MOSFET:

- $+V_{GS}$ turns the transistor "ON", while a zero or $-V_{GS}$ turns the transistor "OFF". Thus the enhancement-mode MOSFET is equivalent to a "normally-open" switch.
- The reverse is true for the p-channel enhancement MOS transistor. When $V_{GS} = 0$ the device is "OFF" and the channel is open. The application of a negative (-ve) gate voltage to the p-type eMOSFET enhances the channels conductivity turning it "ON". Then for a p-channel enhancement mode MOSFET: $+V_{GS}$ turns the transistor "OFF", while $-V_{GS}$ turns the transistor "ON".

1.4.1. Enhancement-mode N-Channel Circuit Symbols



Enhancement-mode MOSFETs make excellent electronics switches due to their low "ON" resistance and extremely high "OFF" resistance as well as their infinitely high input resistance due to their isolated gate. Enhancement-mode MOSFETs are used in integrated circuits to produce CMOS type *Logic Gates* and power switching circuits in the form of as PMOS (P-channel) and NMOS (N-channel) gates. CMOS actually stands for *Complementary MOS* meaning that the logic device has both PMOS and NMOS within its design.

1.5. MOSFET Summary

The **MOSFET** has an extremely high input gate resistance with the current flowing through the channel between the source and drain being controlled by the gate voltage.

Typical applications for metal oxide semiconductor field effect transistors are in Logic CMOS Gates etc.

Also, notice that

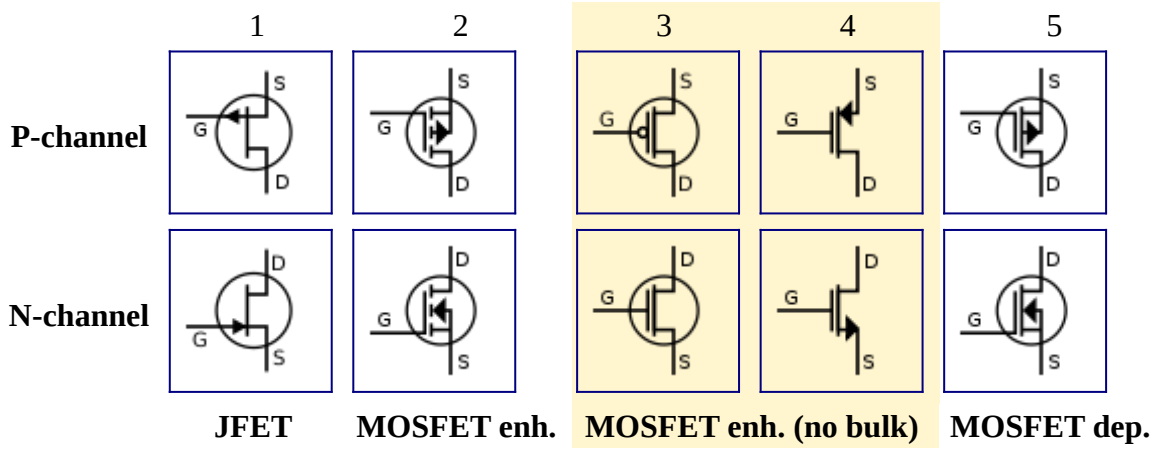
- a dotted or broken line within the symbol indicates a normally "OFF" enhancement type showing that "NO" current can flow through the channel when zero gate-source voltage V_{GS} is applied.
- A continuous unbroken line within the symbol indicates a normally "ON" Depletion type showing that current "CAN" flow through the channel with zero gate voltage.

For p-channel types the symbols are exactly the same for both types except that the arrow points outwards. This can be summarised in the following switching table.

MOSFET type	V_{GS} = +ve	V_{GS} = 0	V_{GS} = -ve
N-Channel Depletion	ON	ON	OFF
N-Channel Enhancement	ON	OFF	OFF
P-Channel Depletion	OFF	ON	ON
P-Channel Enhancement	OFF	OFF	ON

So for n-type enhancement type MOSFETs, a positive gate voltage turns “ON” the transistor and with zero gate voltage, the transistor will be “OFF”. For a p-channel enhancement type MOSFET, a negative gate voltage will turn “ON” the transistor and with zero gate voltage, the transistor will be “OFF”. The voltage point at which the MOSFET starts to pass current through the channel is determined by the threshold voltage V_{TH} of the device.

The following table shows the different symbols of MOSFET. The most used ones are those of column “ and 4 regardless of the type (depletion or enhancement) od the MOS.



2. Logic Gates using MOSFET

2.1. Complementary CMOS

This design method is the most popular method; it is an application of the CMOS inverter with several inputs. The main advantage of this method is the robustness (not very sensitive to noise), while having good performance and low power consumption, with no static power dissipation.

A complementary CMOS logic gate is a combination of two transistor networks:

- a network that connects the output to V_{DD} (PUN: pull-up network) when a "1" is requested and
- a network that connects the output to ground (PDN: pull-down network) when a "0" is request. Figure 1. shows the general diagram of a supplementary circuit.

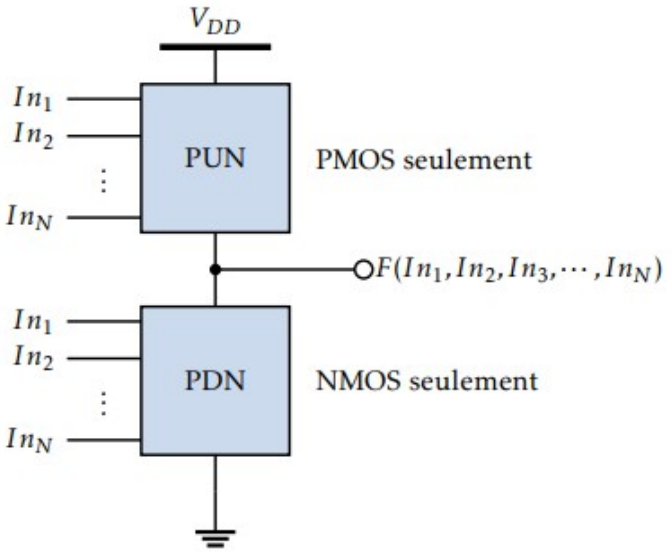


Figure 4: Complementary Logic

The PDN consists only of NMOS, while the PUN consists only of PMOS. The PUN and PDN networks are mutually exclusive: **there is only one of the two networks that is conductive in permanent regime.**

2.1.1. Construction of the PDN and PUN

The table below summarizes the “real” conditions for the different threshold voltages for the various types of MOSFET.

Type of MOSFET	Region of operation		
	Cut-Off (OFF)	Saturation (ON)	Linear/Ohmic (Amplifier)
Enhancement N-Channel	$V_{GS} < V_{TH}$	$V_{GS} > V_{TH}$ and $V_{DS} > V_P$	$V_{GS} > V_{TH}$ and $V_{DS} < V_P$
Enhancement P-Channel	$V_{GS} > -V_{TH}$	$V_{GS} < -V_{TH}$ and $V_{DS} < -V_P$	$V_{GS} < -V_{TH}$ and $V_{DS} > -V_P$
Depletion N-Channel	$V_{GS} < -V_{TH}$	$V_{GS} > -V_{TH}$ and $V_{DS} > V_P$	$V_{GS} > -V_{TH}$ and $V_{DS} < V_P$
Depletion P-Channel	$V_{GS} > V_{TH}$	$V_{GS} < V_{TH}$ and $V_{DS} < -V_P$	$V_{GS} < V_{TH}$ and $V_{DS} > -V_P$

There are a few general rules to follow when building the PDN and PUN networks:

1. A transistor can be modeled as a switch:

- ✔ a NMOS is ON when the input is 1, and OFF when the input is 0;
- ✔ a PMOS is ON when the input is 0, and OFF when the input is 1.

2. An NMOS is a better way to connect an output to ground than to V_{DD}, as shown in Figure 2.
   - ✔ In the first case, if the input is 1, the capacitor (the output) can only be loaded up to $V_{DD} - V_{in}$ (and the effect of the substrate cannot be neglected).
   - ✔ On the other hand, if the source of the NMOS is branched to GND, the capacitor can discharge completely when the input is 1.
   - ✔ **The PDN network will therefore consist only of NMOS.**

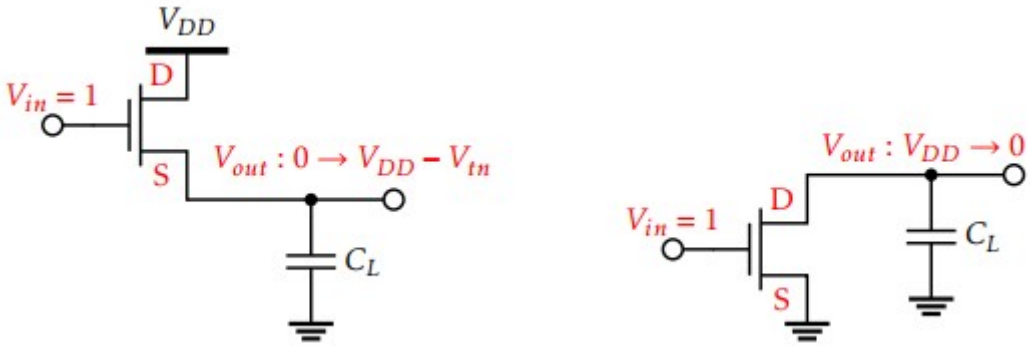


Figure 5: NMOS Logic Gate

3. A PMOS is better for connecting the output to V_{DD}, as shown in Figure 3.
   - ✔ In the first case, if the input is 0, the output can load completely until V_{DD},
   - ✔ while in the second case, the output can only be loaded at V_{tp}.
   - ✔ **The PUN network will therefore consist only of PMOS**.

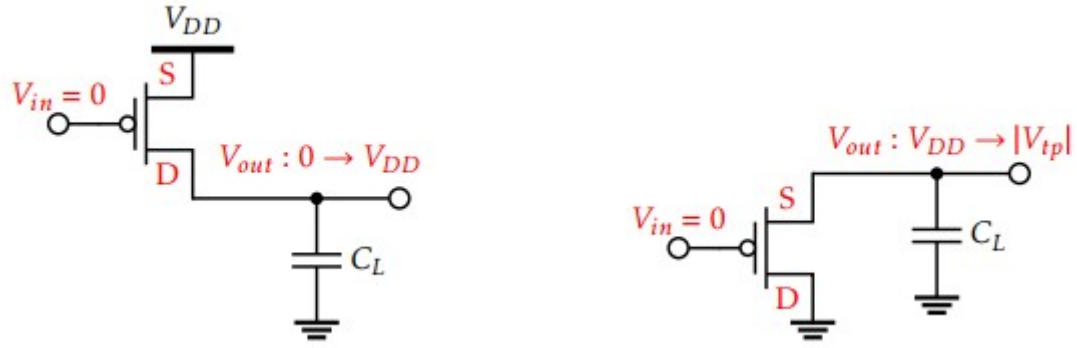


Figure 6: PMOS logic Gate

4. Some rules can be created for the construction of logic gates.
   - ✔ NMOS in series correspond to the AND function.
   - ✔ NMOS in parallel correspond to the OR function.

   These combinations are shown in Figure .

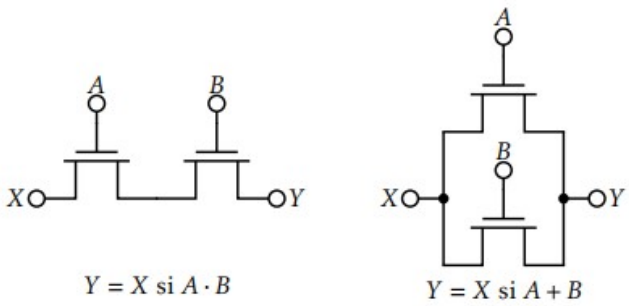


Figure 7: NMOS Logic Gate

5. Serial PMOS correspond to the NOR function, while parallel PMOS correspond to the NAND function; Figure 8.

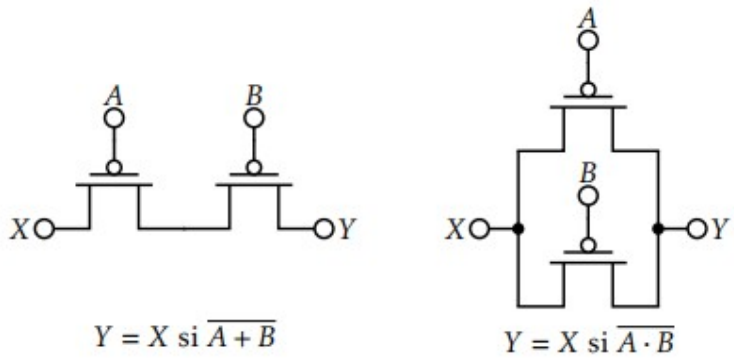


Figure 8: PMOS Logic Gate

6. In complementary logic, the PUN is the complement of the PDN (which can be demonstrated using DeMorgan's theorem[i]). In practice, a parallel combination of transistors in the PDN corresponds to a combination of transistors in the PUN, and vice versa.
7. In complementary logic, the logic gate is naturally reversing:
   - ✔ The gate is a combination of NAND, NOR, and XNOR. To perform the non-inverse logic functions, an inverter must be added to the output.
8. The number of transistors needed to realize a logic function is $2N$, where N is the number of inputs.

2.2. Example1

We will design a NAND gate with 2 inputs. The function $F = \overline{A} \cdot \overline{B}$. According to the above rules, the PDN network is composed of 2 NMOS in series, and therefore the PUN network is composed of 2 PMOS in parallel. Figure 9 shows the corresponding circuit.

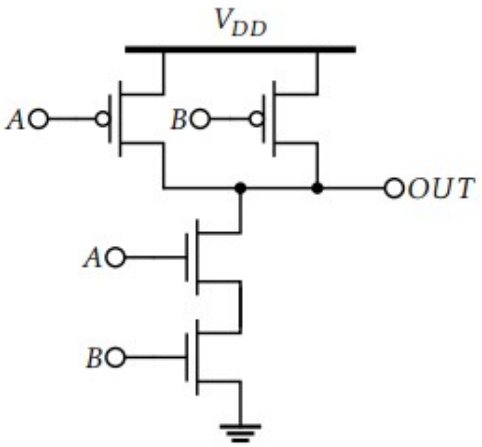


Figure 9: 2 inputs NAND Gate

It can be verified that the output is always branched to V_{DD} or GND, depending on the input, **but never to both at the same time.**

To design any gate, we conform to the following procedures:

1. Make sure the function is reversing (everything is NOT), and simplify it.
2. Building the PDN
   a) If we have a "+", the transistors are in parallel,
   b) If we have a "·", the transistors are in series
3. Building the PUN
   a) If transistors are in parallel in the PDN, they are in series in the PUN
   b) If transistors are in series in the PDN, they are in parallel in the PUN

2.3. Example 2

Build the circuit to implement the function $F=\overline{D+A\cdot(B+C)}$.

The function is reversing, so there is no need to change it. You cannot simplify the function.

So we start by creating the PDN network.

- You have to start at the bottom of the equation.
- In this case, since we have B + C, we must place these transistors in parallel.
- Then, because A multiplies (B + C), it must be placed in series with this combination.
- And lastly, since D is added to the combination A·(B + C), D must be placed in parallel with A·(B+C). The result is shown in Figure 10.

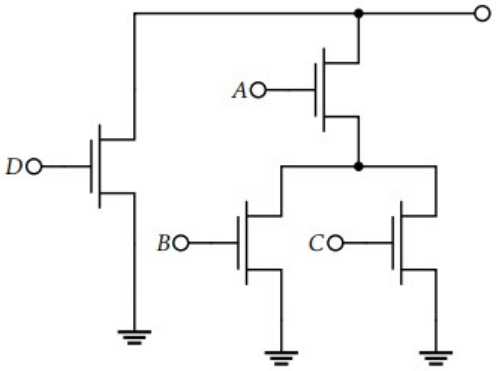


Figure 10: Pull Down Network (PDN)

The PUN can then be created. The transistors in series are now in parallel, and vice versa, as shown in Figure 11.

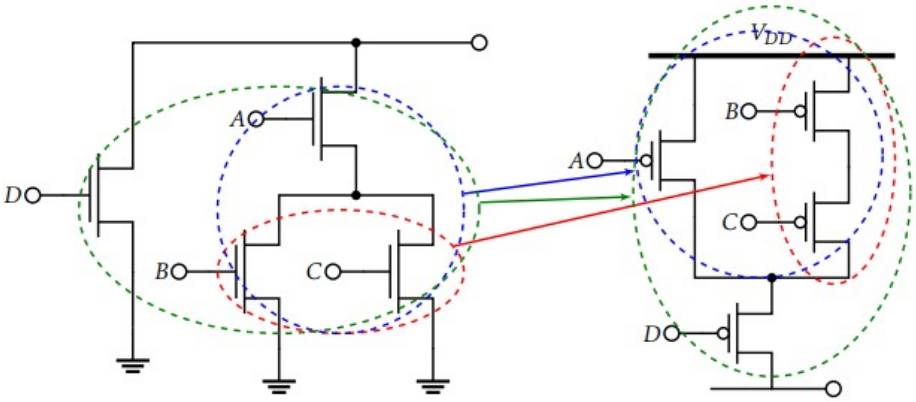


Figure 11: PUN building

The final result is shown in Figure 12.

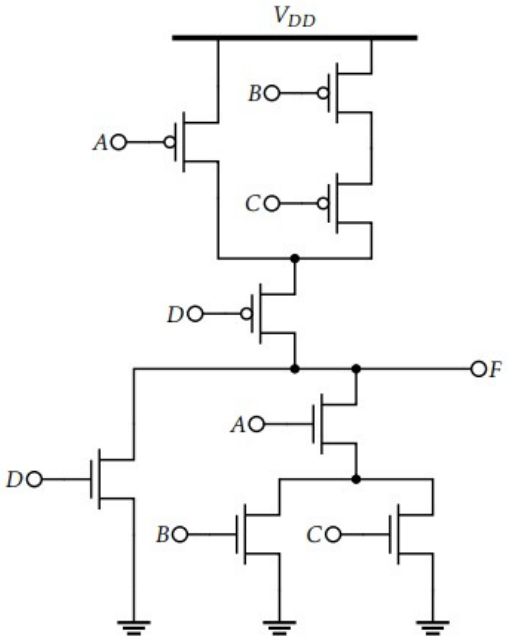


Figure 12: Final Circuit for F function

3. Boolean Algebraic Identities

Let us begin our exploration of Boolean algebra by adding numbers together:

Basic Boolean Algebraic Identities

	Additive	Multiplicative
0 + 0 = 0	A + 0 = A	0A = 0
0 + 1 = 1	A + 1 = 1	1A = A
1 + 0 = 1	A + A = A	AA = A
1 + 1 = 1	A + $\overline{A}$ = 1	A$\overline{A}$ = 0

$\overline{\overline{A}} = A$

3.1. DeMorgan's Theorem

$\overline{AB} = \overline{A} + \overline{B}$

3.2. Usefull Boolean rules

Useful Boolean rules for simplification

$A + AB = A$
$A + \overline{A}B = A + B$
$(A + B)(A + C) = A + BC$

$A + AB$
↓ Factoring A out of both terms
$A(1 + B)$
↓ Applying identity A + 1 = 1
$A(1)$
↓ Applying identity 1A = A
A

$A + \overline{A}B$
↓ Applying the previous rule to expand A term A + AB = A
$A + AB + \overline{A}B$
↓ Factoring B out of 2nd and 3rd terms
$A + B(A + \overline{A})$
↓ Applying identity A + $\overline{A}$ = 1
$A + B(1)$
↓ Applying identity 1A = A
$A + B$

$(A + B)(A + C)$
↓ Distributing terms
$AA + AC + AB + BC$
↓ Applying identity AA = A
$A + AC + AB + BC$
↓ Applying identity A + AB = A to the A + AC term
$A + AB + BC$
↓ Applying identity A + AB = A to the A + AB term
$A + BC$

i

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https://www.electronics-tutorials.ws/transistor/tran_6.html