Field effect transistors

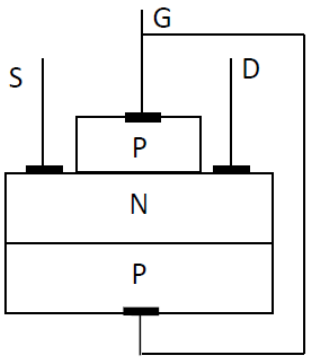
1. Introduction

Bipolar transistors, although still very useful in electronics, are nevertheless characterized by a number of defects, such as their low input impedance and the fact that they can be considered as sources of current controlled by current.

There is another family of transistors which have the advantage of having a very high input impedance and whose state depends on a voltage, and not a current, which makes them sources of current controlled by voltage. These are the field-effect transistors.

2. Junction field-effect transistors

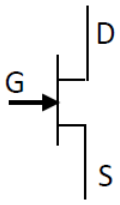
Acronyms: JFET (Junction Field Effect Transistor)



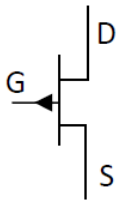
A JFET consists of a doped silicon "channel" and two differently doped zones surrounding it. These two areas are connected to each other and form the Gate (G) of the transistor. Two contacts filed on the channel form its Drain (D) and its Source (S)

The drawing opposite represents a JFET Channel N.

Symbols :



N-Channel JFET



P-Channel JFET

3. Characteristics of field-effect transistors

Let's take the example of a JFET Channel N.

3.1. Operating principle:

The N channel, between the drain and the source, constitutes a dipole that will be conductive[1] according to the value of the voltage v_{GS} applied between the gate and the source. Indeed, the presence of a negative voltage between the gate and the source creates an electrostatic effect in the channel. We have:

- If $-V_p \leq V_{GS} \leq 0$ => Drain-Source channel is conductive.
- If $V_{GS} \leq -V_p$ => Drain-Source channel is blocked.

The voltage V_p is a characteristic of the transistor. It is called pinch-off voltage.

When the transistor is conductive ($-V_p \leq V_{GS} \leq 0$), it can have two types of operation depending on the voltage V_{DS} between the Drain and the Source.

- If $0 \leq V_{DS} \leq V_P$, the Drain-Source channel behaves as a resistor. The drain current is proportional to V_{DS}. The proportionality factor is called channel resistance R_{DS}, and depends on the voltage V_{GS}.

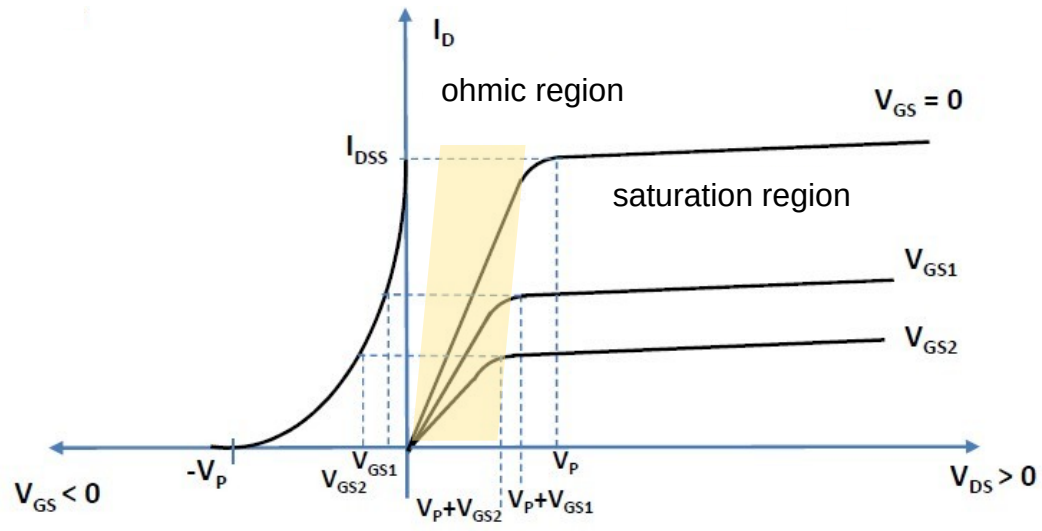
  The transistor is said to operate in its resistive or ohmic zone.

- If $V_{DS} \geq V_p$, the current I_D becomes almost constant and independent of V_{DS}.

  The transistor is said to operate in its saturation zone.

For a given value of V_{DS}, the drain current varies in respect to the voltage V_{GS} according to the law: $I_D = I_{D_{SS}}\left(1 - \frac{V_{GS}}{V_P}\right)^2$. The current $I_{D_{SS}}$, also denoted $I_{D_{max}}$, is an increasing function of V_{DS}.

The entire operation of an N - Channel JFET is summarized on the following feature network. The transistor appears as a dipole controlled by the voltage V_{GS}.



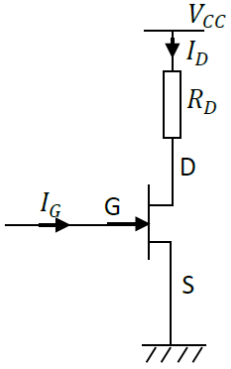
1 Drain-source conductive channel: there is a current noted I_D, called drain current (although it will also be the source current) that flows between D and S.

For a P-channel transistor, the operating principle remains the same, except that all signs of currents and voltages must be reversed.

4. Polarization of JFETs

We try to polarize the transistor in its linear zone.

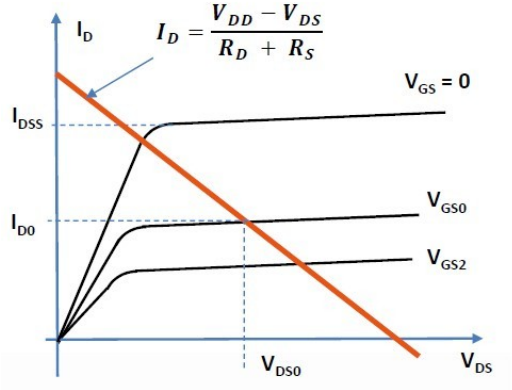
4.1. Polarization by drain resistor.



Note: The input impedance of the transistor being very high, the gate current of the transistor is very low. It is, most of the time, neglected.

If V_{GS} is given, the characteristic $I_D = f(V_{DS})$ is entirely determined among all the curves of the features network. (internal conditions)

In addition, the application of the laws of electronics (law of meshes, Ohm's law) makes it possible to write: $I_D = \frac{V_{CC} - V_{DS}}{R_D}$. (external conditions).



The operating point is found by plotting the load line and the characteristic. It corresponds to the intersection of the two curves. If we want to polarize the JFET in its linear zone, we will choose R_D so that this point is such that $V_{DS} \leq V_P$.

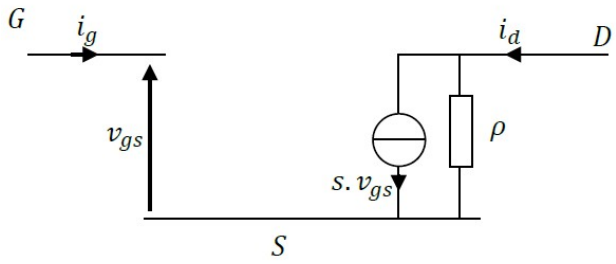
5. Linear equivalent scheme

As with the bipolar transistor, the JFET is used to make amplifiers. In these assemblies, one exploits the properties of linear operation, such as the proportionality between the drain current and the voltage V_{GS}, which puts the action on the particularity of this transistor to be traversed by a current controlled by a voltage.

If the transistor is polarized in its linear area and a small signal v_{gs} is superimposed on the bias voltage $V_{GS,}$ variations i_d and v_{ds} will appear around the continuous values of polarization I_D and V_{DS}. It is shown that: $i_d = s.v_{gs} + \frac{v_{ds}}{\rho}$ (This relation will be accepted), with:

- s = dynamic slope of the transistor = transconductance (of the order of $10^{-3} S$ for usual JFETs). s is also called g_m.
- ρ = dynamic output resistor of the transistor, generally considered to be ∞.

We then obtain the following equivalent scheme:



6. MOS Transistors

There are many variations of FETs, intended for various applications. One of them brings together field-effect transistors called MOS (Metal Oxide Semiconductors), or MOSFETs. For these transistors, the gate is isolated from the channel by an insulating layer of silicon oxide. The gate current is then rigorously zero. The principle of operation is substantially similar to that of the JFET.

As before, there are two types of MOSFETs:

- N-Channel MOS transistors(MOSN) and
- P-Channel MOS transistors (MOSP)

whose symbols are given below:

Transistors and Logic Gates

6.1. Switching transistors

REMINDER: Switching operation: going from conducting to blocked and from blocked to conduction. This mode of operation is the basis for the realization of logic gates.

For MOS transistors, we have:

- MOSFET Channel N :
  - Blocked if $V_{GS}=0\,V$
  - Conductor if $V_{GS}=5\,V$
- MOSFET Channel P :
  - Blocked if $V_{GS}=0\,V$
  - Conductor if $V_{GS}=-5\,V$

A blocked transistor is equivalent to an open switch between the drain and the source, a conductive transistor is equivalent to a closed switch between the drain and the source.

Note : Switching times are not zero and are at the origin of the propagation times of logic gates.

6.2. Technologies: TTL/CMOS

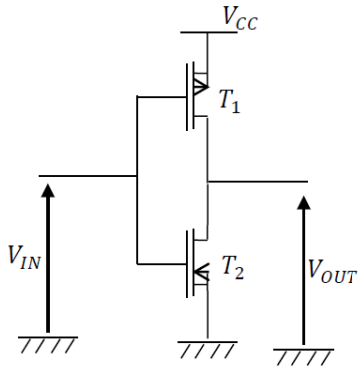
TTL (Transistor Transistor Logic) gates are manufactured using bipolar transistors. These gates are very energy intensivey, due to the low input impedance of the transistors. In addition, these transistors are controlled by a current, while the logical levels are represented by voltage levels. On the other hand, they are fast.

CMOS (Complementary Metal Oxide Semiconductor) logic gates are based on MOSFETs, which consume very little energy (input impedance ∞). They are also voltage controlled. In addition, even though they are known to be slower than bipolar transistors, and thanks to technological advances, are mostly fast enough for most common applications of digital electronics.

6.3. Examples of CMOS technology gates

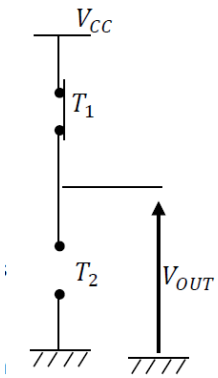
To analyze such circuits, one must ask whether the transistors are conductive or not. It is therefore necessary to express for each of them the voltage V_{GS}, the input voltages being equal to either O $0\,V$ or V_{CC} (= $5\,V$ here).

6.3.1. Not Gate



T_1 is a MOSP, T_2 is a MOSN.

- *If* $V_{IN}=0\,V$:
  - $T_1: V_{GS_1}=V_{IN}-V_{cc}=-5\,V$: the transistor is conductive
  - $T_2: V_{GS_2}=V_{IN}-0=0\,V$: the transistor is blocked

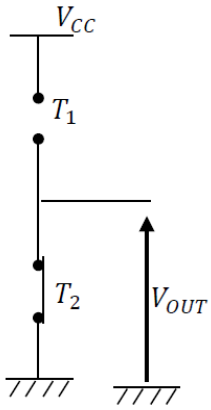


An equivalent diagram can then be redrawn by replacing the transistors with switches. This gives:

In this case, the output is directly connected to the potential V_{CC}. So we have: $V_{OUT}=V_{CC}$.

Note : We can notice that on the diagram equivalent-switches that the gate no longer appears. This is not entirely true, since it is the applied potential in G that determines the state of the transistors (conductor or blocked)

- *If* $V_{IN}=5\,V$:
  - $T_1: V_{GS_1}=V_{IN}-V_{cc}=0\,V$: the transistor is blocked
  - $T_2: V_{GS_2}=V_{IN}-0=5\,V$: the transistor is conductive

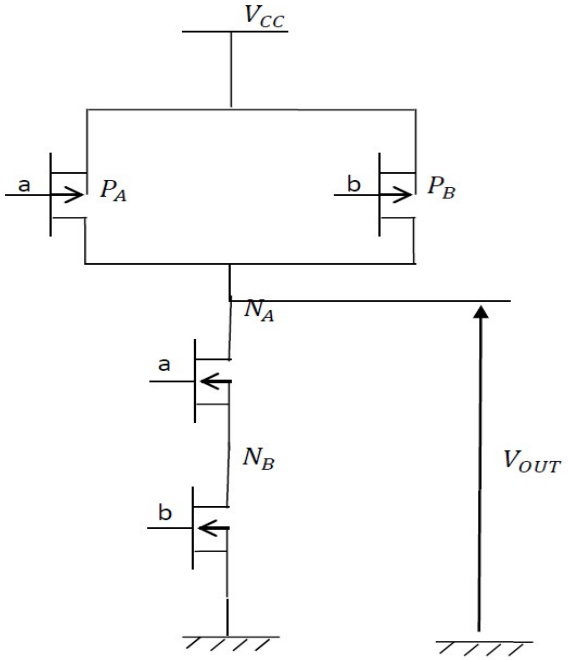


An equivalent diagram can then be redrawn by replacing the transistors with switches. This gives:

In this case, the output is directly connected to the ground. So we have:

$V_{OUT}=0\,V$.

6.3.2. NAND Gate



We could reason in the same way as before to determine the output voltage as a function of the voltages V_a and V_b applied to the inputs “a” and “b” of the transistors.

There are, however, faster methods. First of all, if we observe the diagram well, we can notice that there is a stage comprising only MOSP transistors and a second comprising only MOSN transistors.

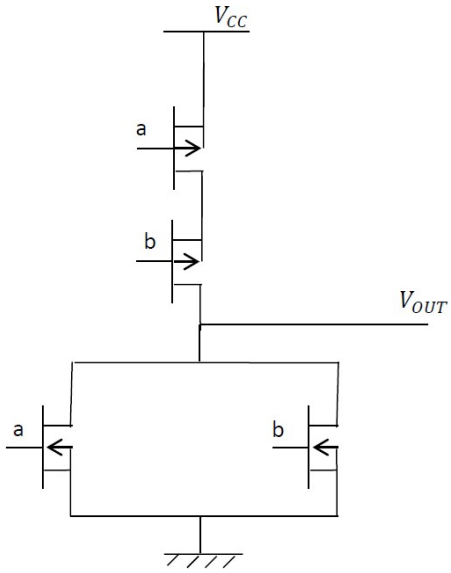
In addition, we see that, if MOSPs are in parallel, MOSNs are in series. Both stages are Complementary. This complementarity ensures one fully defined output. Thus, if the MOSP stage is not conductive, the MOSN stage will be conductive and vice versa.

It is then sufficient to study only one part of the diagram.

For example, here the output will be connected to V_{CC} if P_A or P_B is conductive. A MOSP is known to be conductive if its voltage V_{GS} is equal to −5V. It is therefore necessary to have $V_a=V_b=0\,V$. This allows us to establish the following equation:

$S=\bar{a}+\bar{b}=\overline{a.b}$ which is the equation of a NAND gate.

6.3.3. NOR Gate



We can thus design a NOR gate by reasoning as before. The opposite diagram is obtained: