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Foundation of Computer Systems (CS5102/CS541)

Duration: 2 Hours | Mid-Sem Examination | Marks: 60

Instructions:

- **All questions are compulsory.**
- **1 mark will be awarded for selecting a correct option for Q1, i.e., Multiple Choice Question: Type-I.**
- **3 Marks will be awarded for selecting a correct option and 1 mark will be deducted for selecting a wrong option for Q2, i.e., Multiple Choice Question: Type-II**
- **Only the given Tables at the last page will be evaluated for Q1 and Q2.**
- **No doubt will be entertained during the examination.**

1. Multiple Choice Questions: Type-I

$1 \times 10 = 10$ **Marks**

(i) Consider A, B, and C are in sign magnitude form, and they form an expression as $A = (B - C)$. B and C are each represented in y bits and for the representation of A requires a *minimum* of x bits to avoid overflow. Based on the given conditions, which of the following is the minimum required value of x?

(a) $x = y/2$
(b) $x = y^2$
(c) $x = y + 1$
(d) $x = y + 2$

(ii) Which of the following is the suitable expression for a carry out C of a full-adder with input X, Y, and Z, where Z is carry-in?

(a) $C = (X + Y)(X \oplus Y)Z$
(b) $C = (XY)(X \oplus Y) + Z$
(c) $C = (X + Y) + (X \oplus Y) + Z$
(d) $C = (XY) + (X \oplus Y)Z$

(iii) What will be the value of a 32-bit register, `$s0`, after executing

```
lui $s0, 10101010 00000000 11110000
11110000
```

(a) `11110000 00000000`
(b) `10101010 00000000 00000000 00000000`
(c) `10101010 00000000 11110000 11110000`
(d) `00000000 00000000 10101010 10101010`

(iv) What will be the value of `$s0` in the following assembly code, if $g = 15$ and $h = 5$?

```
#$s0 =f, $s1 = g, $s2 = h
bne $s1, $s2, L1
add $s0, $s1, $s2
L1:  sub $s0, $s1, $s2
```

(a) 15
(b) 10
(c) 5
(d) 0

(v) Which of the following is true for a Callee procedeure?

(a) Returns the result to caller
(b) Returns to the point of call
(c) Must not overwrite registers or memory needed by the caller
(d) All of the above are true

(vi) The performance of a pipeline suffers if

(a) the pipeline stages have different delays
(b) consecutive instructions are dependent on each others
(c) the pipeline stages share hardware resources
(d) All of the above

(vii) In a MIPS multicycle floating point pipeline that supports operand forwarding, there will be _____ stalls between a pair of adjacent MUL instructions that has a RAW dependency between them.

(a) 4
(b) 5
(c) 6
(d) 7

(viii) Let there be two identical CPUs – one is pipelined (say C_1) and another one is non-pipelined (say C_2). To execute a single instruction, C_1 takes τ_1 time and C_2 takes τ_2 time. Then, we can say that:

(a) $\tau_1 \leq \tau_2$
(b) $\tau_1 \geq \tau_2$
(c) $\tau_1 < \tau_2$
(d) τ_1 plus τ_2 is the time taken for one instruction fetch cycle

(ix) Which register set of the following is known as ***Callee-saved*** registers?

(a) `s0 - s7`
(b) `t0 - t9`
(c) `a0 - a3`
(d) `v0 - v1`

(x) Which of the following are NOT true in a pipelined processor?

(I) Bypassing can handle all RAW hazards.
(II) Register renaming can eliminate all register carried WAR hazards.
(III) Control hazard penalties can be eliminated by dynamic branch prediction.

(a) I and II only
(b) I and III only
(c) II and III only
(d) I, II, and III

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2. **Multiple Choice Questions: Type-II**

$3 \times 10 = 30$ **Marks**

(i) Consider a 32 bits hypothetical processor, which supports 4 categories of instruction with 1, 2, 3, and 4 words long, respectively. Program contains 40 instructions of category 1, 30 instructions of category 2, 20 instructions of category 3, and 10 instructions of category 4. How much memory space is required to store the program in bytes?

(a) 1120
(b) 1000
(c) 900
(d) 800

(ii) A hypothetical processor supports a 14 bits address, 22 bits data bus. The CPU is 1 word long and Instruction is designed with 3 memory operands. How many bits are required to encode the instruction?

(a) 60
(b) 64
(c) 80
(d) 84

(iii) Consider a 32 bit hypothetical processor which supports 1 word instruction. Instruction contain opcode, one register operand, and one memory operand. Processor supports 12 registers and 64MB memory. How many number of instructions are possible in CPU

(a) 2
(b) 4
(c) 8
(d) 16

(iv) Which of the following is the reduced form of the boolean function: $F(X,Y,Z) = X'Y + YZ' + YZ + XY'Z'$?

(a) Y+XZ'
(b) X+Y+XZ'
(c) XY+XZ'
(d) Y+X+Z

(v) A 5-stage pipelined processor has Instruction Fetch (IF), Instruction Decode(ID), Operand Fetch(OF), Perform Operation (PO) and Write Operand (WO) stages.The IF, ID ,OF, and WO stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD and SUB instructions, 3 clock cycles for MUL instruction, and 6 clock cycles for DIV instruction, respectively. Operand forwarding is used in the pipeline. The instructions sequence are as follows:

```
I0: MUL R2, R0, R1
I1: DIV R5, R3, R4
I2: ADD R2, R5, R2
I3: SUB R5, R2, R6
```

What is the number of clock cycles needed to execute the following sequence of instructions?

(a) 13
(b) 14
(c) 15
(d) 16

(vi) Consider two processors P_1 and P_2 executing the same instruction set. Assume that under identical conditions, for the same input, a program running on P_2 takes 25% less time but incurs 20% more CPI (clock cycles per instruction) as compared to the program running on P_1. If the clock frequency of P_1 is $1GHz$, What will be the clock frequency of P_2 (in GHz)?

(a) 0.625
(b) 0.95
(c) 1.6
(d) 1.8

(vii) What will be the impact on the clock cycles per instruction (CPI) of stalling on branches. Assume all other instructions have a CPI of 1 and branches occur in every 10^{th} instant out of 100 instances of the time.:

(a) 11.10
(b) 1.10
(c) 10.10
(d) 100.1

(viii) We have 2 designs $D1$ and $D2$ for a synchronous pipeline processor. $D1$ has 4 stage pipeline with execution time of 2 ns, 3 ns, 5 ns, and 1 ns. While the design $D2$ has 6 pipeline stages each with 3 ns execution time. How much time can be saved using design $D2$ over design $D1$ for executing 50 instructions?

(a) 100
(b) 200
(c) 300
(d) 400

(ix) A non-pipelined single cycle processor operating at 100 MHz is converted into a synchronous pipelined processor with five stages requiring 1ns, 1.5ns, 2ns, and 2.5ns, respectively. The delay of due to a latch is 1.5 sec. What will be the speed-up?

(a) 3.33
(b) 3
(c) 2.5
(d) 2

(x) Consider a 3 GHz (gigahertz) processor with a three-stage pipeline and stage latencies τ_1, τ_2, and τ_3 such that $\tau_1 = \frac{3\tau_2}{4} = 2\tau_3$. If the longest pipeline stage is split into **two** pipeline stages of equal latency, what will be new frequency in GHz, ignoring delays in the pipeline registers?

(a) 2
(b) 4
(c) 6
(d) 8

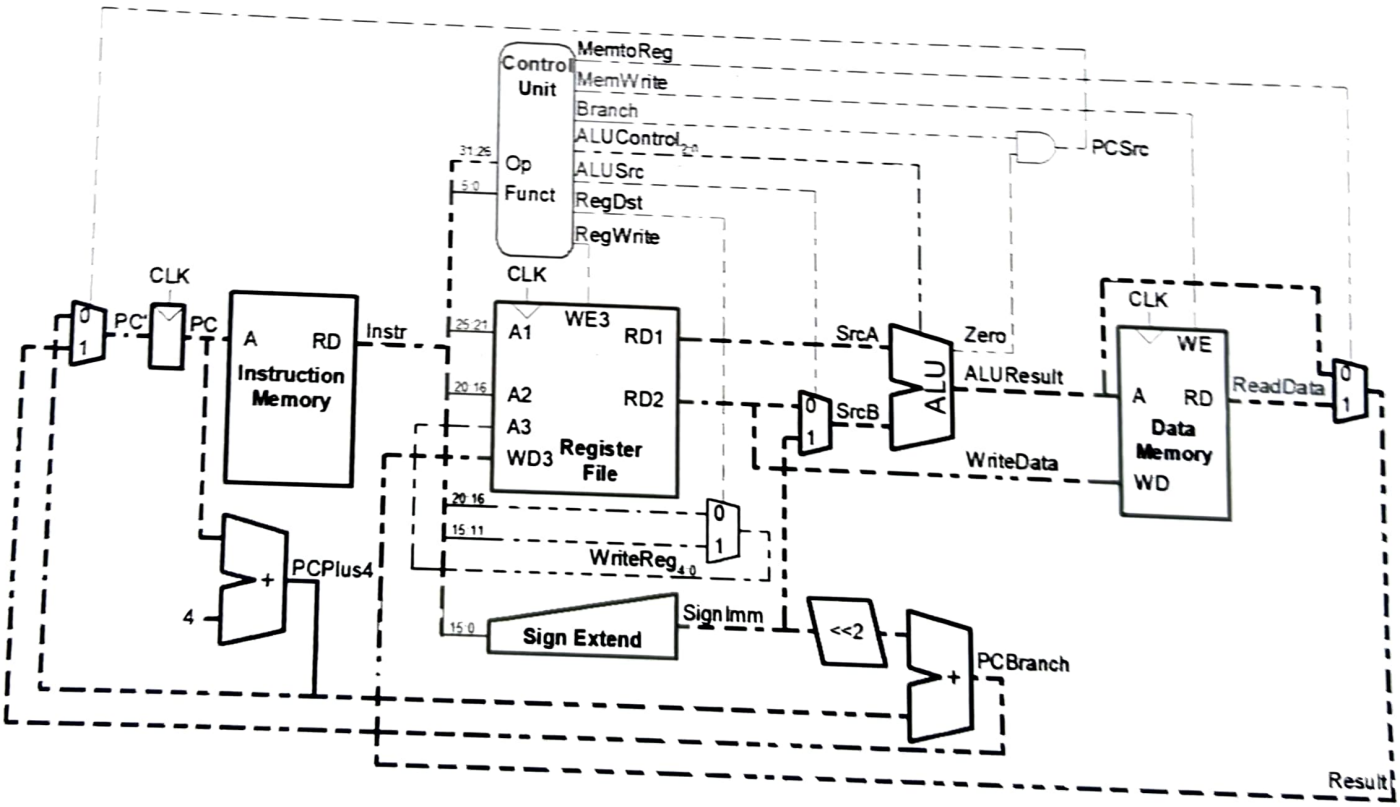
3. Long Answer type Questions

20 Marks

(i) Multiply 5 by 4 using Booth's multiplication algorithm. Use the following information and form a table to perform the multiplication.
M = Multiplicand and Q = Multiplier (No. of bits in $Q = n$), AC initialized with n 0s, Q_{-1} Initialized with 0 and Q_0 LSB of Q
5 Marks

(ii) Explain in details the instruction formats of $R-type$, $I-type$, and $J-type$ instructions for a 32 bit processor. Please include all the fields associated with each of the instructions and mention the number of bits required to represent them.
5 Marks

(iii) The given figure shows an architecture of a single-cycle processor, where the dotted lines indicate the data path and the control path. Trace the required dotted lines to execute a **`lw`** and an **`or`** instructions. Individually, draw the final single-cycle processor architectures for each of these instructions.
5+5 Marks



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