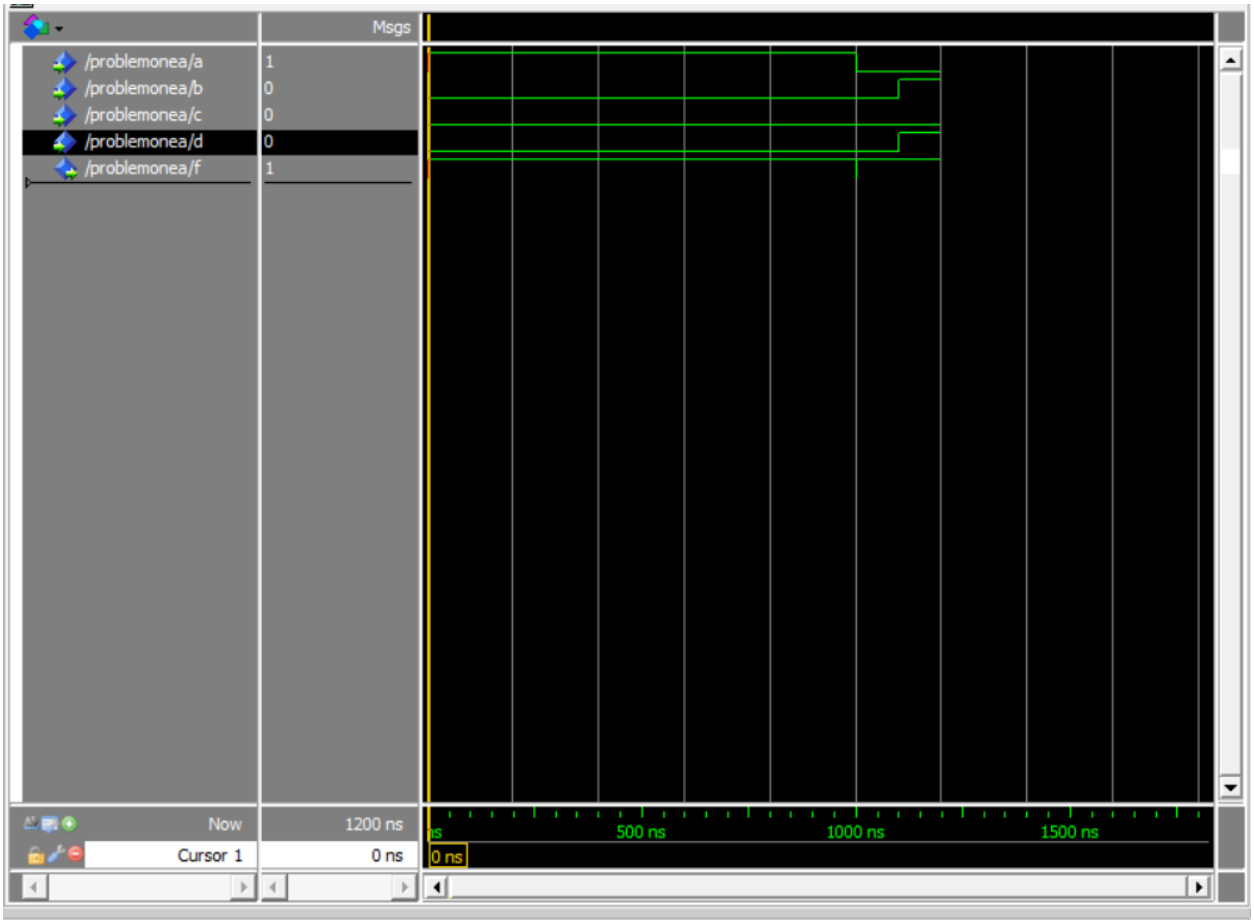
Problem 6.3



Code part A in combinational

```
entity problemoneA is

port (a,b,c,d: in bit;

f:out bit);

end problemoneA;

architecture fiboA of problemoneA is


signal tmpA: bit;

signal tmpB: bit;

signal tmpC: bit;

signal tmpD: bit;
```

```
signal tmpE: bit;
signal tmpF: bit;
signal tmpG: bit;

begin
tmpA<= not b;
tmpB<= not c;
tmpC<= not d;
tmpD<= not a;
tmpE<= a and tmpA and tmpB and tmpC;
tmpF<= tmpD and tmpA;
tmpG<= tmpB and b and d;
F<= tmpE or tmpF or tmpG;
end fiboA;
```

Problem 1 in if else:

```
entity problemoneA is
port (a,b,c,d: in bit;
f:out bit);
end problemoneA;
architecture fiboA of problemoneA is
begin
process (a,b,c,d) begin
if(a<='1' and b<='0' and c<='0' and d<='0') then f<='1';
elsif(a<='0' and b<='0') then f<='1';
elsif(b<='1' and c<='0' and d<='1') then f<='1';
else
f<='0';
```

end if;

end process;

end fiboA;

Problem 2:

Code using case statement:

entity problemtwoA is

port(A: in bit_vector(3 downto 0);

output: out bit);

end;

architecture twoA of problemtwoA is

begin

process(A)

begin

case A is

when"0011"=>

```
output<='1';
when"0110"=>
output<='1';
when"1001"=>
output<='1';
when"1100"=>
output<='1';
when"1111"=>
output<='1';
when others=>
output<='1';
end case;
end process;
end;
```

Code using digital

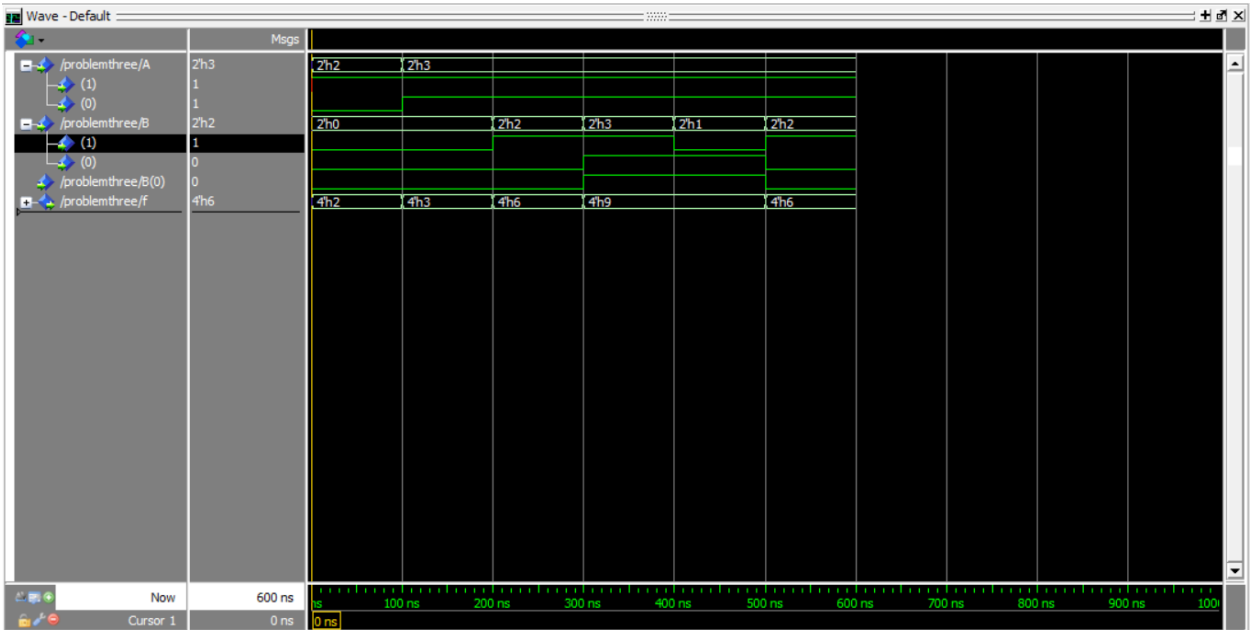
```
entity problemtwoA is
port(input: in bit_vector(3 downto 0);
output: out bit);

end;

architecture twoA of problemtwoA is
begin
output<= (input(0) AND input(1) AND (NOT input(3))) OR
        ( input(3) AND input(2) AND (NOT input(1)) AND (NOT input(0))) OR
```

(input(0) AND (NOT input(2)) AND input(3)) OR

(input(0) AND input(1) AND input(3)) ;

end twoA;

Problem 3:



Using a case statement

entity problemthree is

port(A: in bit_vector(1 downto 0);

B: in bit_vector(1 downto 0);

f: out bit_vector(3 downto 0));

end problemthree;

architecture problemthreeB of problemthree is

begin

process(A,B)

begin

```
case (a,b)
when a="00"and b="00"
output<="0000"
when a="01"and b="00"
output<="0001"
when a="10"and b="00"
output<="0010"
when a="00"and b="10"
output<="0010"
when a="11"and b="00"
output<="0011"
when a="00"and b="11"
output<="0011"
when a="11"and b="11"
output<="1001"
when others=>
output<="0000"
end case;
end process;

end;
```

using when else

```
entity problemthree is
port(A: in bit_vector(1 downto 0);
B: in bit_vector(1 downto 0);
f: out bit_vector(3 downto 0));
end problemthree;
```

```
architecture problemthreeA of problemthree is

begin
f<= "0000" when a="00" and b="00" else
"0001" when a="00" and b="01" else
"0001" when a="01" and b="00" else
"0010" when a="10" and b="00" else
"0010" when a="00" and b="10" else
"0011" when a="11" and b="00" else
"0011" when a="00" and b="11" else
"0110" when a="11" and b="10" else
"0110" when a="10" and b="11" else
"0100" when a="10" and b="10" else
"1001" when a="11" and b="11";

end;
```