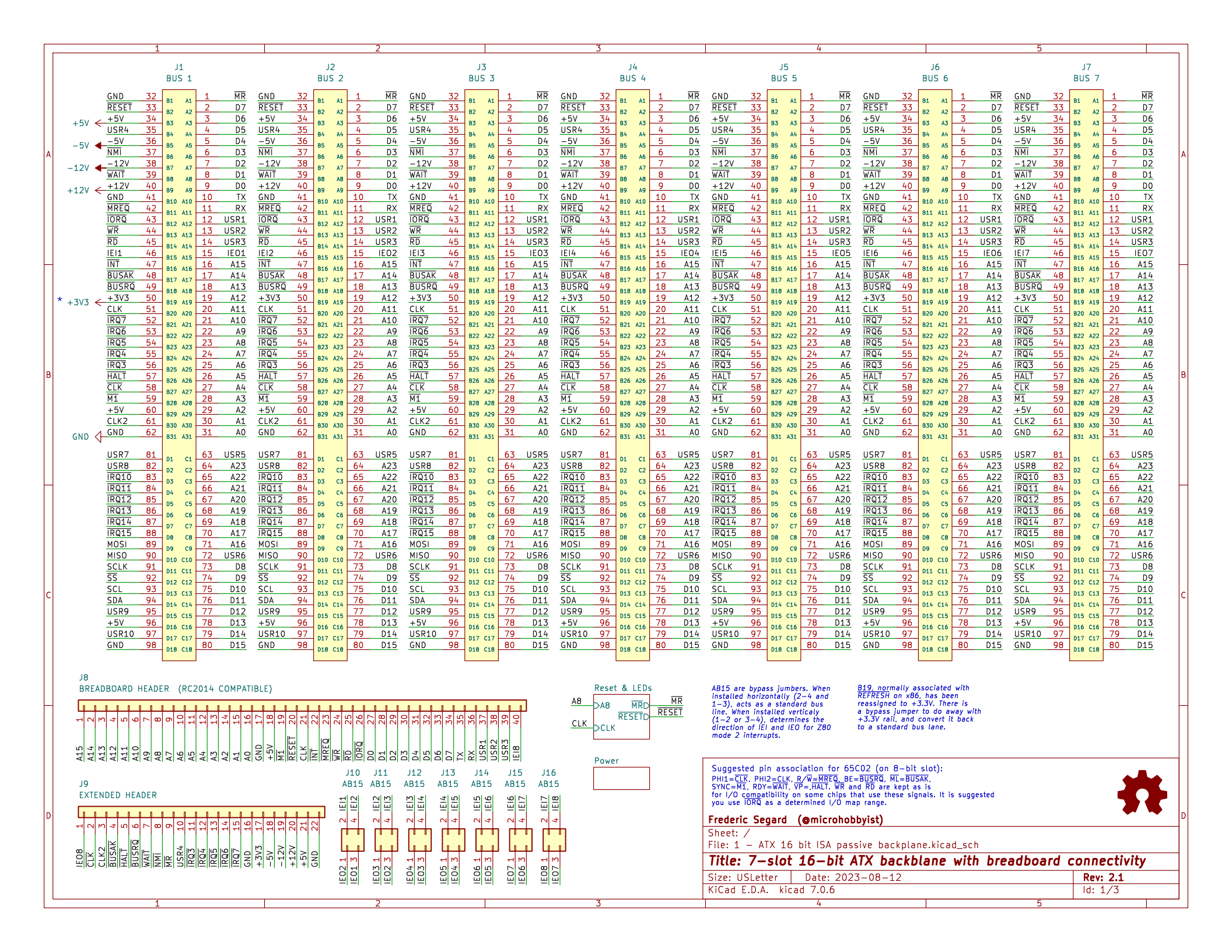
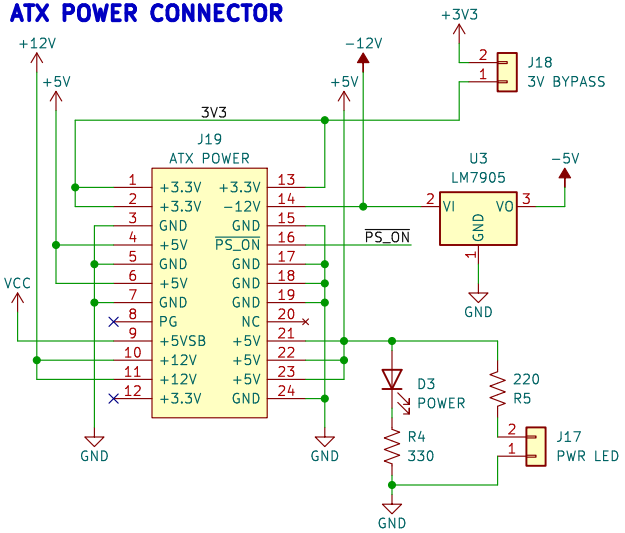
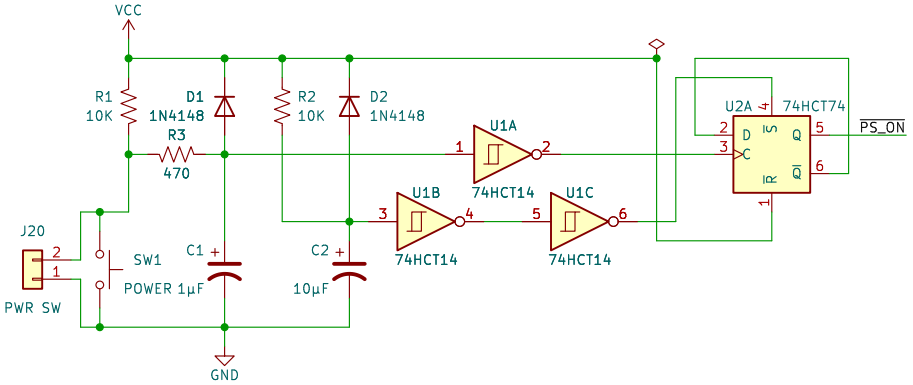

J1
BUS 1
J2
BUS 2
J3
BUS 3
J4
BUS 4
J5
BUS 5
J6
BUS 6
J7
BUS 7
+5V
-5V
-12V
+12V
* +3V3
GND
J8
BREADBOARD HEADER (RC2014 COMPATIBLE)
J9
EXTENDED HEADER
J10 AB15
J11 AB15
J12 AB15
J13 AB15
J14 AB15
J15 AB15
J16 AB15
Reset & LEDs
A8
CLK
MRD
RESET
Power
AB15 are bypass jumbers. When installed horizontally (2–4 and 1–3), acts as a standard bus line. When installed verticaly (1–2 or 3–4), determines the direction of IEI and IEO for Z80 mode 2 interrupts.
B19, normally associated with REFRESH on x86, has been reassigned to +3.3V. There is a bypass jumper to do away with +3.3V rail, and convert it back to a standard bus lane.
Suggested pin association for 65C02 (on 8–bit slot):
PHI1=CLK, PHI2=CLK, R/W=MREQ, BE=BUSRQ, ML=BUSAK,
SYNC=M1, RDY=WAIT, VP=,HALT. WR and RD are kept as is
for I/O compatibility on some chips that use these signals. It is suggested
you use IORQ as a determined I/O map range.
Frederic Segard (@microhobbyist)
Sheet: /
File: 1 – ATX 16 bit ISA passive backplane.kicad_sch
Title: 7–slot 16–bit ATX backblane with breadboard connectivity
Size: USLetter
Date: 2023–08–12
Rev: 2.1
KiCad E.D.A. kicad 7.0.6
Id: 1/3

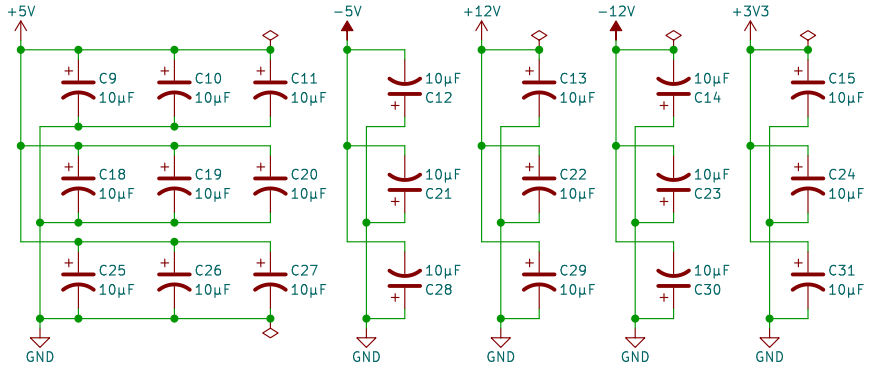
ATX POWER CONNECTOR

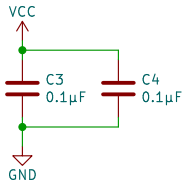


ATX POWER ON CIRCUIT



BYPASS CAPACITORS

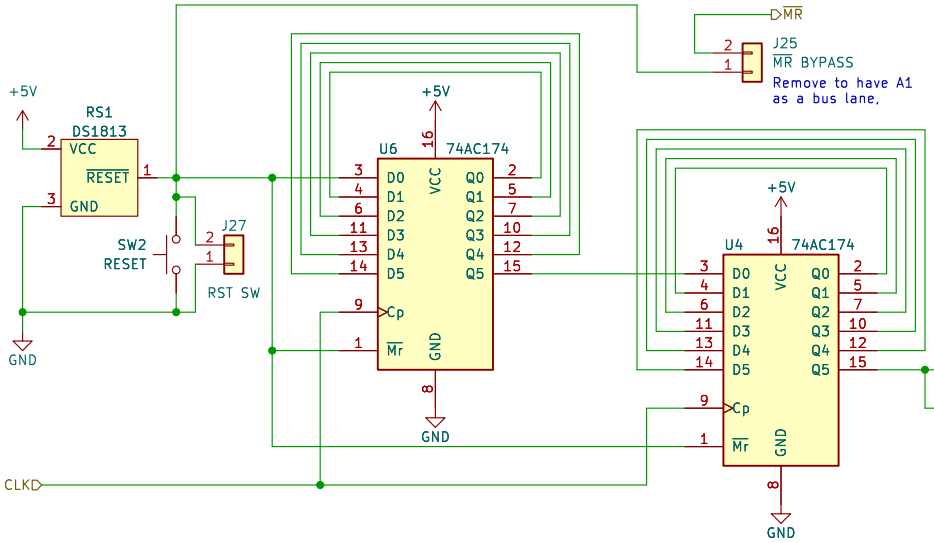


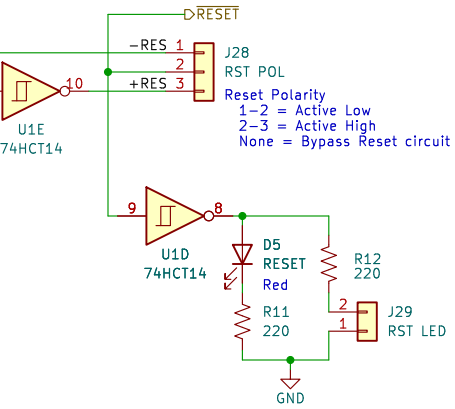


Frederic Segard (@microhobbyist)	
Sheet: /Power/	
File: SoftPower.kicad_sch	
Title:	
Size: USLetter | Date: 2023-08-12	**Rev: 2.1**
KiCad E.D.A. kicad 7.0.6	Id: 2/3

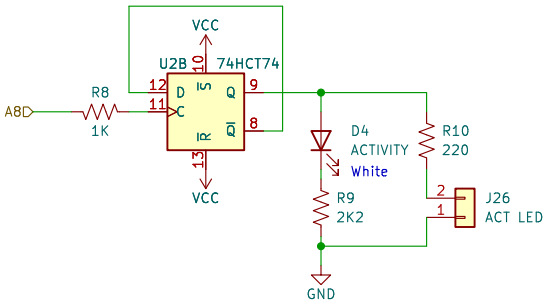
RESET CIRCUIT

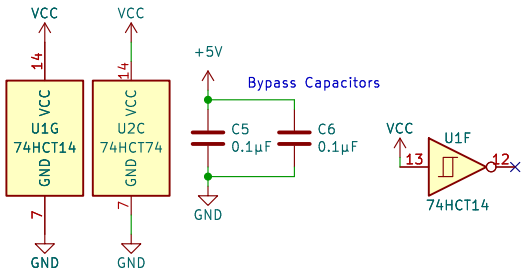
The DS1813 maintains reset for 150ms after stabalized power, or reset button has been pressed. Wheras the 74174 further delays reset by 12 clock cycles. Specs for some devices require reset to be maintained for a certain number of clocks after reset. For example, VT8242 is 10.

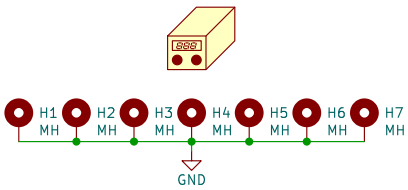




CPU ACTIVITY







Frederic Segard (@microhobbyist)	
Sheet: /Reset & LEDs/	
File: ResetCircuit.kicad_sch	
Title:	
Size: USLetter	Date: 2023-08-12
KiCad E.D.A. kicad 7.0.6	Id: 3/3

Rev: 2.1