

Frédéric Segard

MicroHobbyist

Sheet: /CPU/

File: CPU.sch

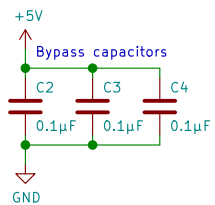
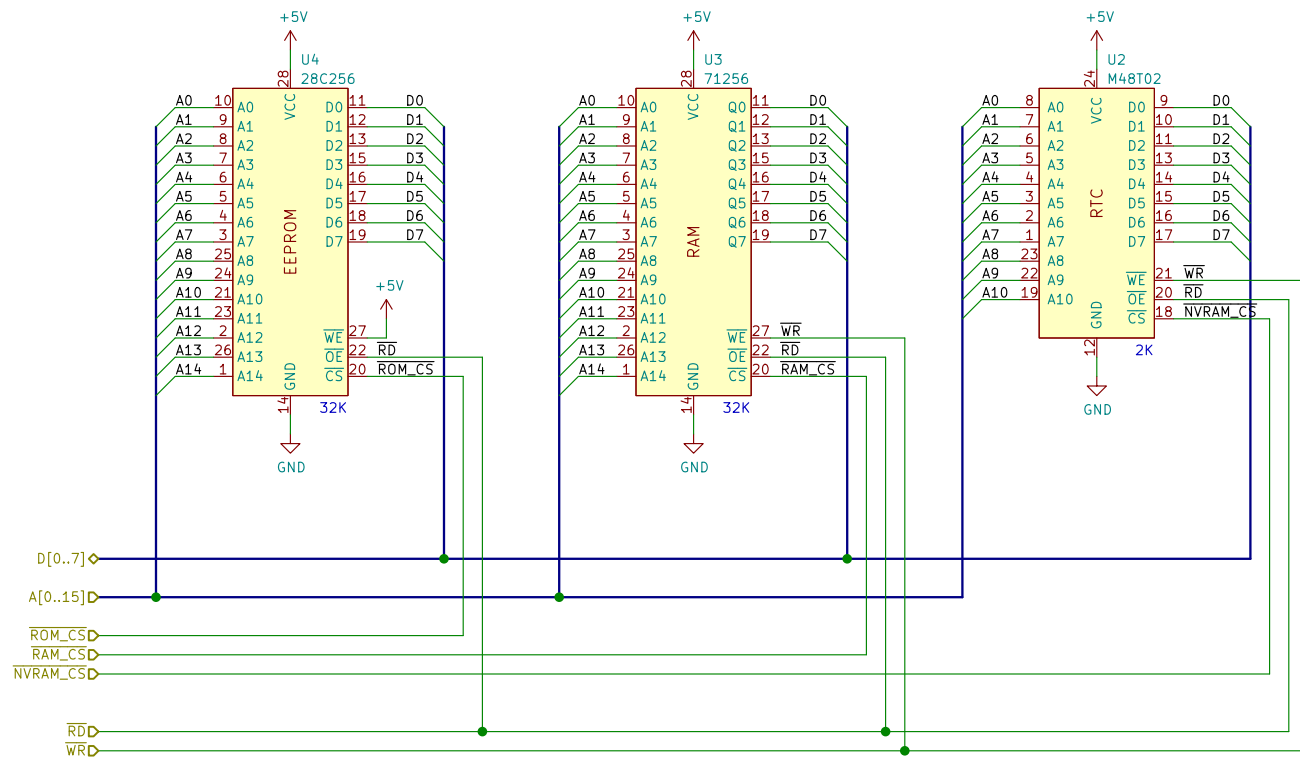
Title: CPU

Size: USLetter Date: 2022-06-02

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Rev: 4.1

Id: 2/11



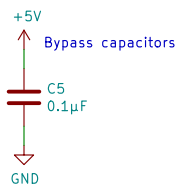
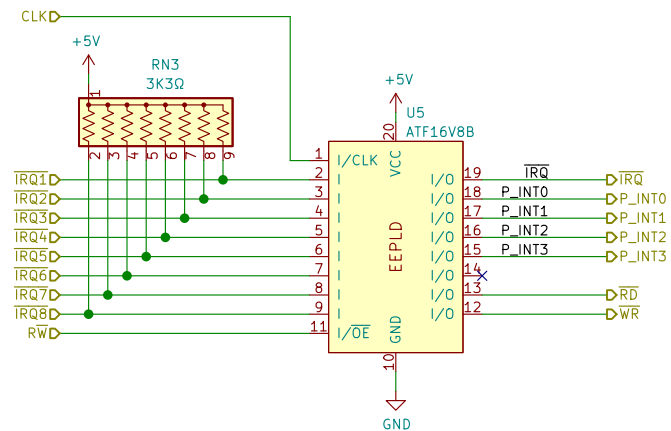
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Sheet: /Memory/
File: Memory.sch

Title: Memory: ROM, RAM, Bank RAM, and NVRAM with RTC

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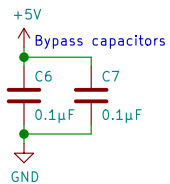
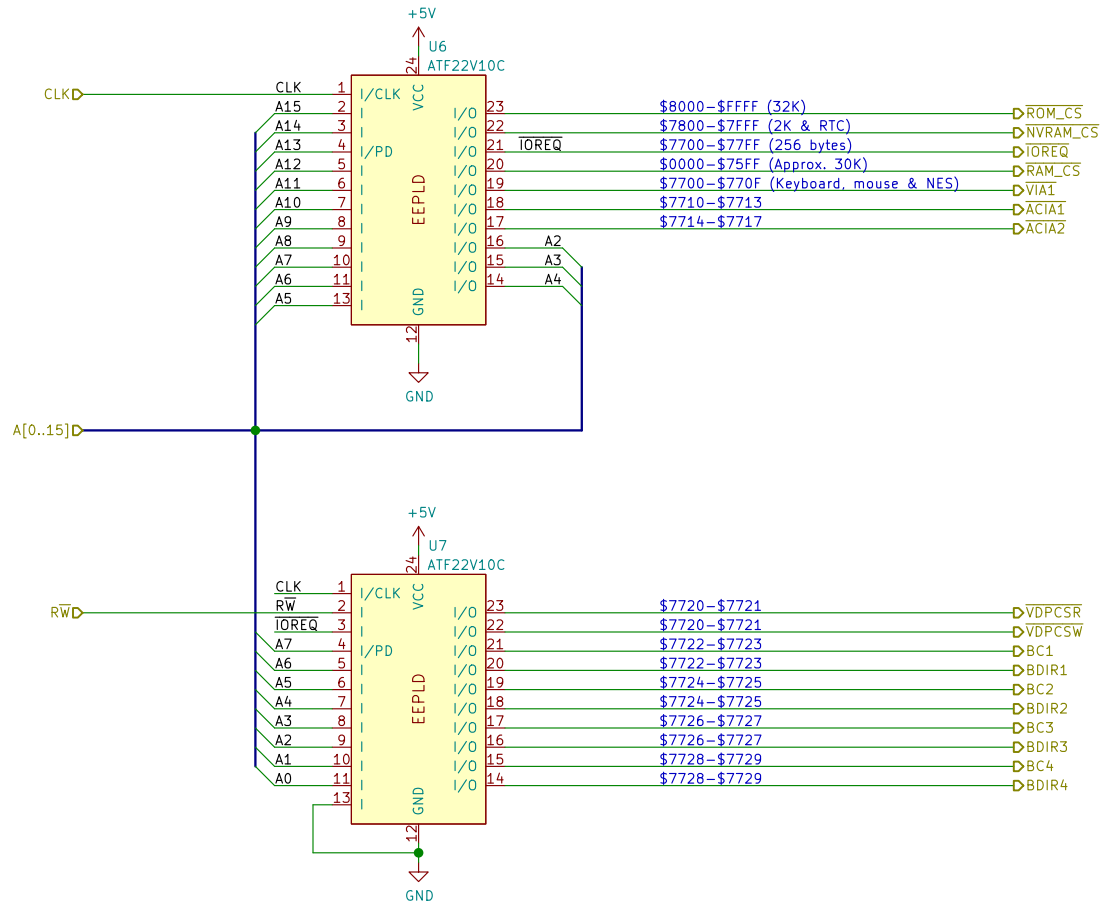
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Sheet: /Interrupt/
File: Interrupts.sch

Title: Interrupt Priority Handler and Config DIP seitches

Size: USLetter Date: 2022-06-02
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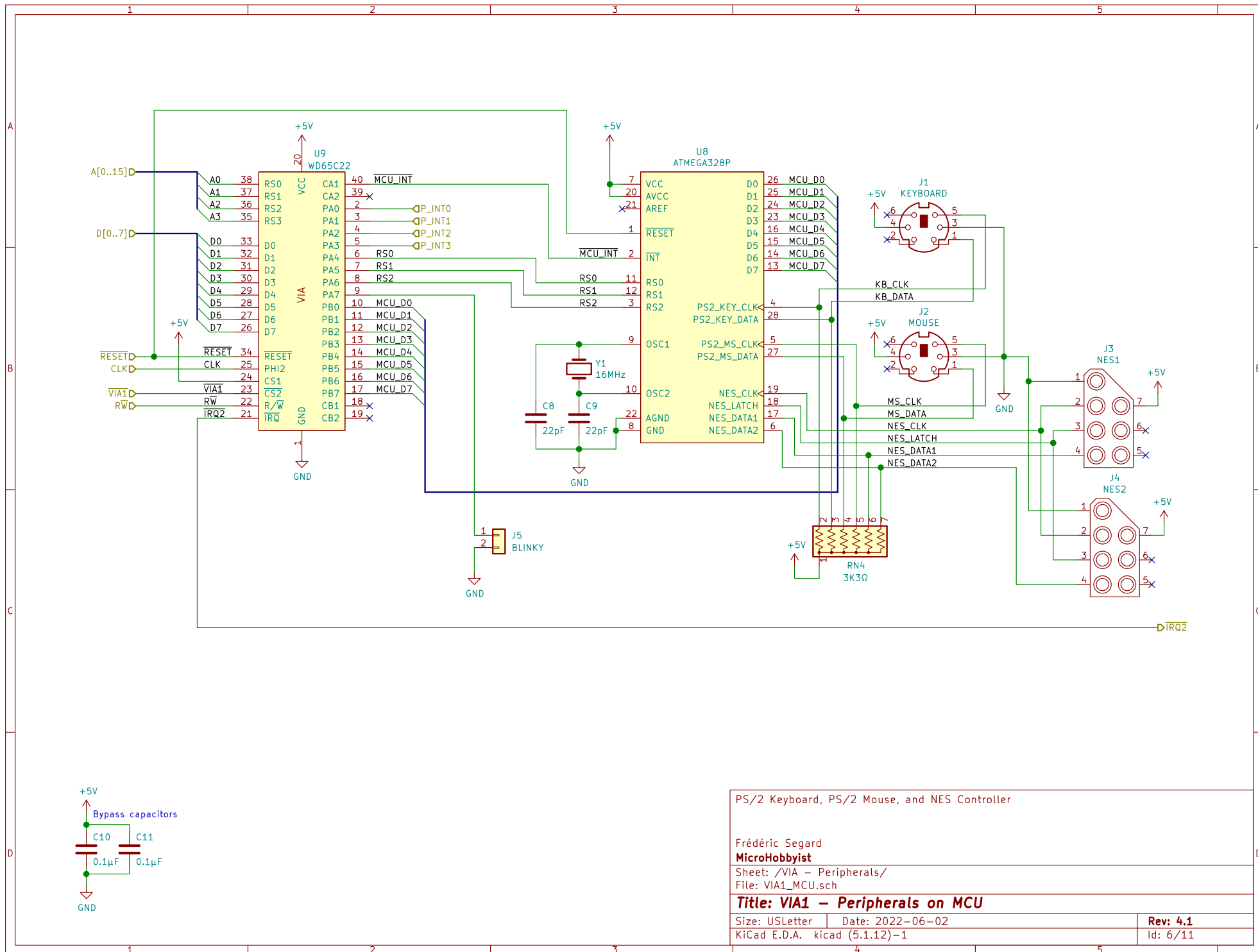
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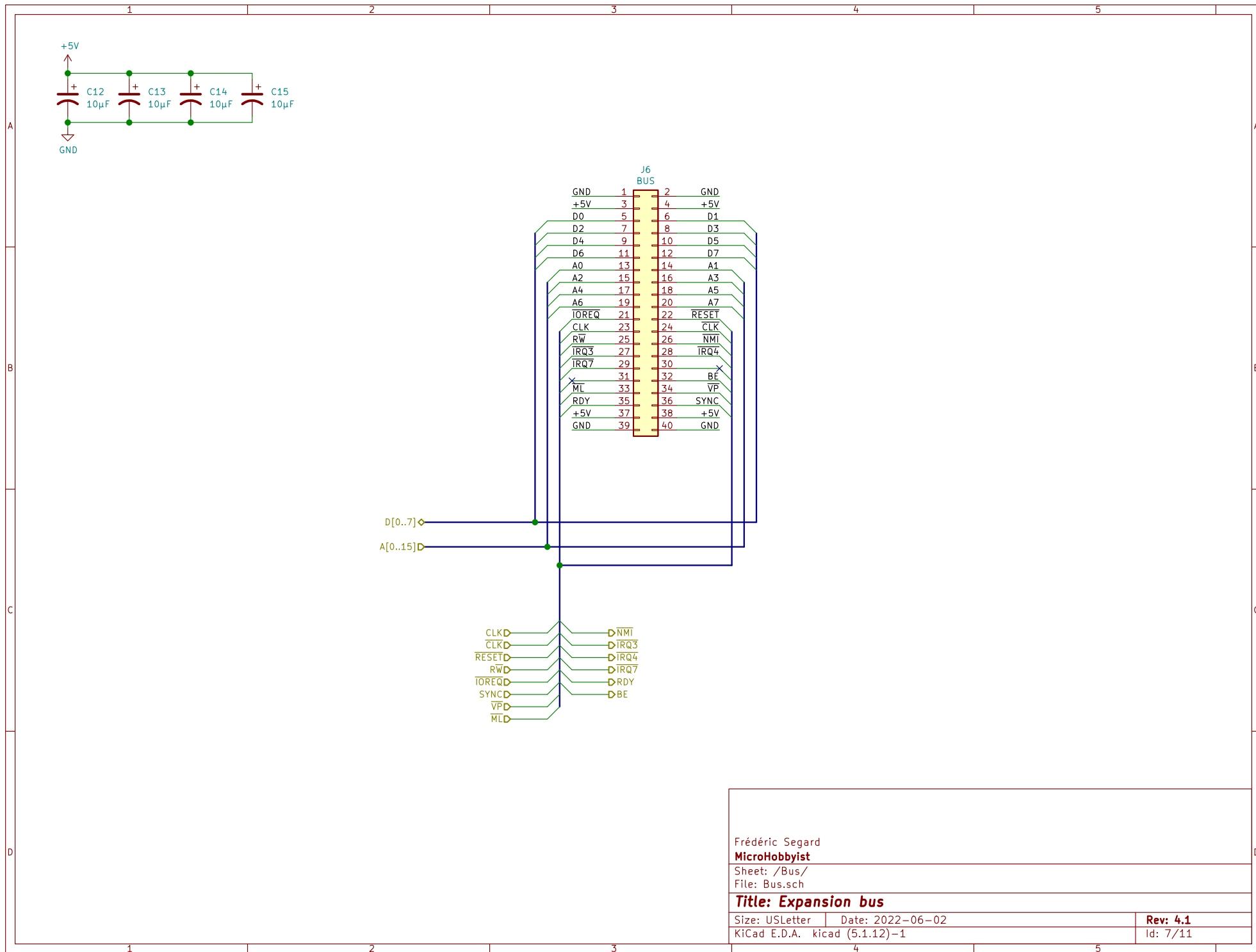
Sheet: /Logic Decode/
File: MemoryMap.sch

Title: Memory Map Decoding

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Sheet: /Bus/

File: Bus.sch

Title: Expansion bus

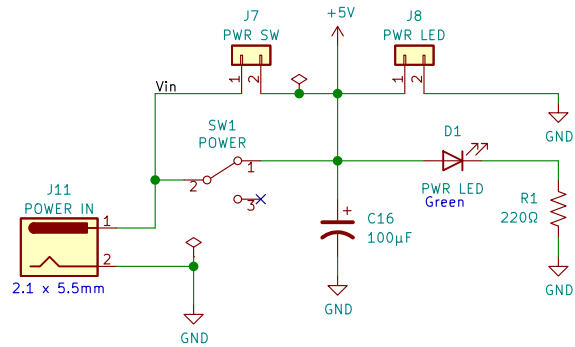
Size: USLetter | Date: 2022-06-02

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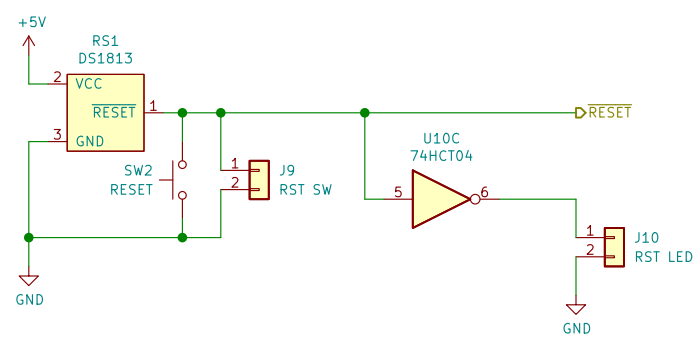
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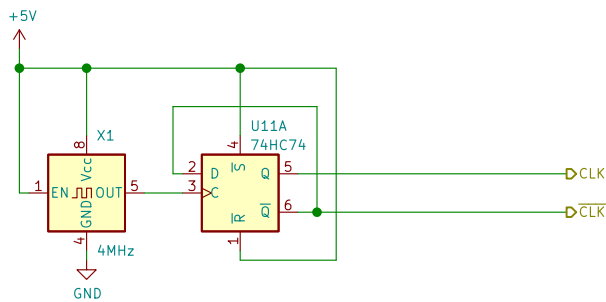
POWER



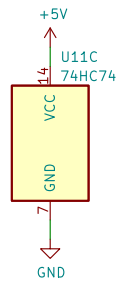
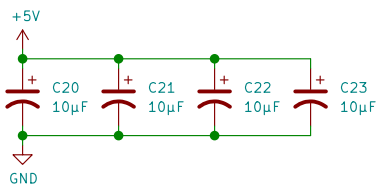
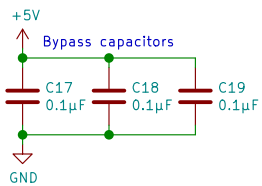
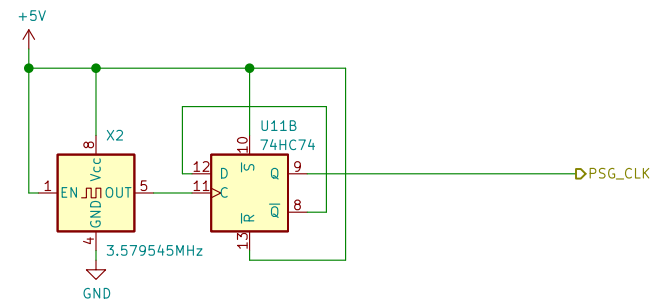
RESET



CPU CLOCK



PSG CLOCK



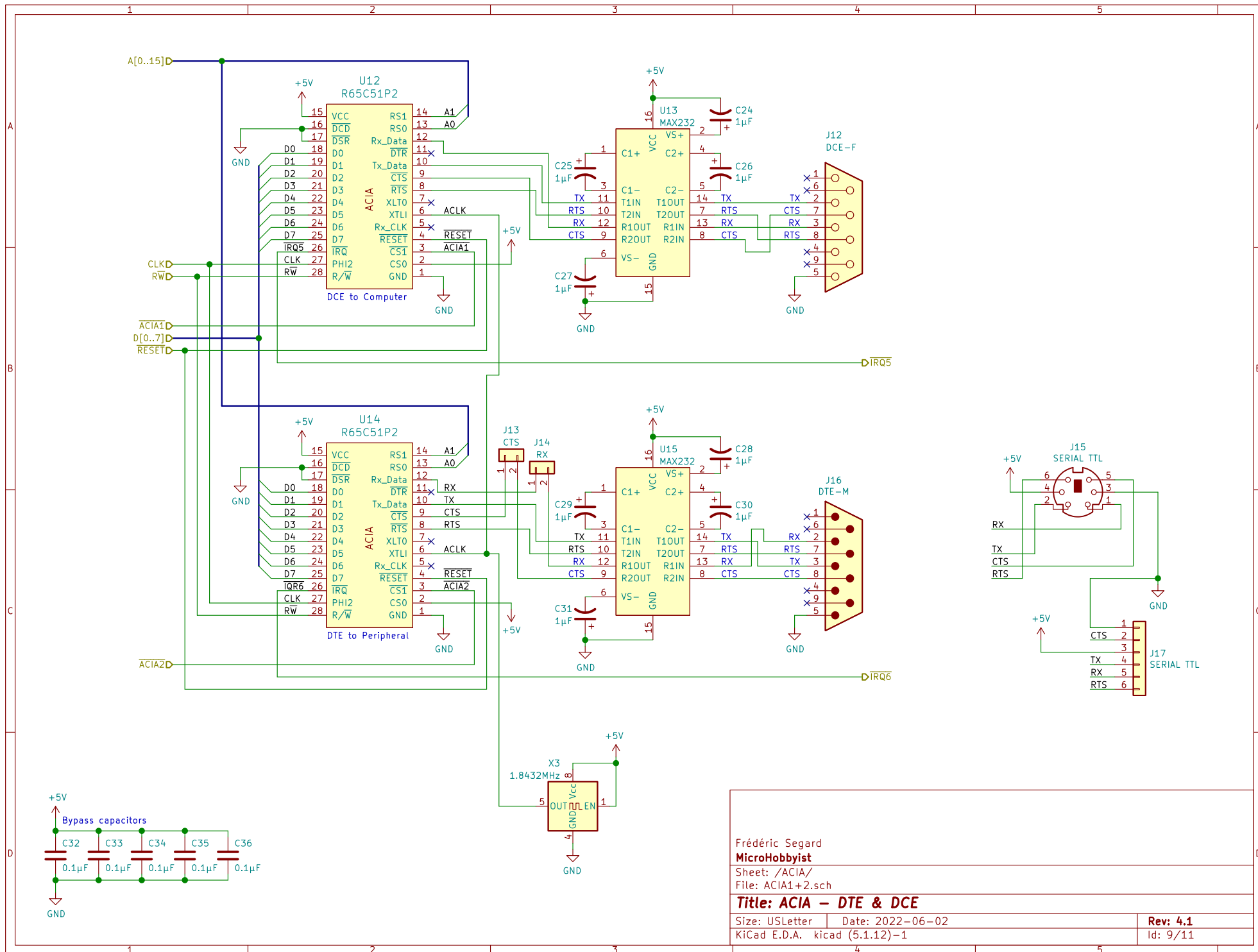
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Sheet: /Power, Reset & Clock/
File: PowerReset.sch

Title: Power and Reset

Size: USLetter Date: 2022-06-02
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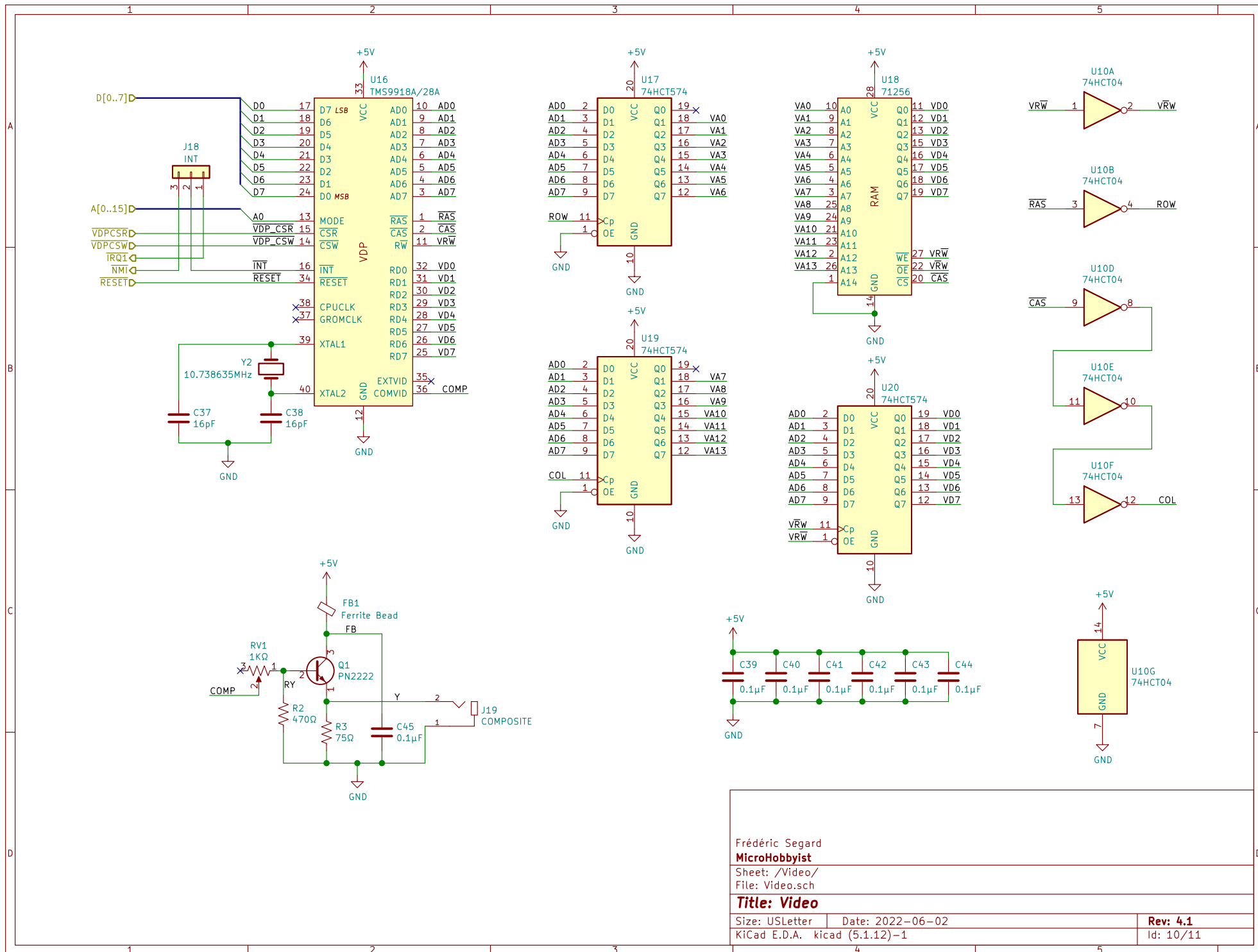
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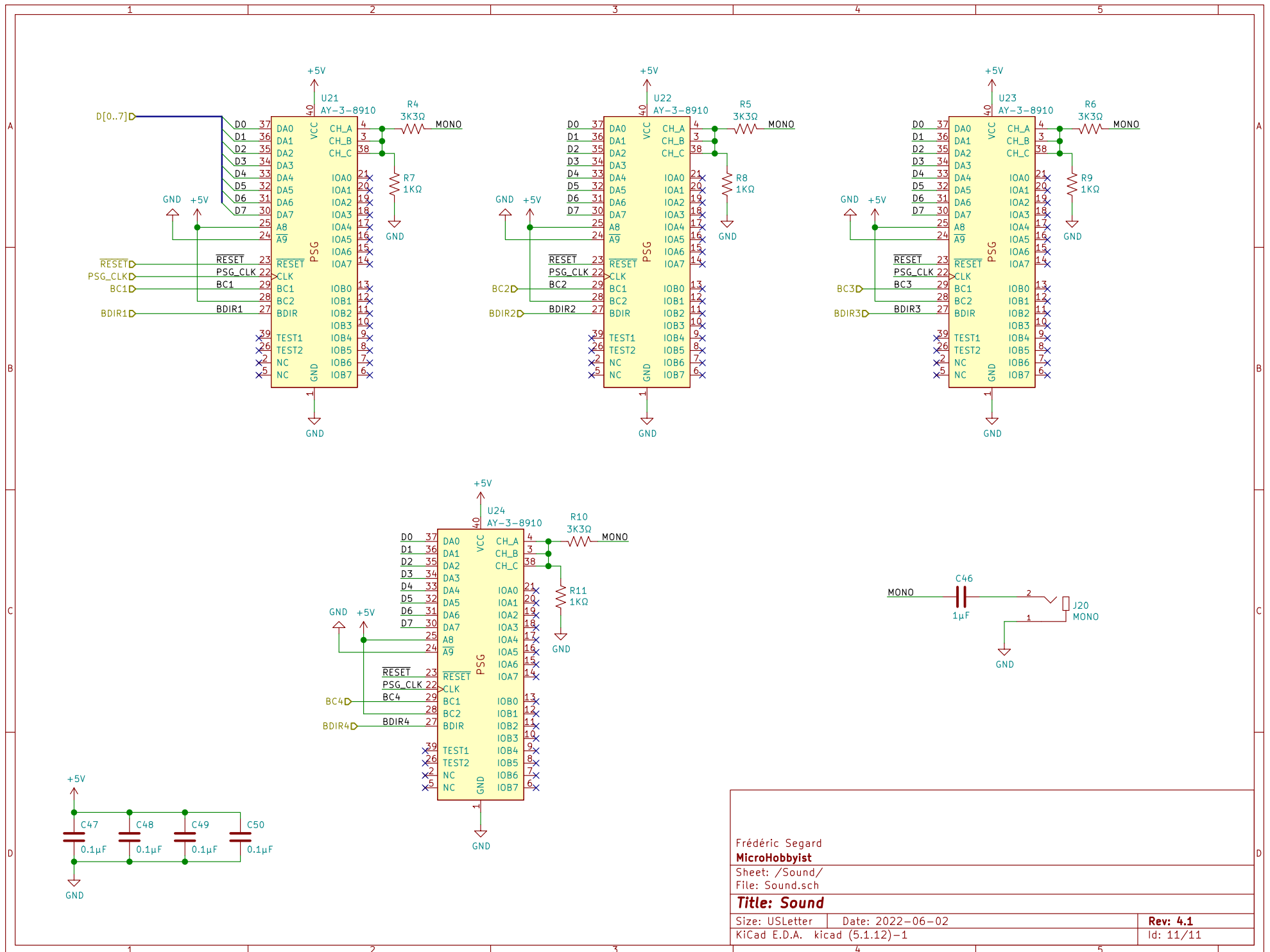
Sheet: /ACIA/
File: ACIA1+2.sch

Title: ACIA - DTE & DCE

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Sheet: /Sound/
File: Sound.sch

Title: Sound

Size: USLetter Date: 2022-06-02
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Rev: 4.1
Id: 11/11