

The Bipolar Junction Transistor

7.5 DC LOAD LINE OF CE CONFIGURATION:

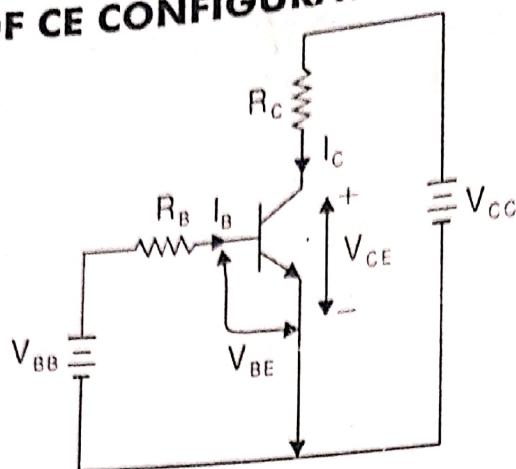


Fig. 7.16

Applying KVL in output circuit of transistor,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\therefore V_{CE} = V_{CC} - I_C R_C \quad \dots (1)$$

Case 1: Assuming transistor is Off

$$\therefore I_C \approx 0$$

Putting this in eqn. (1)

We get

$$V_{CE} = V_{CC}$$

Case 2: Assuming transistor is conducting at the maximum level such that $V_{CE} = 0$.

Putting this value in eqn. (1) we get,

$$0 = V_{CC} - I_C R_C$$

$$I_C = \frac{V_{CC}}{R_C}$$

That is maximum collector current that can flow through transistor is $\frac{V_{CC}}{R_C}$.

So here we get two points:

$$(1) \quad V_{CE} = V_{CC}$$

$$(2) \quad I_C = \frac{V_{CC}}{R_C}$$

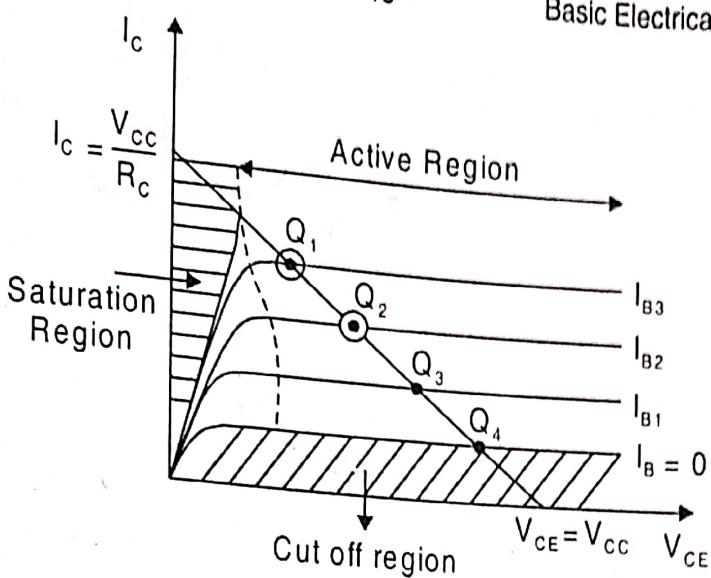


Fig. 7.17

Q_1, Q_2, Q_3 and Q_4 are called Quiescent or operating point.

It is the point on the load line which represents the dc current through the transistor (I_{CQ}) and the voltage across it (V_{CEO}) when no ac signal is applied.

In short, it represents the dc biasing condition.

7.5.1 SELECTION OF OPERATING POINT:

As we know that transistor works as an amplifier in the active region, but then question arises where the Q point of the transistor should be located? Consider the 3 different cases;

(1) Operating point near the cut off region:

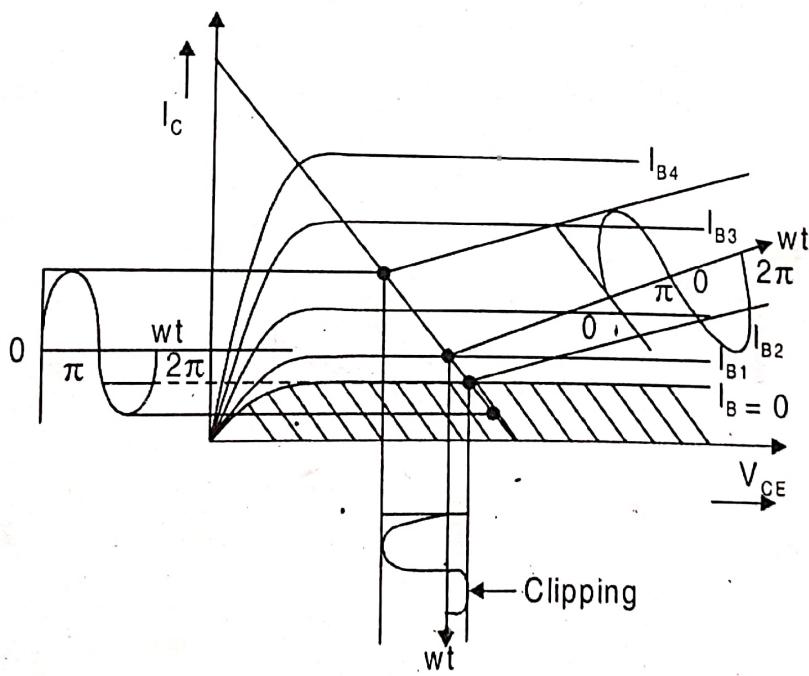


Fig. 7.18

As shown in the Fig. 7.18 if the Q point is near the cut off region then for some portion of the negative half cycle of the input signal, the Q point of transistor goes into cut off region. Therefore, collector current gets clipped at the negative half cycle. Hence, at the output some portion of negative half cycle of amplified signal gets clipped.

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(2) Q point near saturation region:

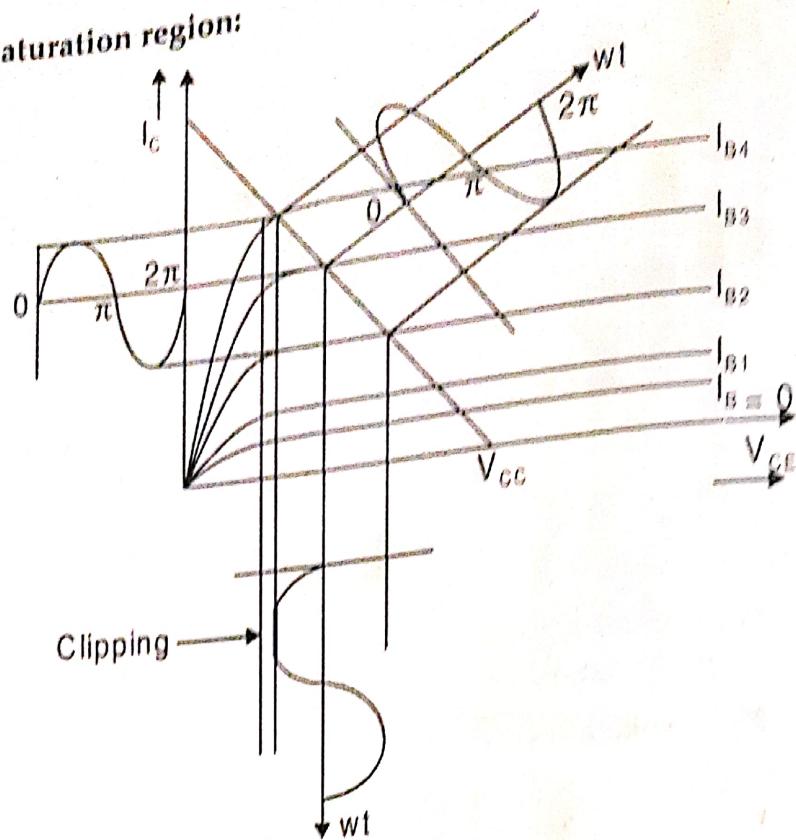


Fig. 7.19

If the Q point is near the saturation region, then during some portion of the positive half cycle, Q point goes into saturation region. Hence, collector current gets clipped. Therefore the output is distorted.

(3) Q point is at the centre of load line:

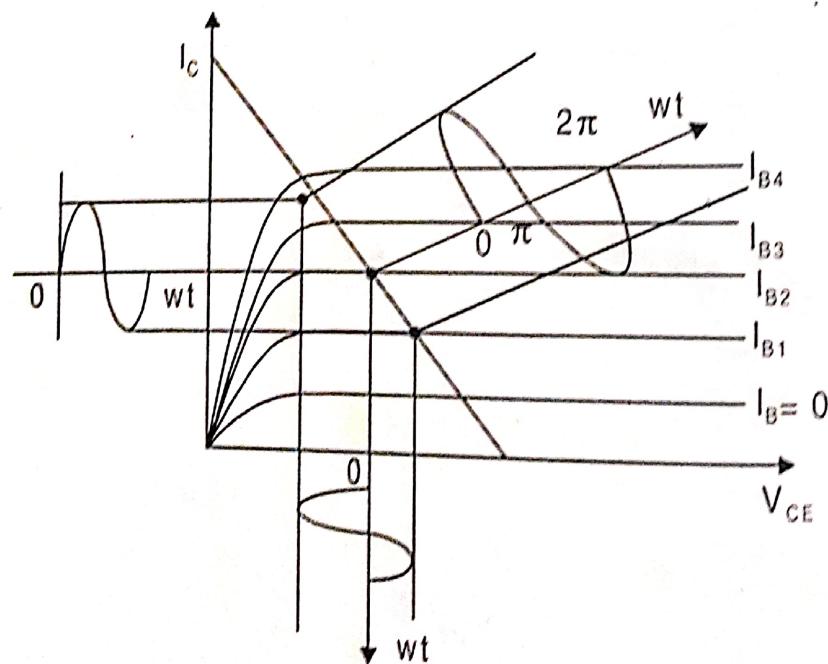


Fig. 7.20

If the Q point of the transistor is situated exactly at the centre of the load line. Then transistor works like a perfect amplifier. If the input signal varies sinusoidally, then output also varies sinusoidally. It means we do not get distortion.

Thus, for transistor to work like a voltage amplifier, Q point of the transistor must be situated exactly at the centre of load line. And to establish Q point at the centre of load line, we connect some external resistances with dc power supply. This circuit is known as Biasing Circuit.

Thus biasing is the process of establishing Q point of the transistor exactly at the centre of Load Line.

But change in temperature, change in β factor, affect Q point. Because of this operating point shift upward or downward on load line. That is Q point is shifted near saturation or cut off and we get distorted output so to avoid this or to stabilized Q point we use biasing circuit.

7.6 TRANSISTOR BIASING CIRCUITS:

The following are the most commonly used methods of obtaining transistor biasing from one source of supply (i.e. V_{CC}).

- (1) Base resistor method (Fixed bias)
- (2) Biasing with feedback resistor.
- (3) Voltage divider bias.

7.6.1 BASE RESISTOR METHOD:

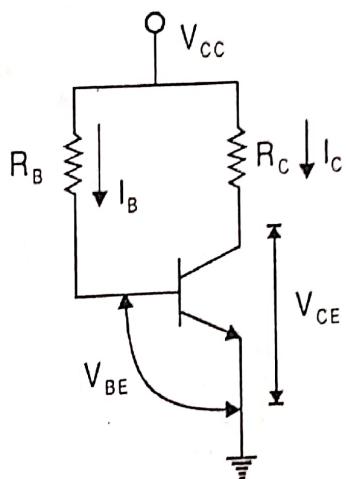


Fig. 7.21

(1) In this method, a high resistance R_B is connected between the base and +ve end of supply for n-p-n transistor.

Circuit analysis:

- (1) It is required to find the value of R_B so that required collector current flows in the zero signal conditions.
- (2) Let I_C be the required zero signal collector current.

$$I_B = \frac{I_C}{\beta}$$

- (3) Applying KVL to input side, we get,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} \quad \dots (1)$$

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- (4) As V_{CC} and I_B are known and $V_{BE} = 0.7$ for silicon, 0.4 for Germanium therefore, value of β can be easily get.
- (5) From eqn. (1), V_{CC} is fixed known quantity and I_B is chosen at some suitable value. Hence, R_B can always found directly, and for this reason, this method is sometimes called fixed bias method.

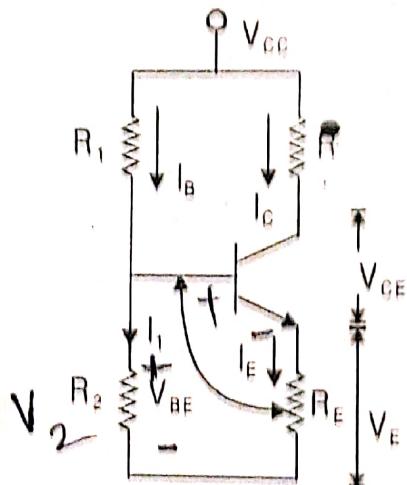
Advantages:

- (1) This circuit is very simple as only one resistance R_B is required.
- (2) Biasing conditions can easily be set and the calculations are simple.

Disadvantages:

- (1) This method provides poor stabilization. It is because there is no means to stop a self increase in collector current due to temperature rise and individual variation. For example, if β increases due to transistor replacement, then I_C also increases by the same factor as I_B is constant.
- (2) The stability factor is very high. Therefore, there are strong chances of thermal runaway.

7.6.2 VOLTAGE DIVIDER BIAS METHOD:



$$V_2 = V_{BE} + I_E R_E$$

Fig. 7.22

- (1) This is the most widely used method of providing biasing and stabilisation to a transistor.
- (2) In this method, two resistances R_1 and R_2 are connected across the supply voltage V_{CC} , and provide biasing.
- (3) The emitter resistance R_E provides stabilisation.
- (4) The name "voltage divider" comes from the voltage divider formed by R_1 and R_2 .
- (5) The voltage drop across R_2 forward biases the base-emitter junction.
- (6) This causes the base current and hence collector current flow in the zero signal conditions.

Circuit analysis:

- (1) Suppose current flowing through resistance R_1 is I_1 .
- (2) As base current is very small, we assume current flowing through R_2 is also I_1 .

$$(3) \quad I_1 = \frac{V_{CC}}{R_1 + R_2}$$

\therefore Voltage across resistance R_2 is,

$$V_2 = I_1 R_2$$

$$V_2 = \left(\frac{V_{CC}}{R_1 + R_2} \right) R_2$$

Applying KVL to base circuit.

$$V_2 = V_{BE} + V_E$$

$$V_2 = V_{BE} + I_E R_E$$

$$\therefore I_E = \frac{V_2 - V_{BE}}{R_E}$$

Since $I_E \approx I_C$

$$I_C = \frac{V_2 - V_{BE}}{R_E}$$

- (4) From above equation it is clear that I_C does not at all depend upon β .
- (5) Though I_C depends upon V_{BE} but in practice $V_2 \gg V_{BE}$ so that I_C is practically independent of V_{BE} .
- (6) Thus I_C in the circuit is almost independent of transistor parameter and hence good stabilisation is ensured.
- (7) Collector - emitter voltage (V_{CE}):

Applying KVL to the collector side,

$$\begin{aligned} V_{CC} &= I_C R_C + V_{CE} + I_E R_E \\ &= I_C R_C + V_{CE} + I_C R_E \\ &= I_C (R_C + R_E) + V_{CE} \\ V_{CE} &= V_{CC} - I_C (R_C + R_E) \end{aligned}$$

PROBLEMS:

(DEC. 98)

7.7 TRANSISTOR AS AN AMPLIFIER:

An amplifier is an electronic circuit that amplifies (magnifies) small input signal without any distortion.

An amplifier is used to raise the level of input signal.

7.7.1 HOW TRANSISTOR AMPLIFIES?

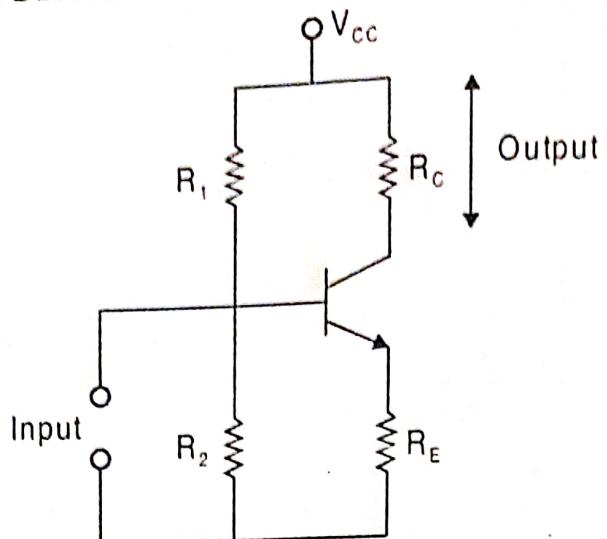


Fig. 7.34

- (1) When a weak ac signal is given to the base of transistor, a small base current (which is ac) starts flowing.
- (2) Due to transistor action, a much larger (β times the base current) ac current flows through the collector load R_C .
- (3) As the value of R_C is quite high (usually $4 - 10 \text{ k}\Omega$), therefore, a large voltage appears across R_C .
- (4) Thus, a weak signal applied in the base circuit appears in amplified form in the collector circuit.

In this way transistor acts as an amplifier.

7.7.2 PRACTICAL CIRCUIT OF TRANSISTOR AMPLIFIER:

Transistor can accomplish faithful amplification if proper associated circuitry is used.
Circuit diagram:

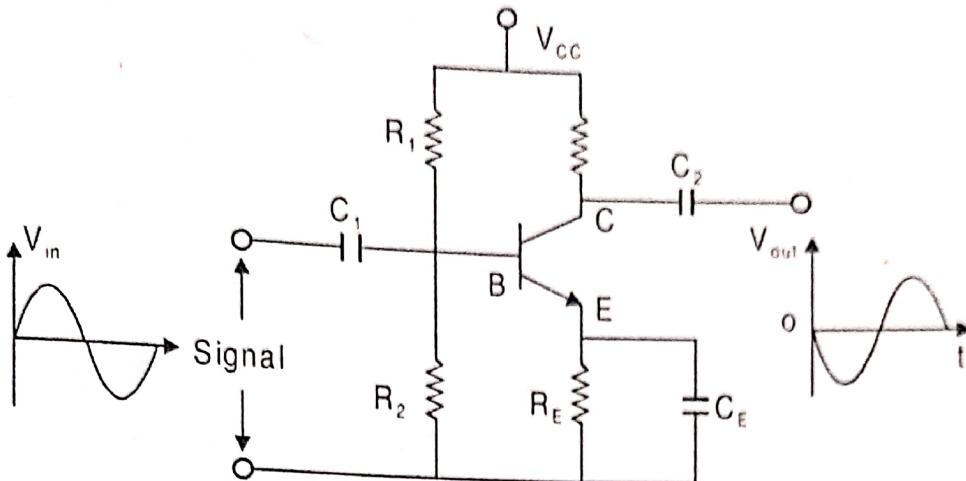


Fig. 7.35

- (1) **Biassing circuit:** The resistance R_1 , R_2 and R_E form the biassing and stabilisation circuit. Biassing circuit provides proper operating point.
- (2) **Input capacitor (C_{in}):** This is used to couple the signal to the base of the transistor. If it is not used, signal source resistance will come across R_2 and thus change the bias. The capacitor C_{in} allows only ac signal to flow but isolates the signal source from R_2 .
- (3) **Emitter bypass capacitor (C_E):** This capacitor is used in parallel with R_E to provide a low reactance path to amplified ac signal. If it is not used, then amplified ac signal flowing through R_E will cause a voltage drop across it, thereby reducing the output voltage.
- (4) **Coupling capacitor (C_C):** This capacitor couples one stage of amplification to the next stage. If it is not used, the bias conditions of the next stage will be drastically changed due to the shunting effect of R_C . This is because R_C will come in parallel with the upper resistance R_1 of the biassing network of the next stage, thereby altering the biassing conditions of the latter. That is the coupling capacitor C_C isolates the dc of one stage from the next stage but allows the passage of ac signal.

7.7.3 PHASE REVERSAL:

- (1) In common emitter connection when the input signal voltage increases in the positive sense, the output voltage increases in the negative direction and vice versa.
- (2) There is a phase difference of 180° between the input and output voltage in CE connection.
- (3) The total output voltage V_{CE} is given by, (from Fig. 7.35)

$$V_{CE} = V_{CC} - I_C R_C$$
- (4) When the signal voltage increases in the positive half cycle, the base current also increases. Therefore, collector current and hence voltage drop $I_C R_C$ increases.
- (5) As V_{CC} is constant, output voltage V_{CE} decreases.
- (6) In other words, as the signal voltage is increasing in the positive half cycle, the output voltage is increasing in the negative sense i.e. output is 180° out of phase with the input.

- (7) Therefore in a common emitter amplifier, the positive half cycle of the signal appears as amplified negative half cycle in the output and vice versa.

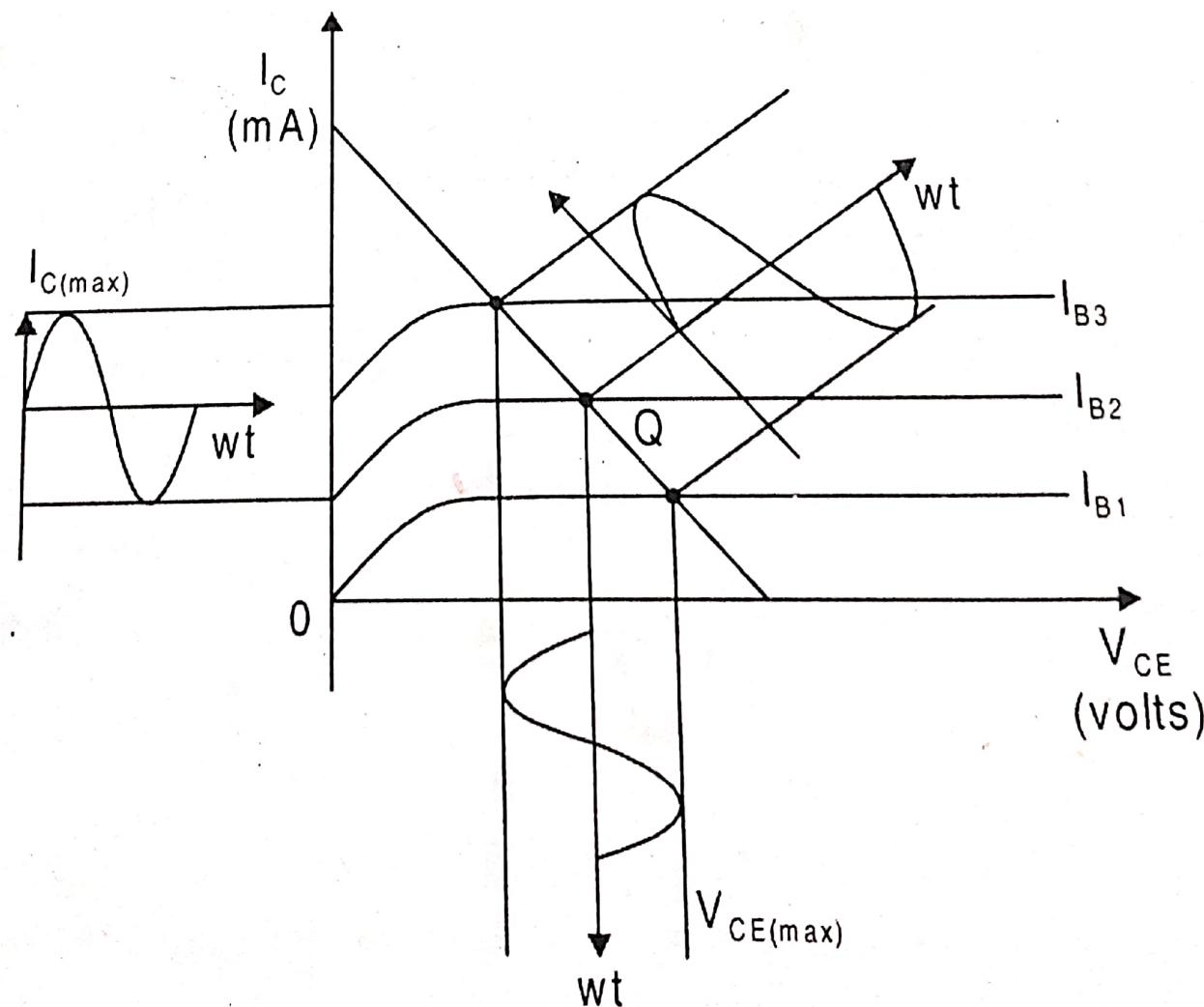


Fig. 7.36