


```

.org INT2addr ;
rjmp EX0_ISR

Main:
; Initialize the Stack Pointer
ldi r16, LOW(RAMEND)
out SPL, r16
ldi r16, HIGH(RAMEND)
out SPH, r16

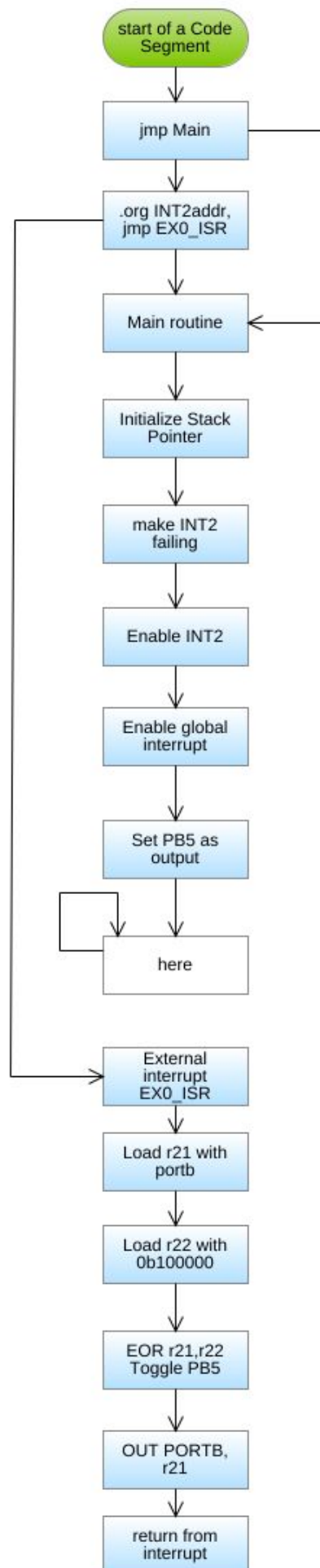
LDI R16, 0b100 ; make INT2 failing
STS EICRA, r16

SBI PORTD, 2 ; pull-up enabled, input pin PIND2
LDI R16, 1<<INT2 ; enable INT2
OUT EIMSK, R16

SEI ; enable interrupt
SBI DDRB, 5 ; PORTB5 as output
here:
inc r25
rjmp here

EX0_ISR:
IN R21, PORTB
LDI R22, (1<<5) ; for toggling PB5
EOR R21, R22
OUT PORTB, R21
reti

```



2 task2

[illegible]

```

ldi r19, 0xff

ldi r21, 0b1;
out DDRB, r19
ldi r25, 0b1; set this constant 0b1

ldi r24, 0b1; always be 1
ldi r23, 0b0; temp register
ldi r22, 0b0; always be 0

ldi r27, 0xff

sei

cpi r26, 0xff
breq jc
cpi r26, 0b0
breq rc

rjmp innit

rc:

ldi r26, 0xff
com r21 ; invert r21 to make
out PORTB, r21
com r21 ; revert r21 back

rcall Delay_1sec

lsl r21; left shift one bit

cpi r21, 0b0 ;compare with 0
breq reset ; if r21 is 0, then reset r21

rjmp rc

reset:
com r21 ; To set r21 to 1111 1111
out portB, r21 ; turn all LEDs off
rcall Delay_1sec; delay 0.5 sec
mov r21, r25; reset r21 to 0b1
;ret; make it stop permanently

rjmp rc

interrupt:

push r26

push r16
in r16, SREG
push r16

```

```

pop r16
out SREG, r16
pop r26
RETI

```

```

jc:
ldi r26, 0x0
or r23, r21
rol r21

```

```

com r23
out PORTB, r23; OUTPUT will be PORTB
com r23

```

```

rcall Delay_1sec

```

```

cpi r23, 0xff
breq decrease
rjmp jc

```

```

decrease:
lsr r23

```

```

com r23
out PORTB, r23; OUTPUT will be PORTD
com r23

```

```

rcall Delay_1sec

```

```

cpi r23, 0x0
breq reset1
rjmp decrease

```

```

reset1:
mov r23, r22 ; reset r23 to 0
mov r21, r24 ; reset r21 to 1

```

```

rjmp jc

```

```

Delay_1sec:                                ; For CLK(CPU) = 1 MHz
    LDI    r16,    4                        ; One clock cycle;
Delay1:
    LDI    r17,    125                      ; One clock cycle
Delay2:
    LDI    r18,    250                      ; One clock cycle

```

```

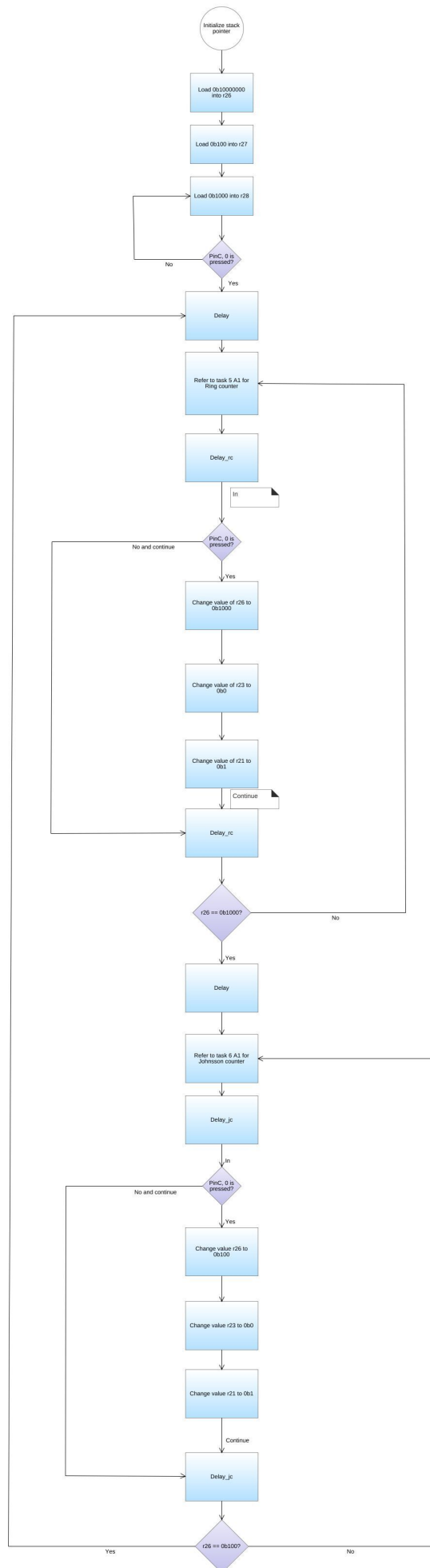
Delay3:
    DEC    r18            ; One clock cycle
    NOP                    ; One clock cycle
    BRNE   Delay3         ; Two clock cycles when jumping to Delay3, 1 clock when continuing
                                ;
    DEC    r17            ; One clock cycle
    BRNE   Delay2         ; Two clock cycles when jumping to Delay2, 1 clock when continuing
                                ;
    DEC    r16            ; One clock Cycle
    BRNE   Delay1         ; Two clock cycles when jumping to Delay1, 1 clock when continuing
RET

```

```

input_Delay:                ; For CLK(CPU) = 1 MHz
    LDI    r16, 1         ; One clock cycle;
Delay1c:
    LDI    r17, 125       ; One clock cycle
Delay2c:
    LDI    r18, 250       ; One clock cycle
Delay3c:
    DEC    r18            ; One clock cycle
    NOP                    ; One clock cycle
    BRNE   Delay3c        ; Two clock cycles when jumping to Delay3, 1 clock when continuing
                                ;
    DEC    r17            ; One clock cycle
    BRNE   Delay2c        ; Two clock cycles when jumping to Delay2, 1 clock when continuing
                                ;
    DEC    r16            ; One clock Cycle
    BRNE   Delay1c        ; Two clock cycles when jumping to Delay1, 1 clock when continuing
RET

```




```

;=====
; 1DT301, Computer Technology I
; Date: 2021-09-18
; Author:
; Student name Li Ang Hu
; Student name Fredric Eriksson Sep lveda
;
; Lab number: 3
; Title: task3 and task4
;
; Hardware: STK600, CPU ATmega2560
;
; Function: Add functions to the previous task for simulating stop lights when braking. Us
the braking.
Functions
1. Brake and no turning
Turn ON all LEDs (0-7).
2. Brake and turn right
LED 4      7 is ON, LED 0      3 is blinking as a Ring counter to the right..
3. Brake and turn left
LED 0      3 is ON, LED 4      7 is blinking as a Ring counter to the left..

; Input ports: PORTD
;
; Output ports: PORTB
;
; Subroutines: If applicable.
; Included files: m2560def.inc
;
; Other information:
;
; Changes in program: (Description and date)
;
;=====
.org 0x00
rjmp innit

.org 0x02
rjmp int_right

.org 0x04
rjmp int_left

.org 0x06
rjmp int_brake

activate_seiC:
ldi r28, 0x1
rjmp int_right

int_right:
cpi r28, 0x0
breq activate_seiC
cpi r26, 0xff
breq brake_turn_right
ldi r27, 0b11000000
out portb, r27

```

```

mov r2, r27;
or r2, r31;
com r2
out portb, r2
rcall Delay_1sec

lsr r31
cpi r31, 0b0
breq resetL

sbis PIND, 0
rjmp int_right
reti

resetL:

mov r31, r23
rjmp int_right

brake_turn_left:
cli
ldi r28, 0xff
ldi r26, 0b0
ldi r27, 0b00001111
out portb, r27

mov r2, r27;
or r2, r30;
com r2
out portb, r2
rcall Delay_1sec

lsl r30
cpi r30, 0b0
breq resetL2

sbic PIND, 2
rjmp int_left

sbic PIND, 1
rjmp int_brake

rjmp brake_turn_left

resetL2:
mov r30, r24
rjmp brake_turn_left

brake_turn_right:
cli
ldi r26, 0b0
ldi r27, 0b11110000
out portb, r27

mov r2, r27;
or r2, r31;
com r2

```

```

out portb, r2
rcall Delay_1sec

lsr r31
cpi r31, 0b0
breq resetR2

sbic PIND, 2
rjmp int_right

sbic PIND, 0
rjmp int_brake

rjmp brake_turn_right

int_brake:
cpi r28, 0x0
breq activate_seiB
ldi r26, 0xff
com r26
out PORTB, r26
com r26

cpi r27, 0b11000000
breq brake_turn_right

cpi r27, 0b00000011
breq brake_turn_left

sbic PIND, 2
reti
rjmp int_brake

activate_seiB:
sei
ldi r28, 0x1
rjmp int_brake

resetR2:
mov r31, r23
rjmp brake_turn_right

int_left:
cpi r28, 0x0
breq activate_sei
cpi r26, 0xff
breq brake_turn_left
ldi r27, 0b00000011
out portb, r27

mov r2, r27;
or r2, r30;
com r2
out portb, r2
//rcall Delay_1sec

lsl r30
cpi r30, 0b0
breq resetR

```

```

sbis PIND, 1
rjmp int_left
reti
activate_sei:
ldi r28, 0x1
sei
rjmp int_left

```

```

resetR:
mov r30, r24
rjmp int_left

```

```

innit:
ldi r31, LOW(RAMEND)
out spl, r31
ldi r31, HIGH(RAMEND)
out sph, r31

```

```

LDI R16, 0b00101010 ; make INT0
STS EICRA, r16

```

```

ldi r19, 0xff

```

```

out DDRB, r19

```

```

SBI PORTD, 2 ; pull-up enabled, input pin PIND2
LDI R16, 1<<INT0 | 1<<INT1 | 1<<INT2
OUT EIMSK, R16

```

```

ldi r23, 0b00001000
ldi r24, 0b0010000
mov r31, r23
mov r30, r24
sei

```

```

test:
ldi r28, 0x0
ldi r27, 0b0
ldi r26, 0b1
ldi r22, 0b00111100
out PortB, r22

```

```

rjmp test

```

```

input_Delay:                                ; For CLK(CPU) = 1 MHz
    LDI    r16,    1                        ; One clock cycle;
Delay1c:
    LDI    r17,    125                      ; One clock cycle
Delay2c:
    LDI    r18,    250                      ; One clock cycle
Delay3c:
    DEC    r18                              ; One clock cycle
    NOP                                     ; One clock cycle

```

```

    BRNE    Delay3c        ; Two clock cycles when jumping to Delay3, 1 clock when continu

    DEC     r17             ; One clock cycle
    BRNE    Delay2c        ; Two clock cycles when jumping to Delay2, 1 clock when contin

    DEC     r16             ; One clock Cycle
    BRNE    Delay1c        ; Two clock cycles when jumping to Delay1, 1 clock when contin
RET

Delay_1sec:                ; For CLK(CPU) = 1 MHz
    LDI     r16,    4      ; One clock cycle;
Delay1:
    LDI     r17,    125    ; One clock cycle
Delay2:
    LDI     r18,    250    ; One clock cycle
Delay3:
    DEC     r18            ; One clock cycle
    NOP                    ; One clock cycle
    BRNE    Delay3        ; Two clock cycles when jumping to Delay3, 1 clock when continu

    DEC     r17            ; One clock cycle
    BRNE    Delay2        ; Two clock cycles when jumping to Delay2, 1 clock when contin

    DEC     r16            ; One clock Cycle
    BRNE    Delay1        ; Two clock cycles when jumping to Delay1, 1 clock when contin
RET

```

