

JURNAL PRAKTIKUM

OARKOM II

MODUL IV

IMPLEMENTASI FPGA



Nama : Fresinendi

No. BP : 2211512019

Hari/Tanggal : Jumat/ 25 November 2024

Shift : III

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FAKULTAS TEKNOLOGI INFORMASI

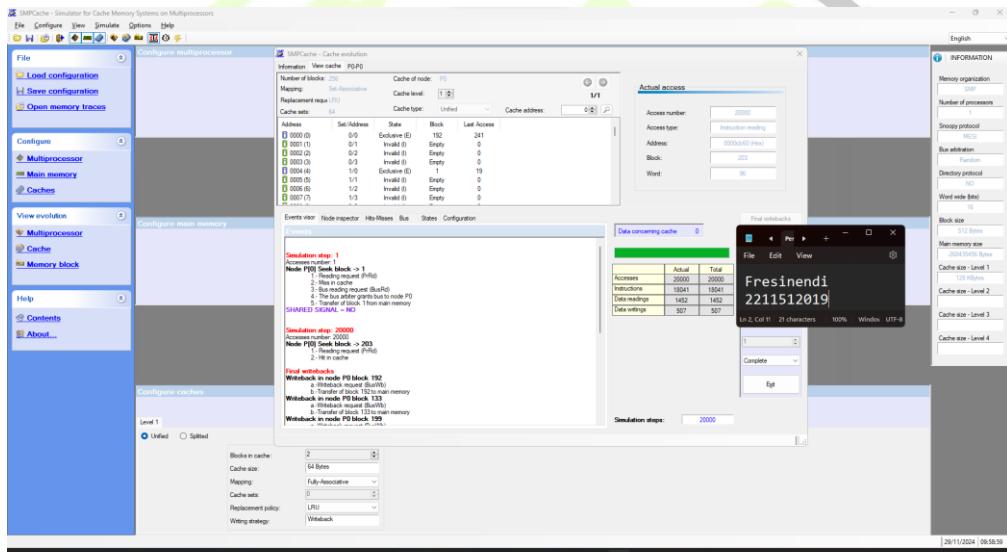
UNIVERSITAS ANDALAS

2024

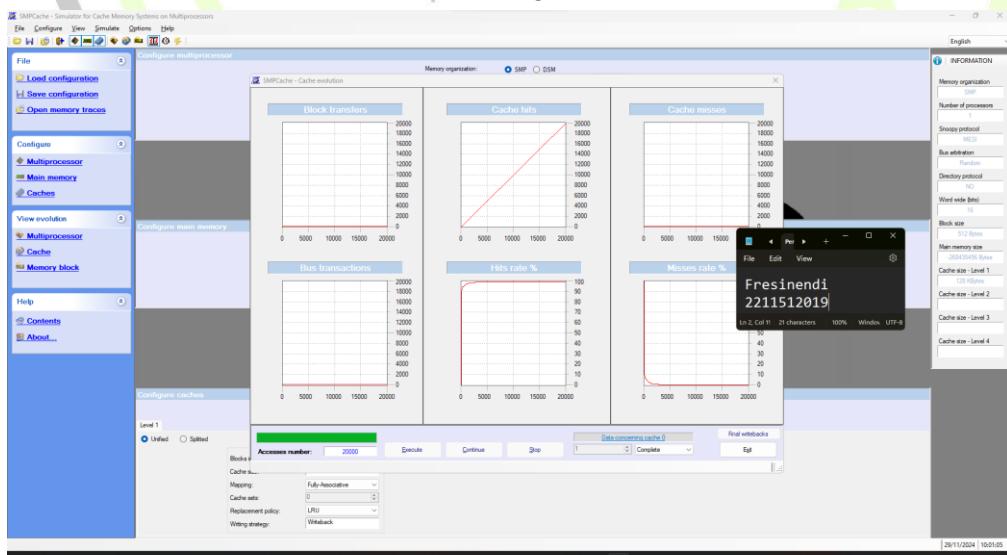
1.JURNAL PRAKTIKUM

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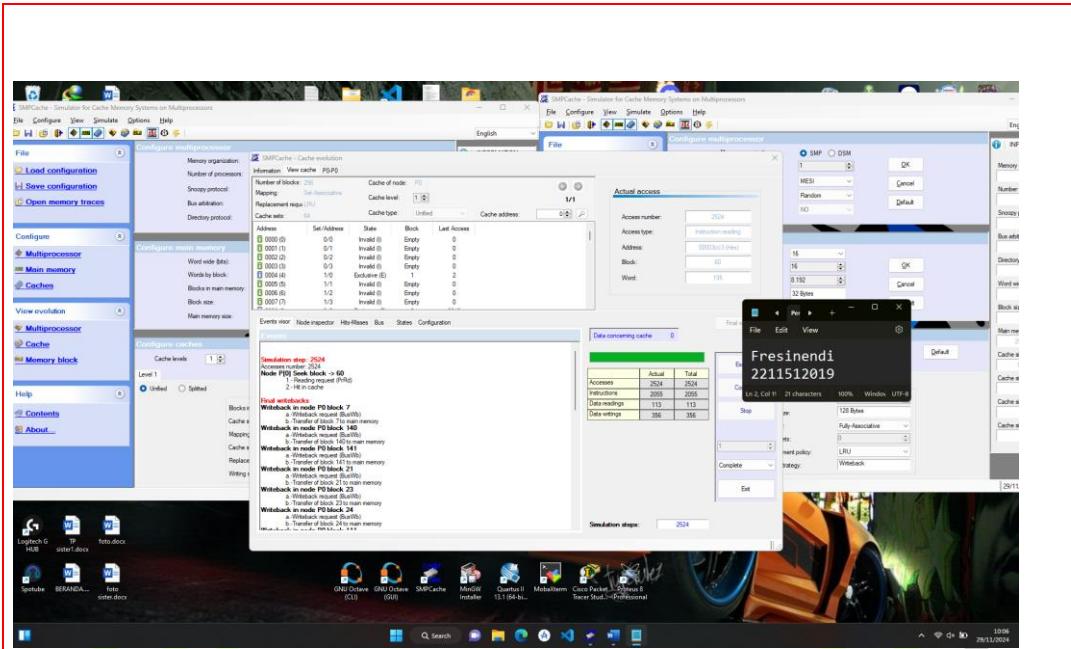
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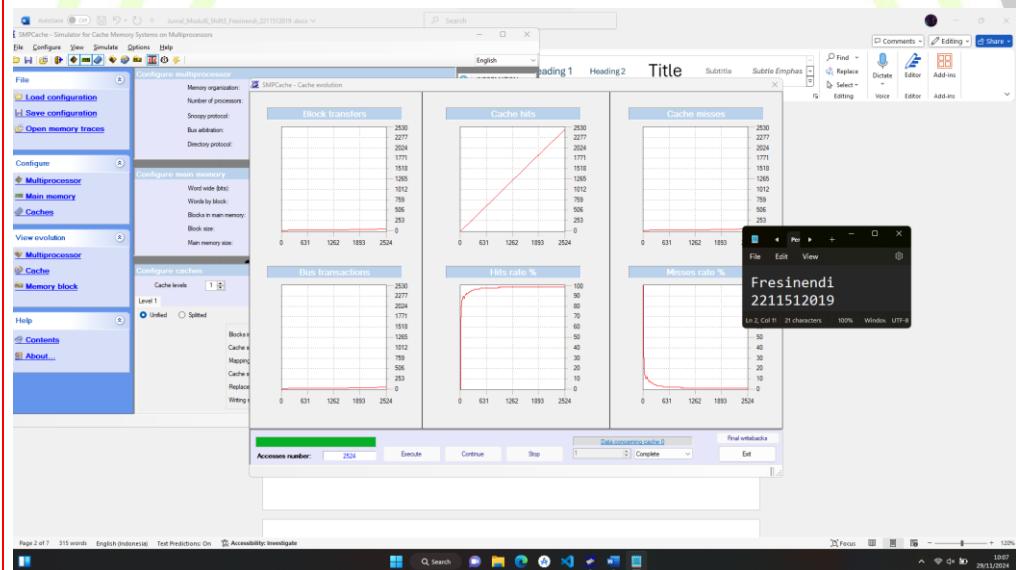
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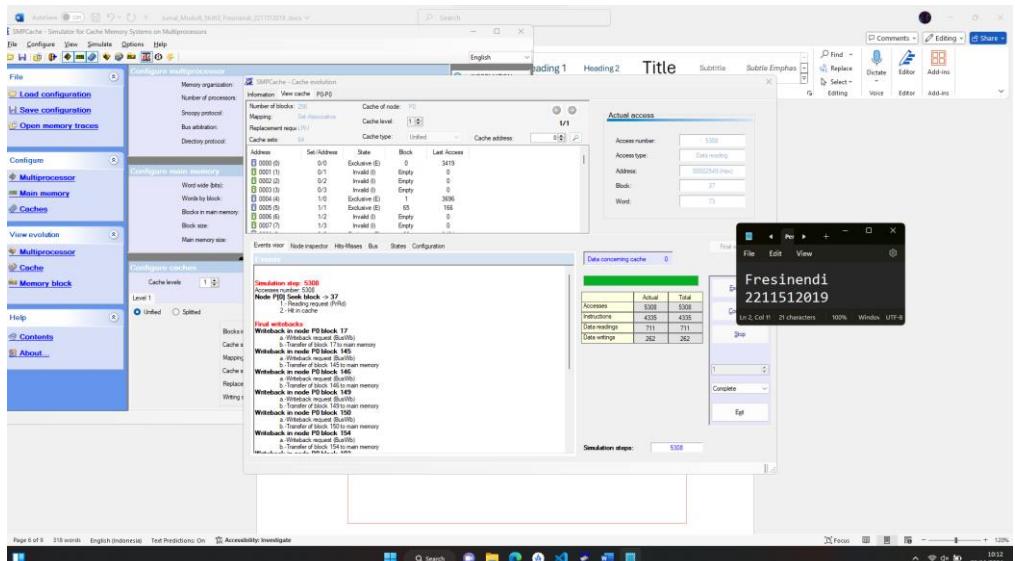


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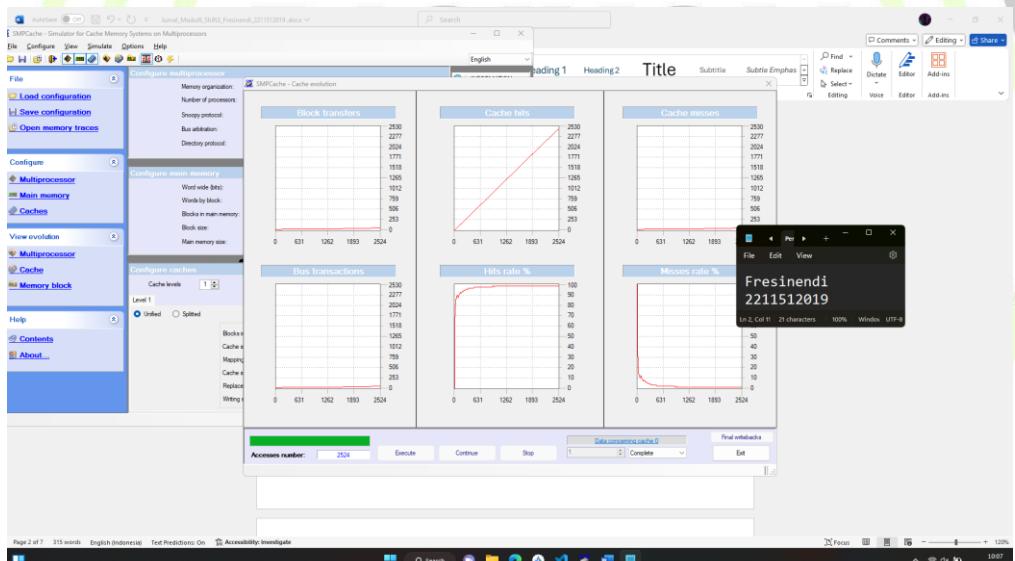


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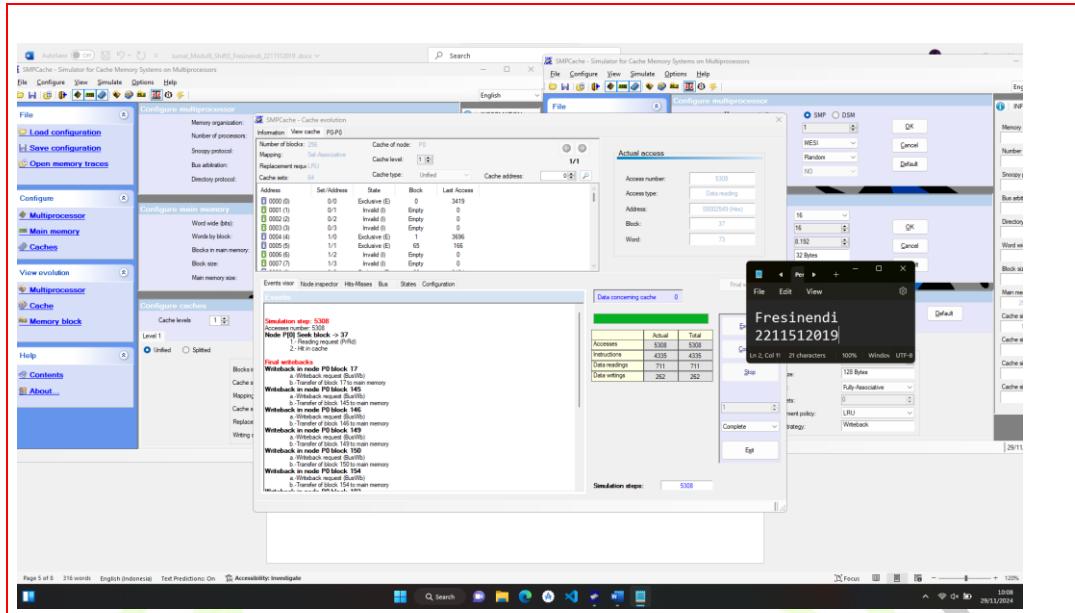
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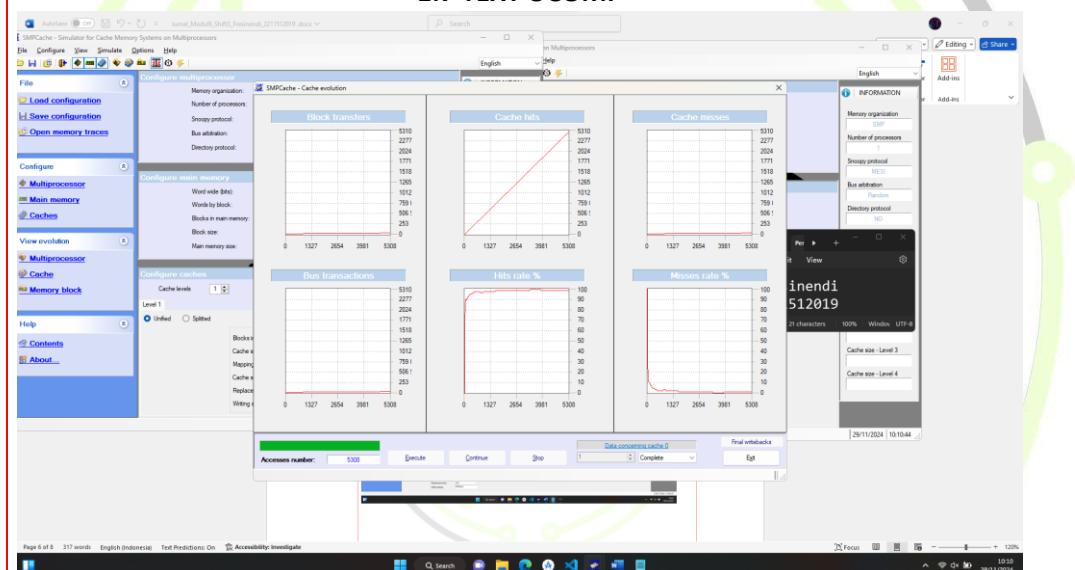
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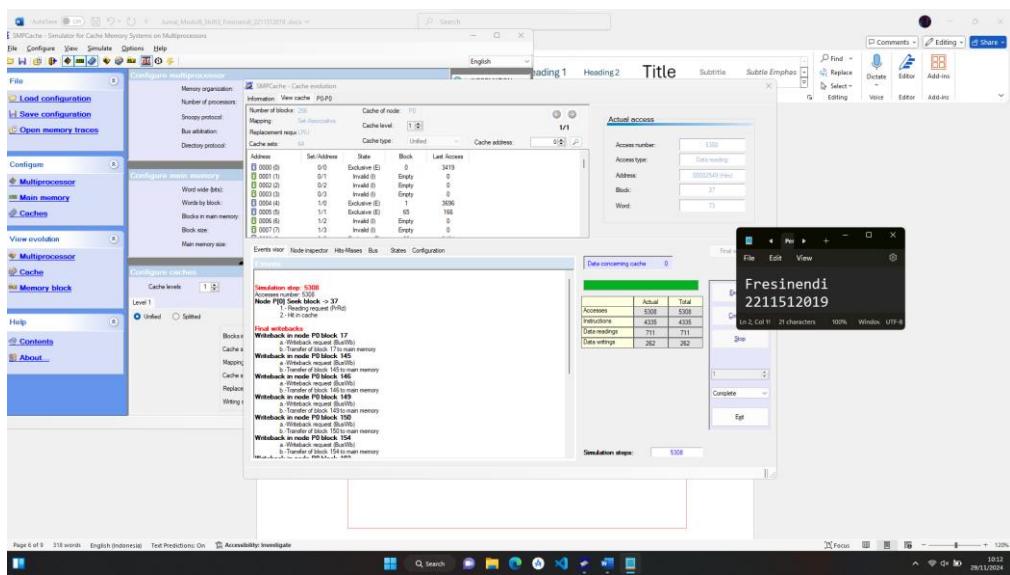


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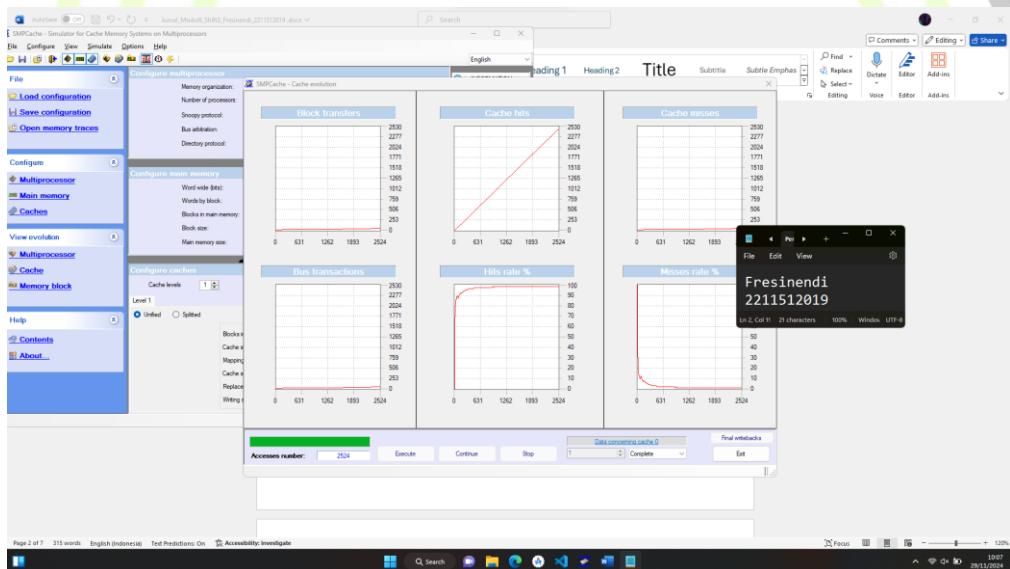


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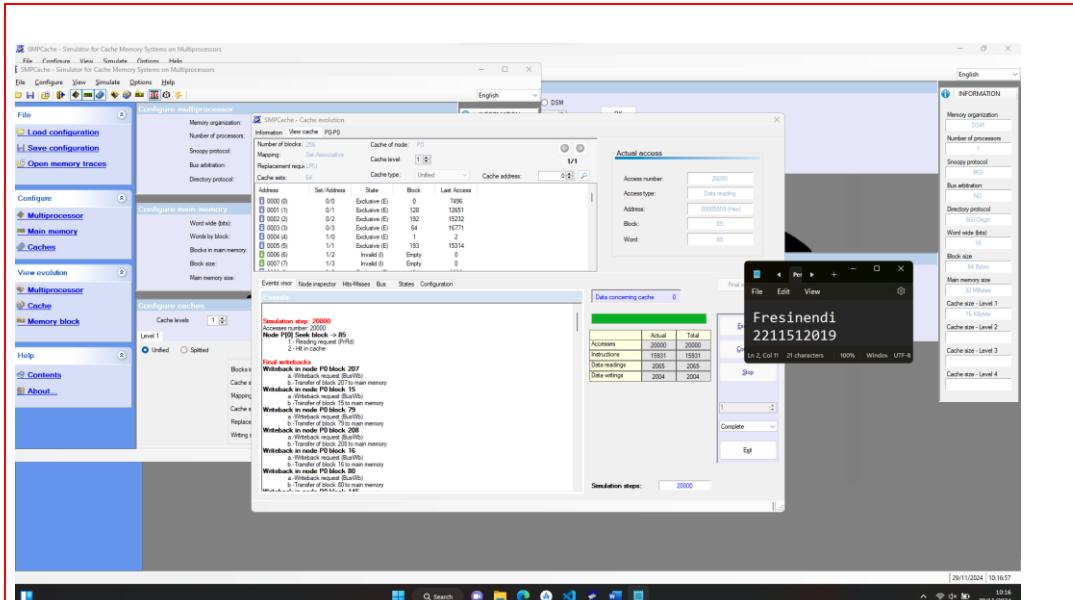
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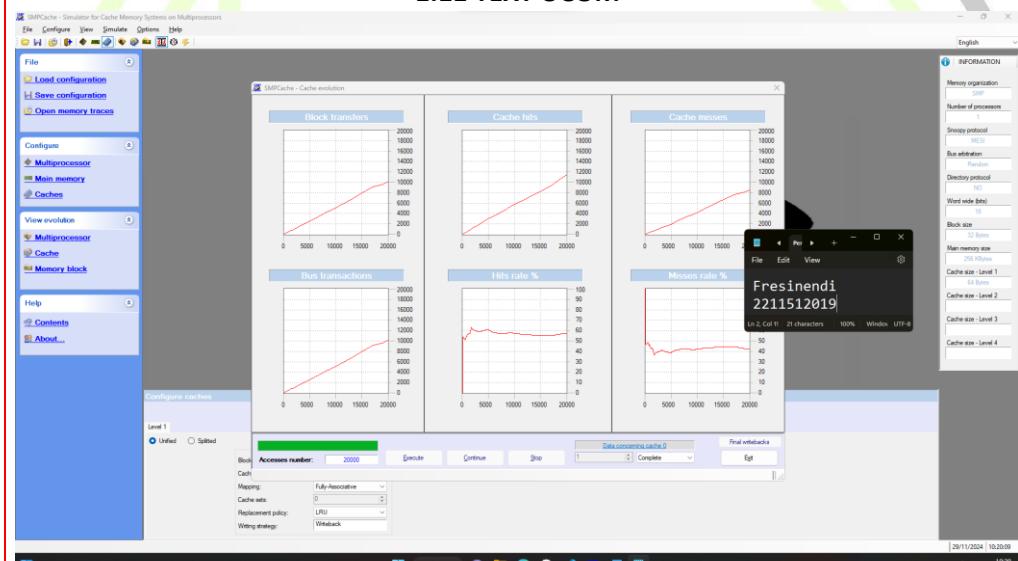
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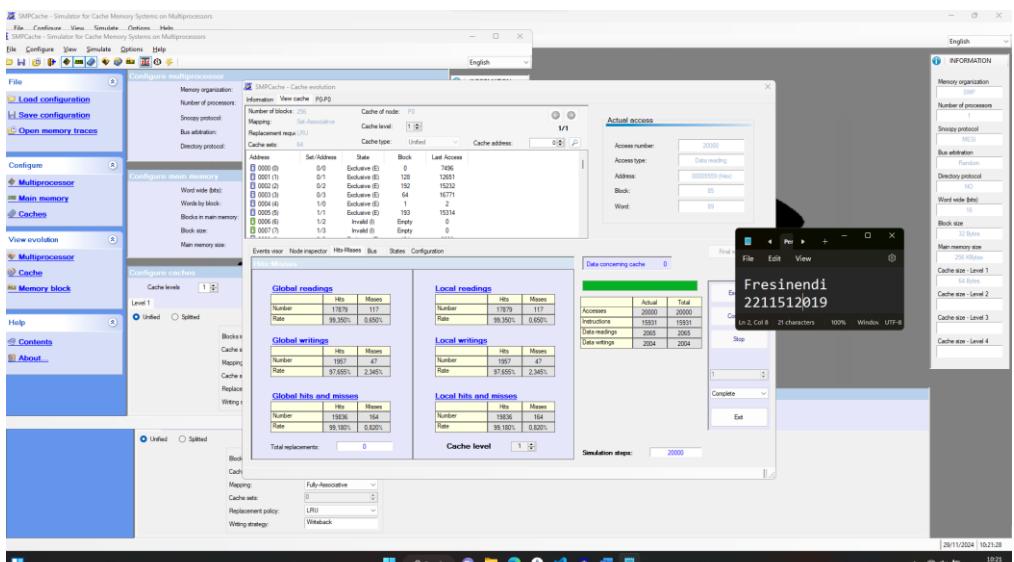


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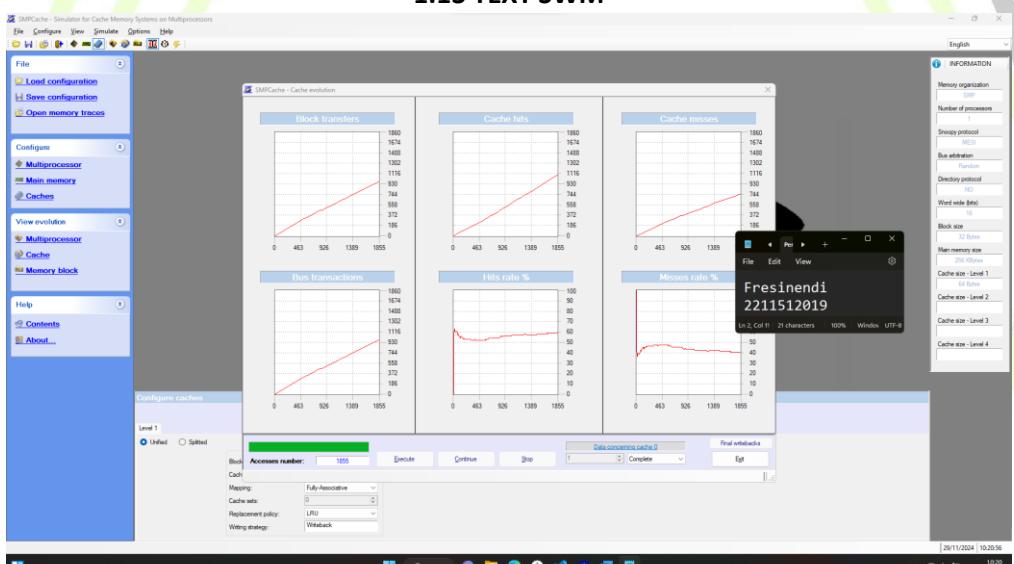


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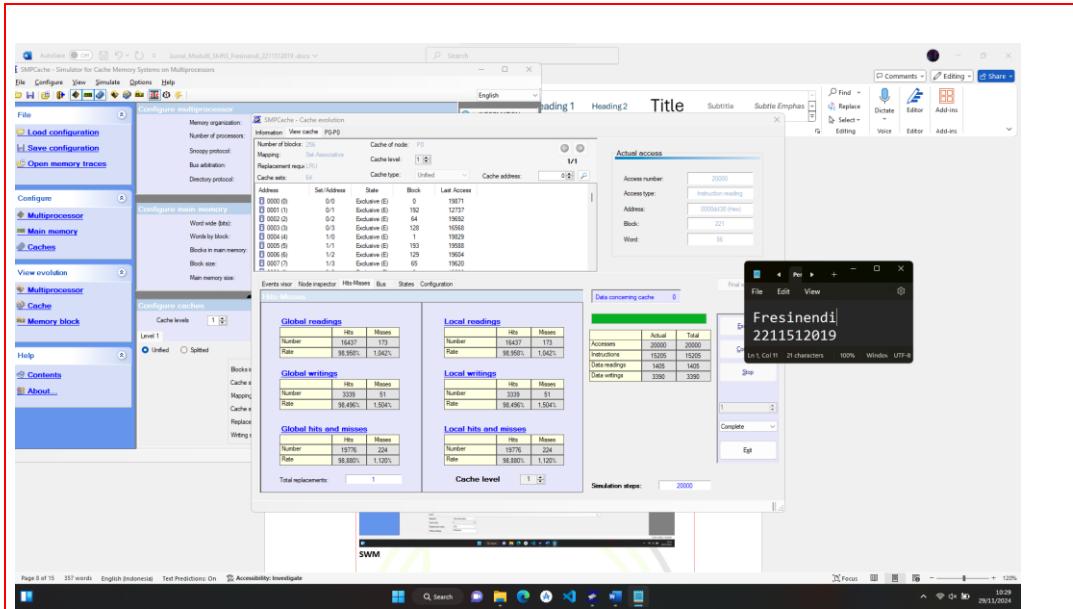
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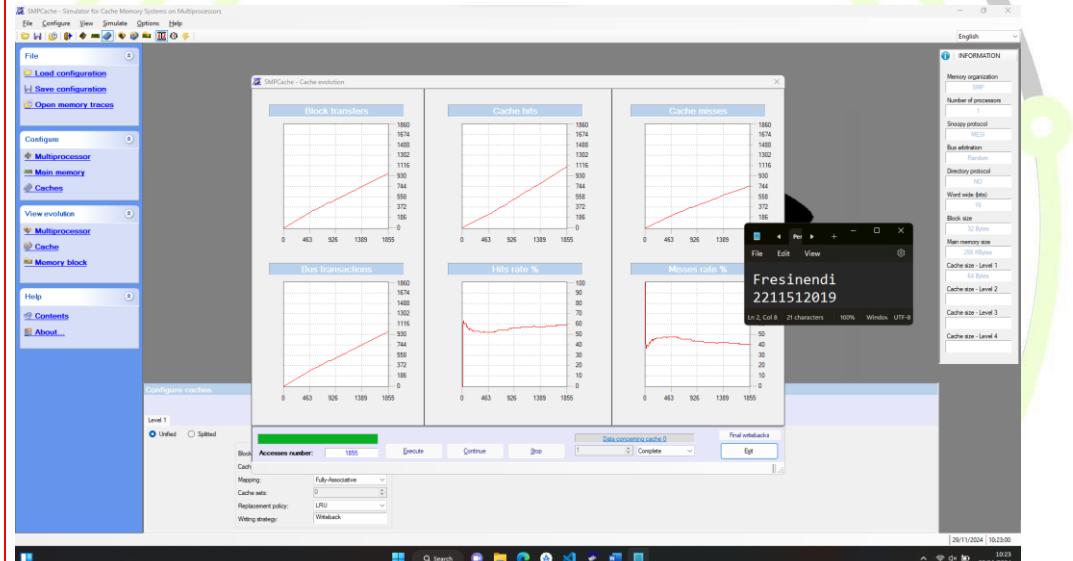
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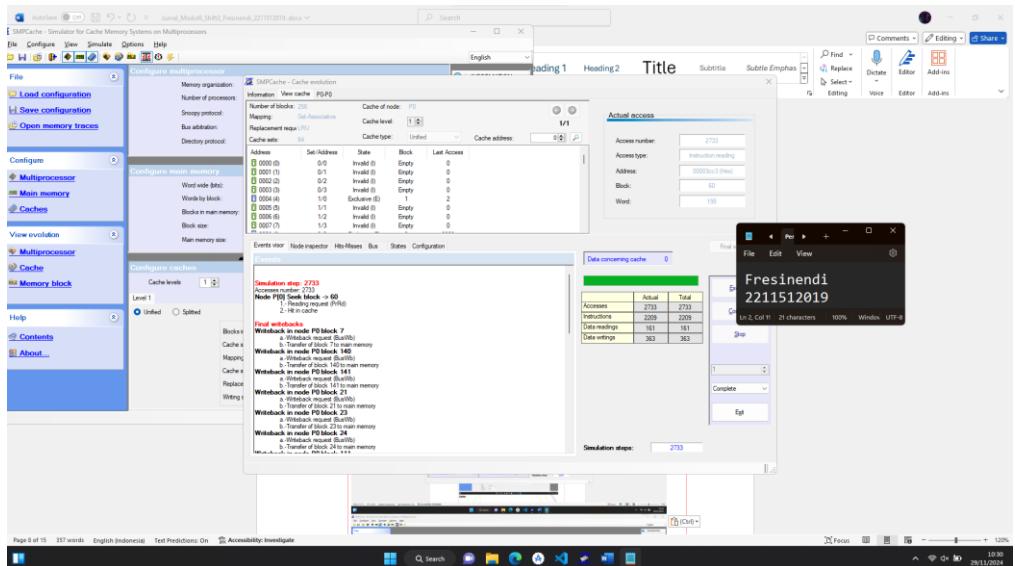


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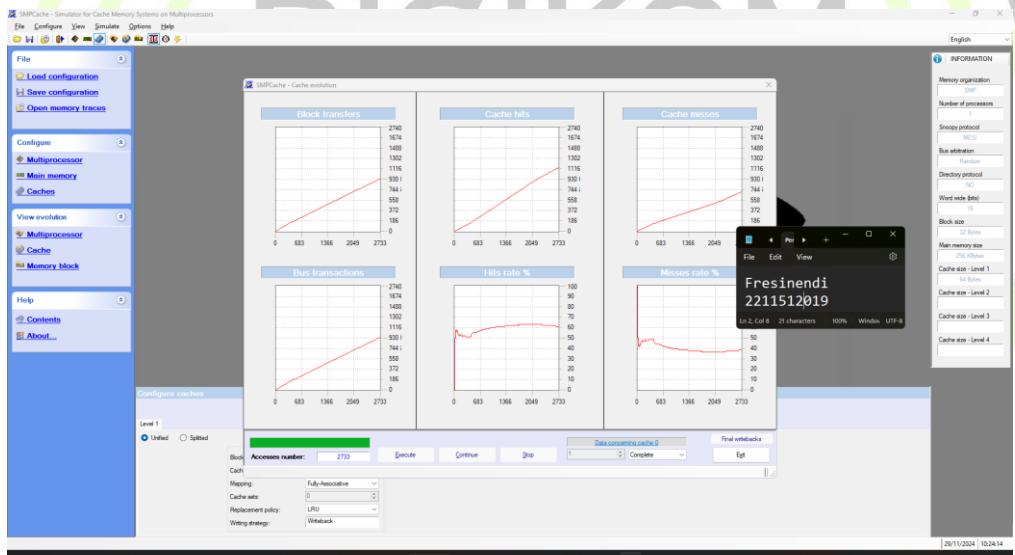


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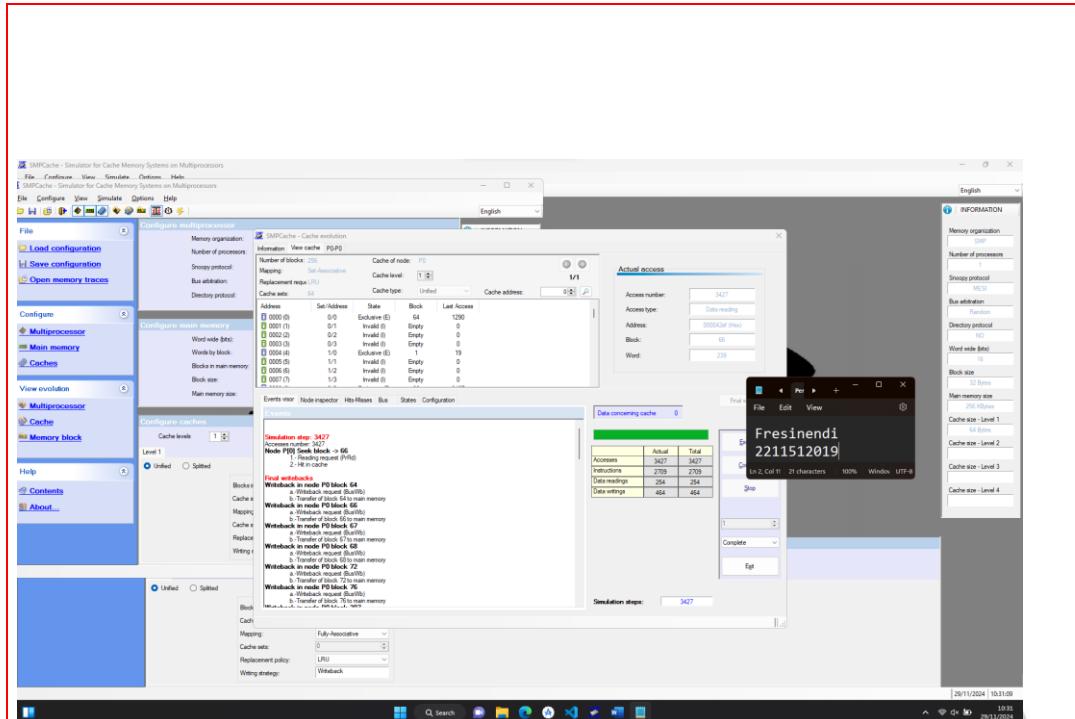
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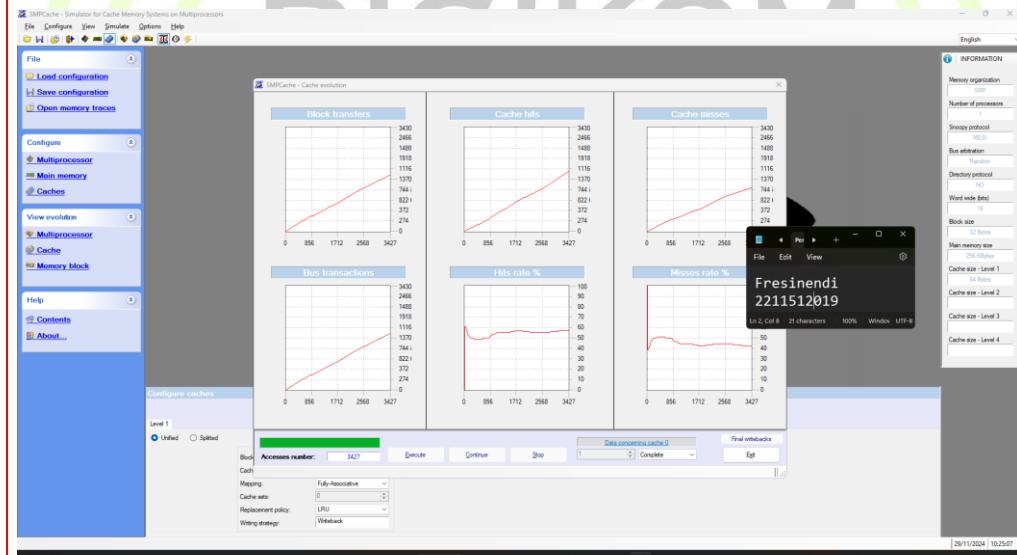
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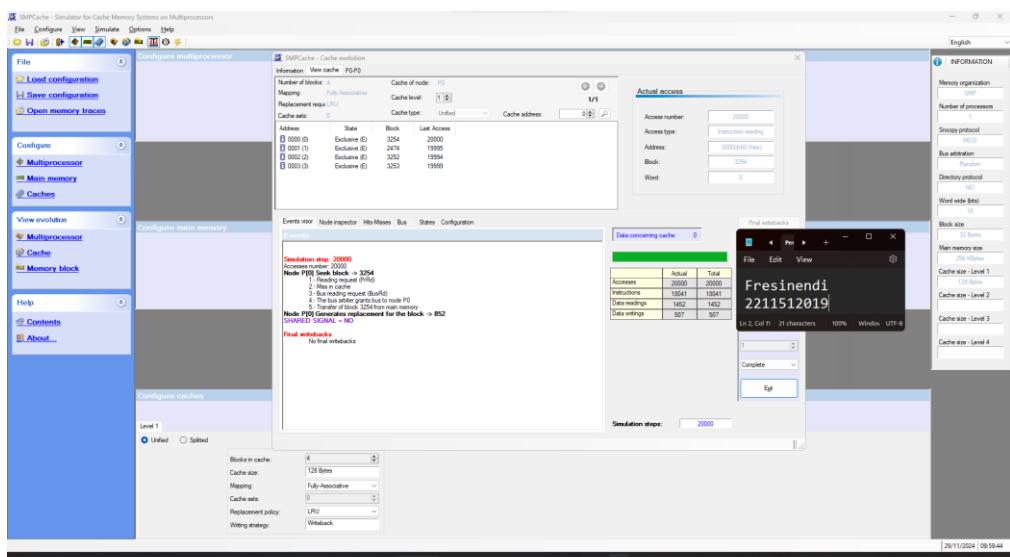


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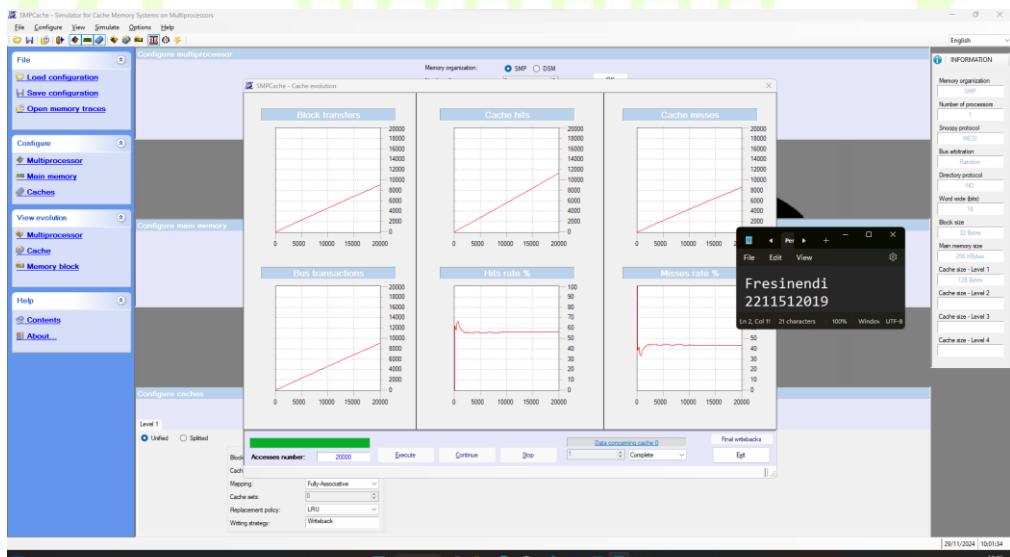


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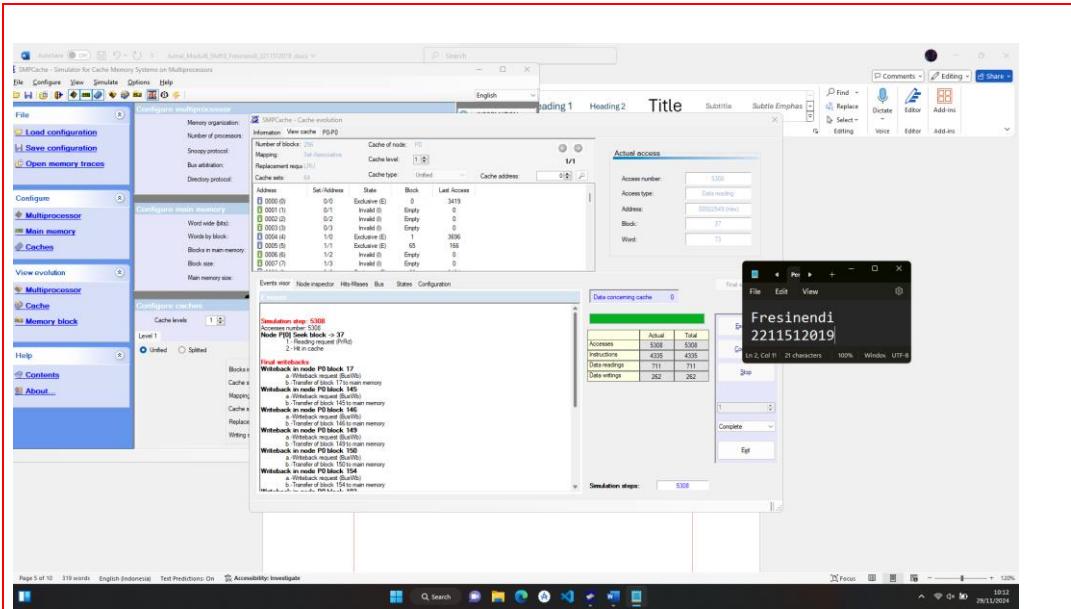
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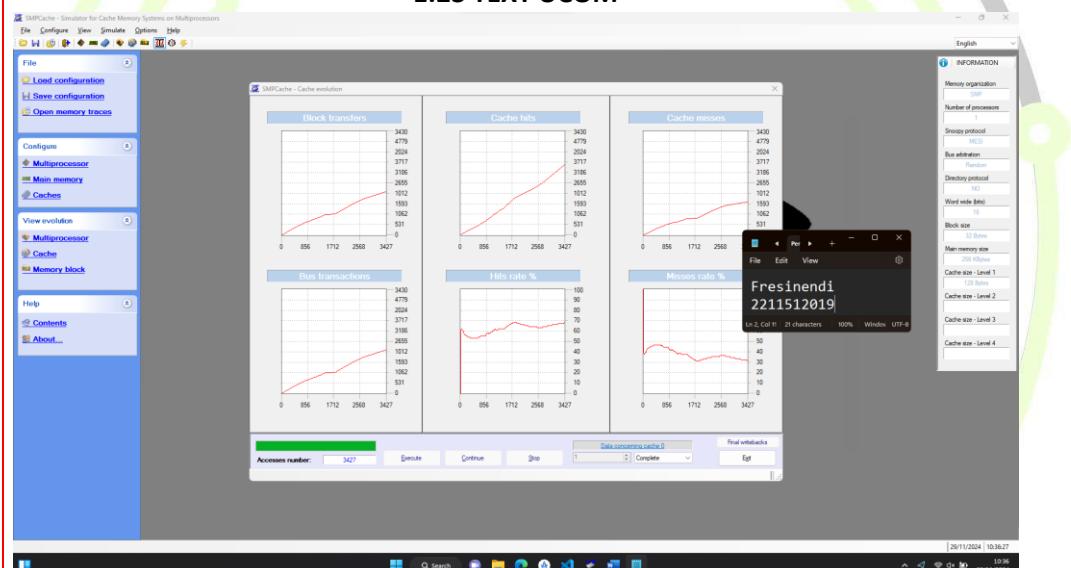
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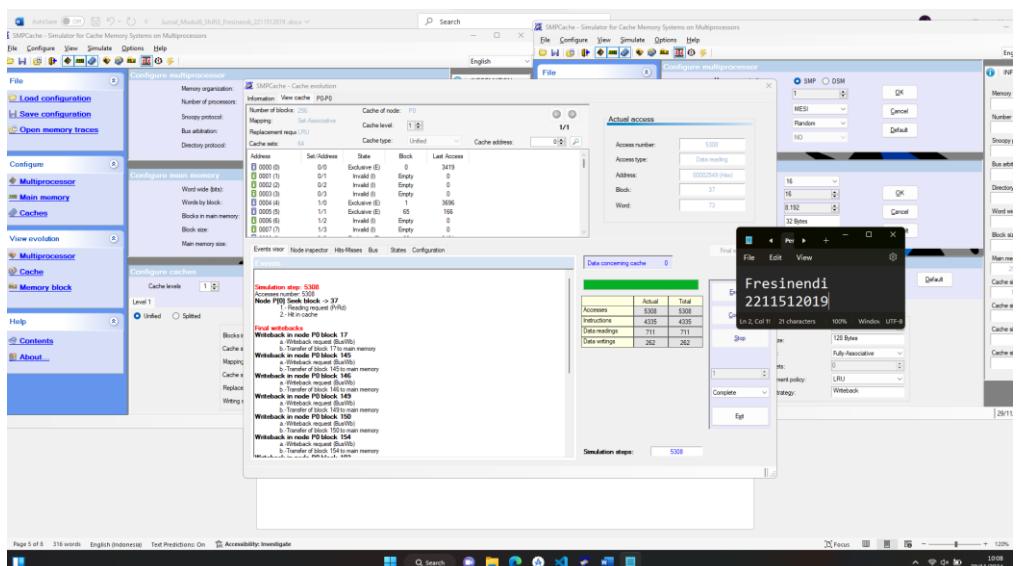


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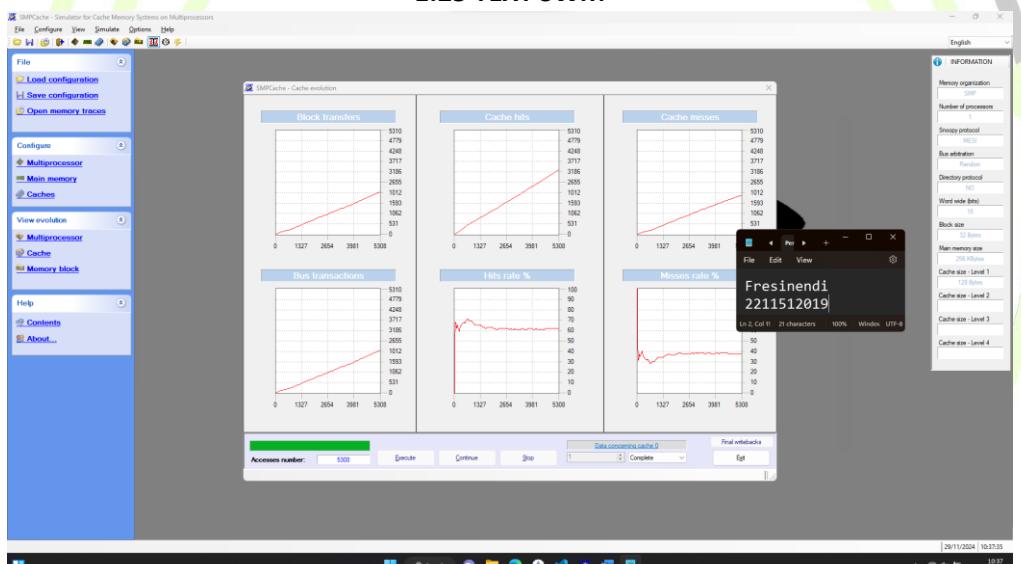


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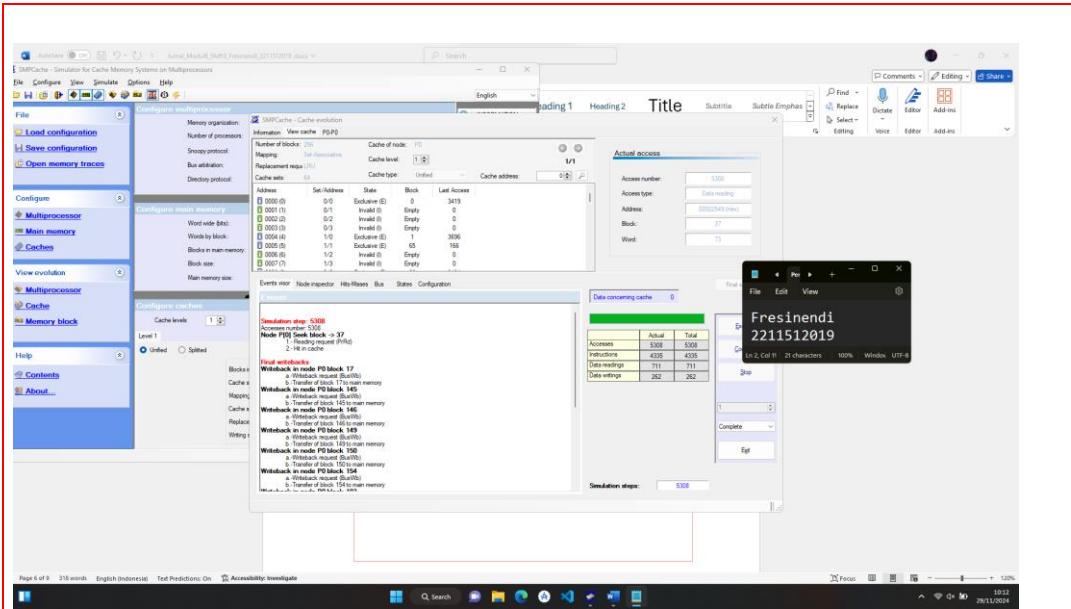
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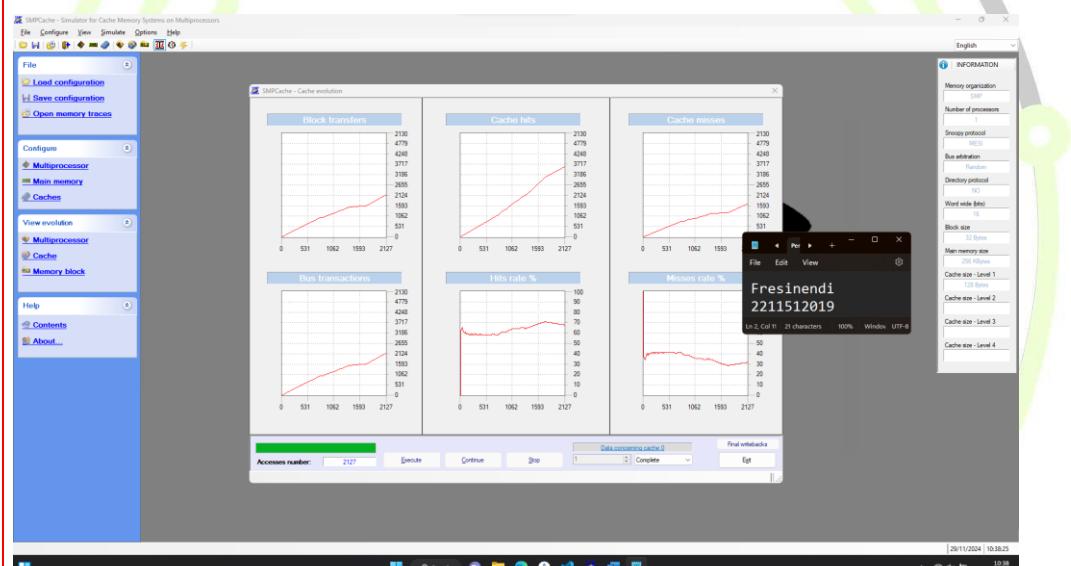
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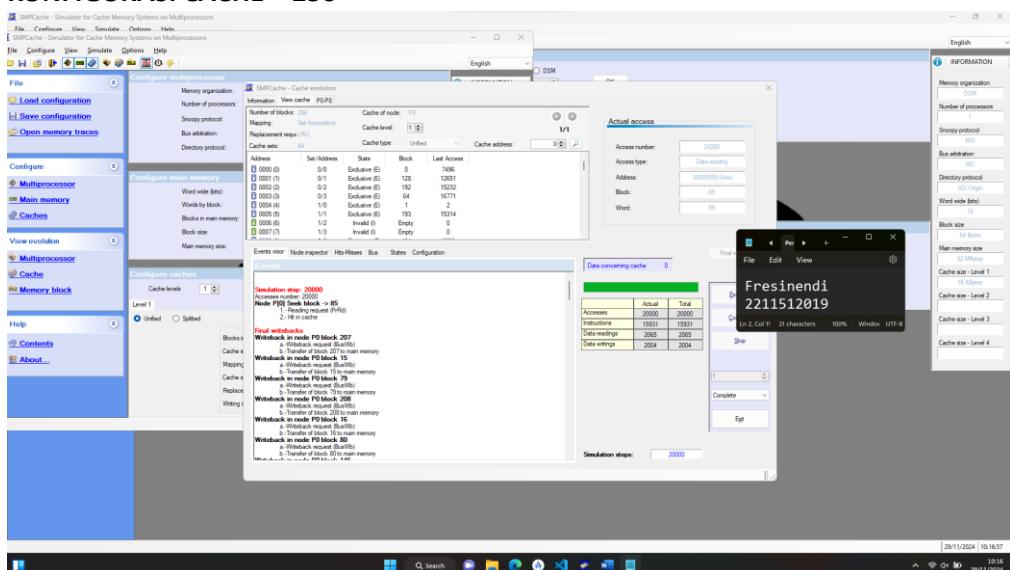


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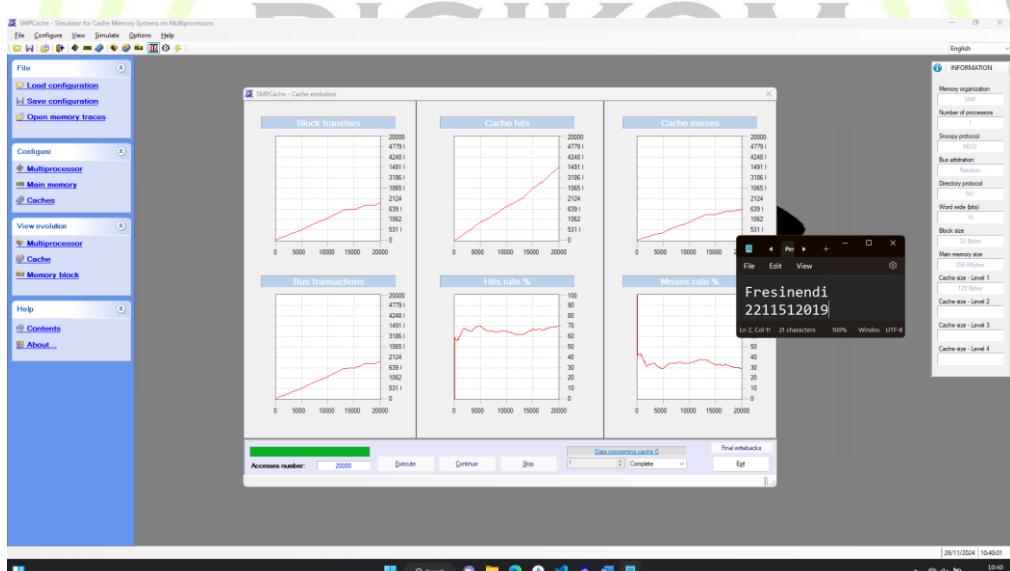


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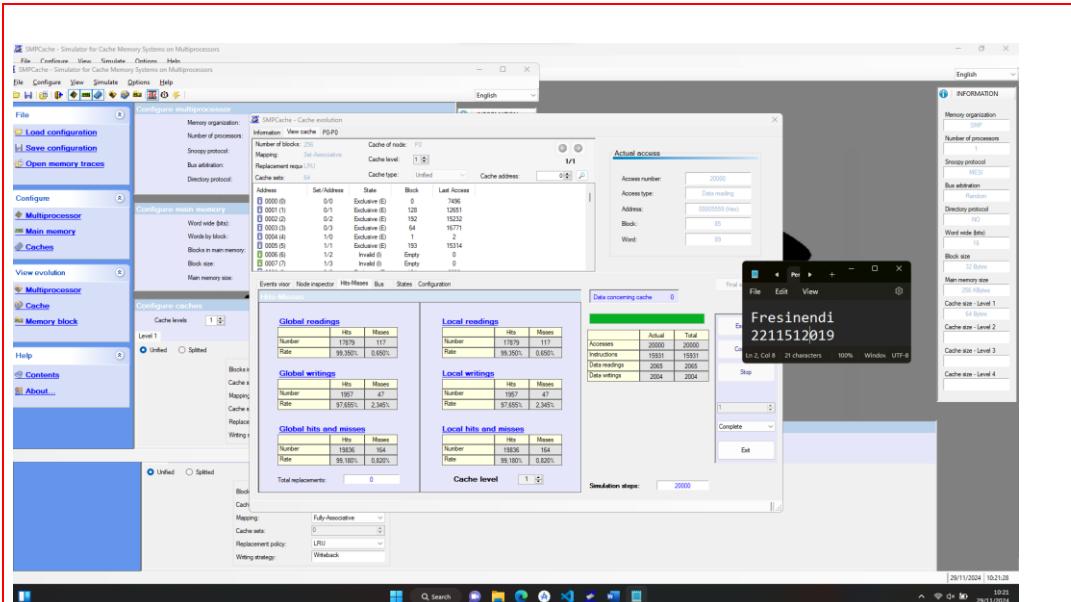
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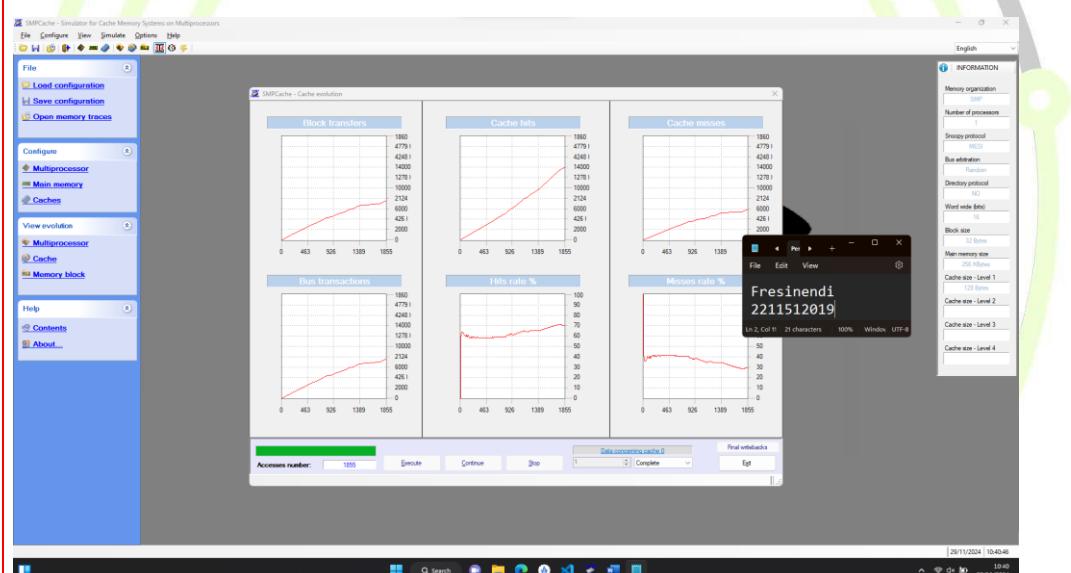
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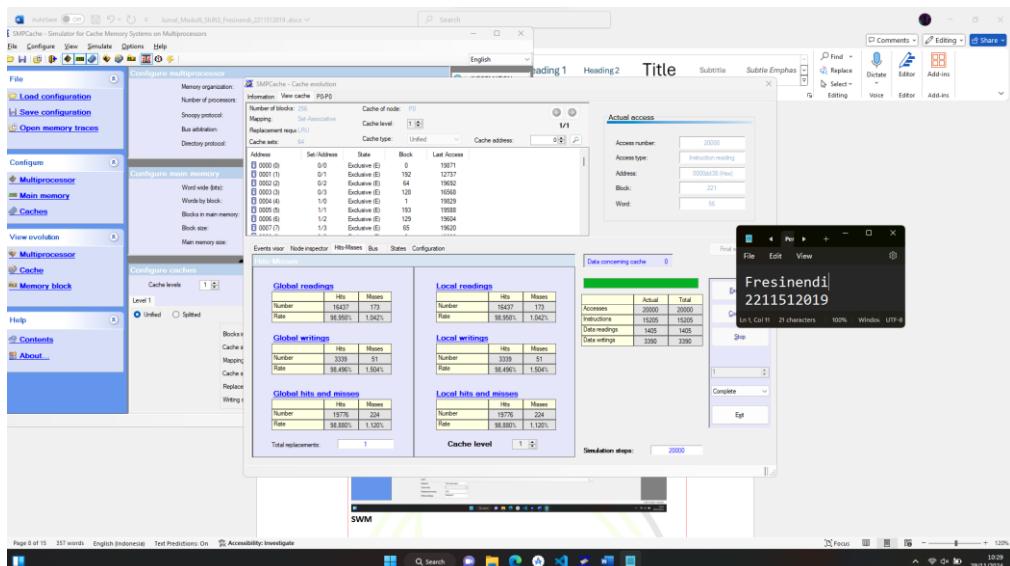


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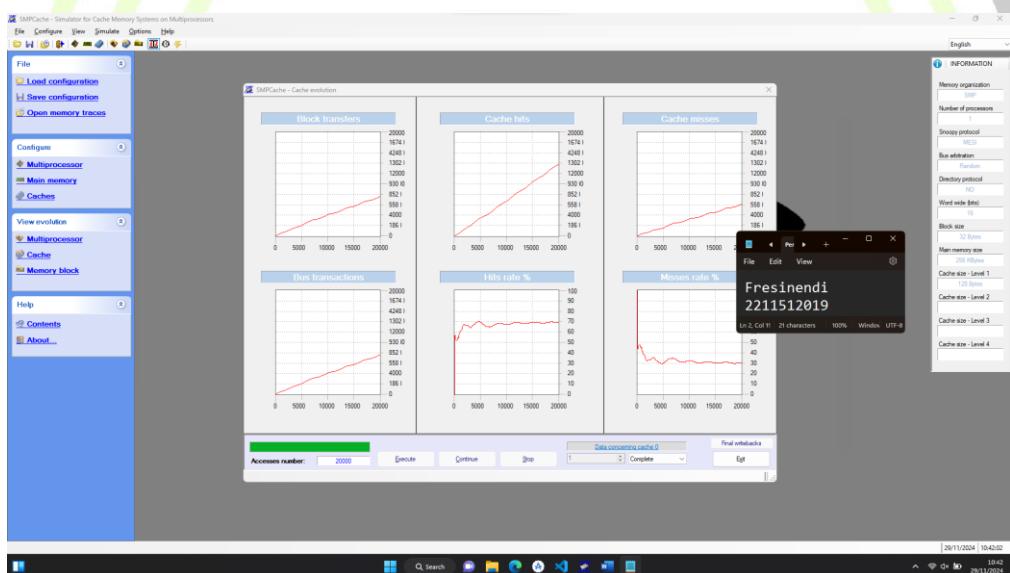


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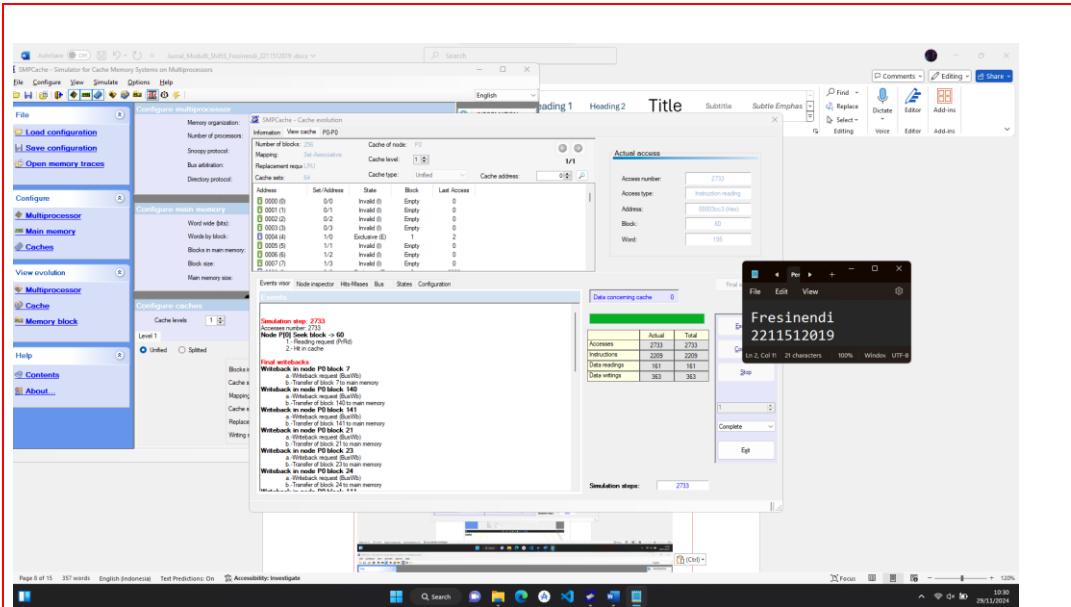
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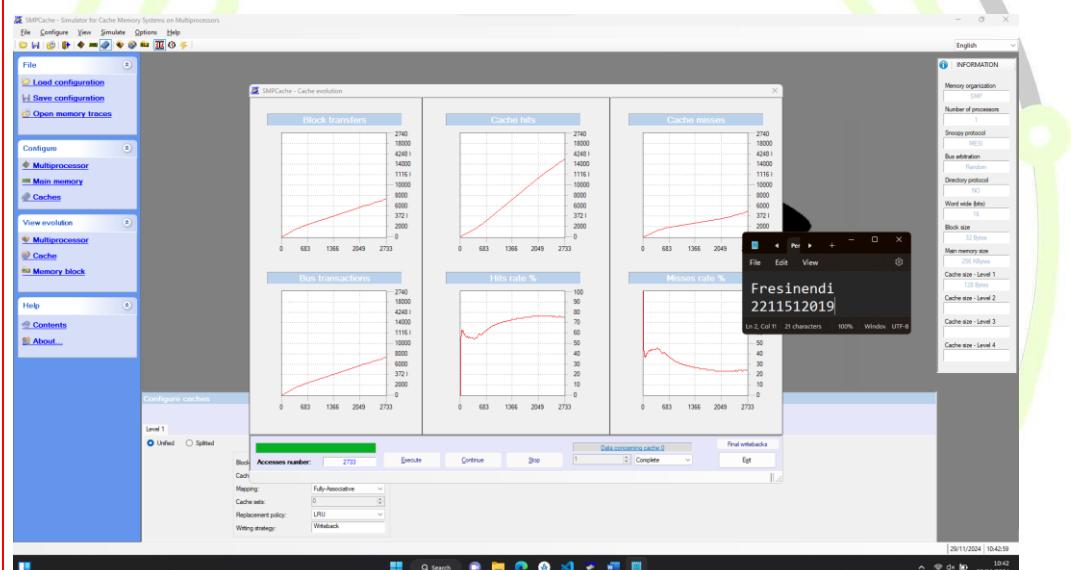
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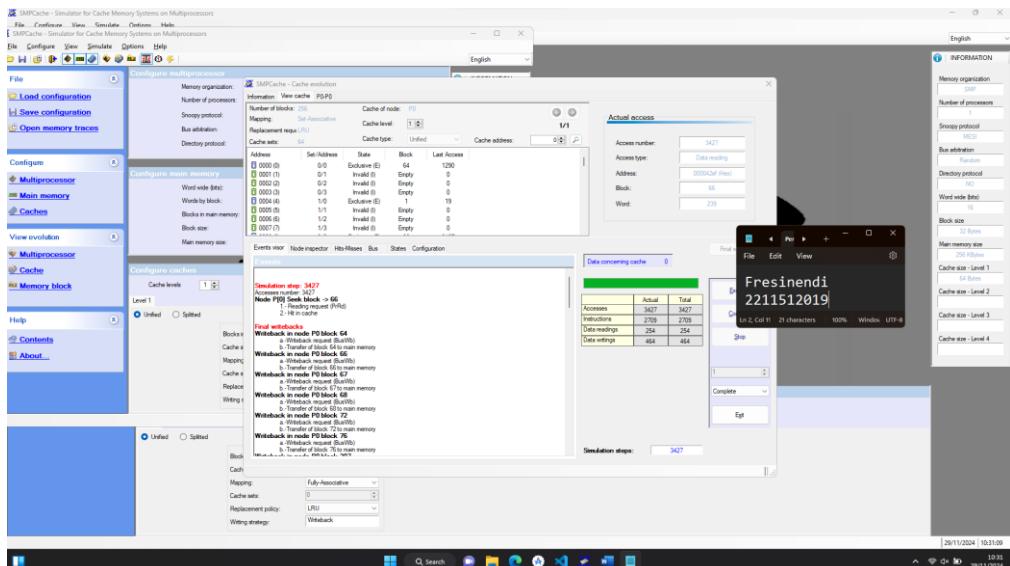


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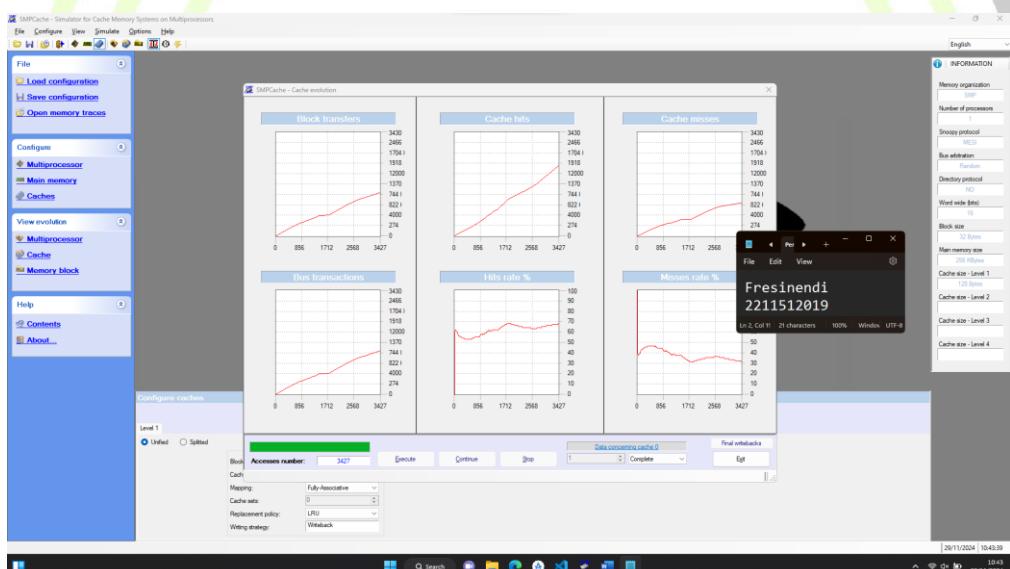


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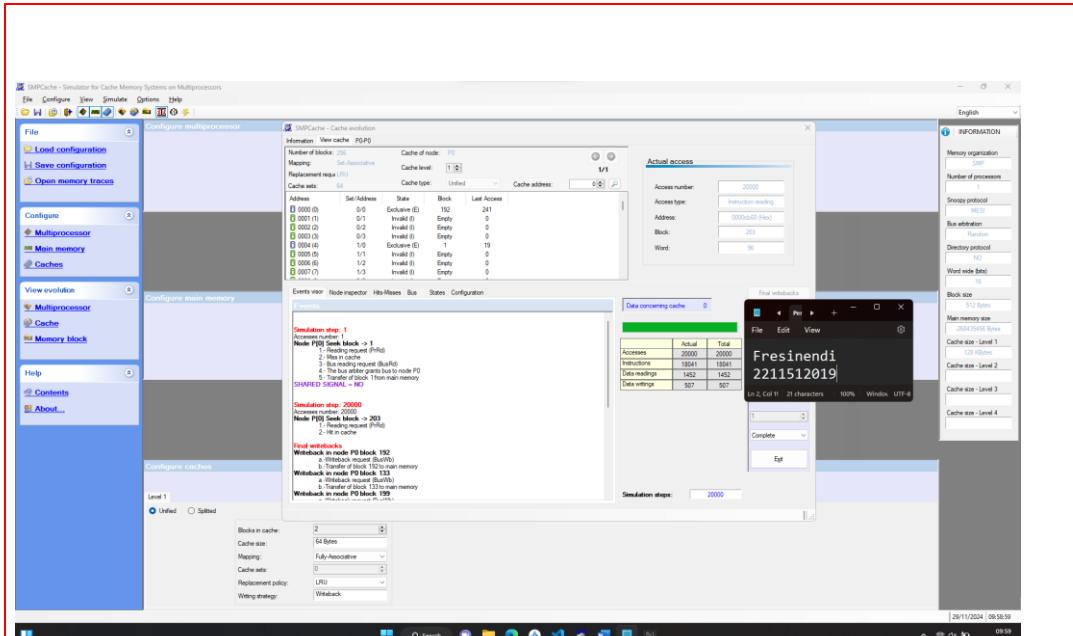
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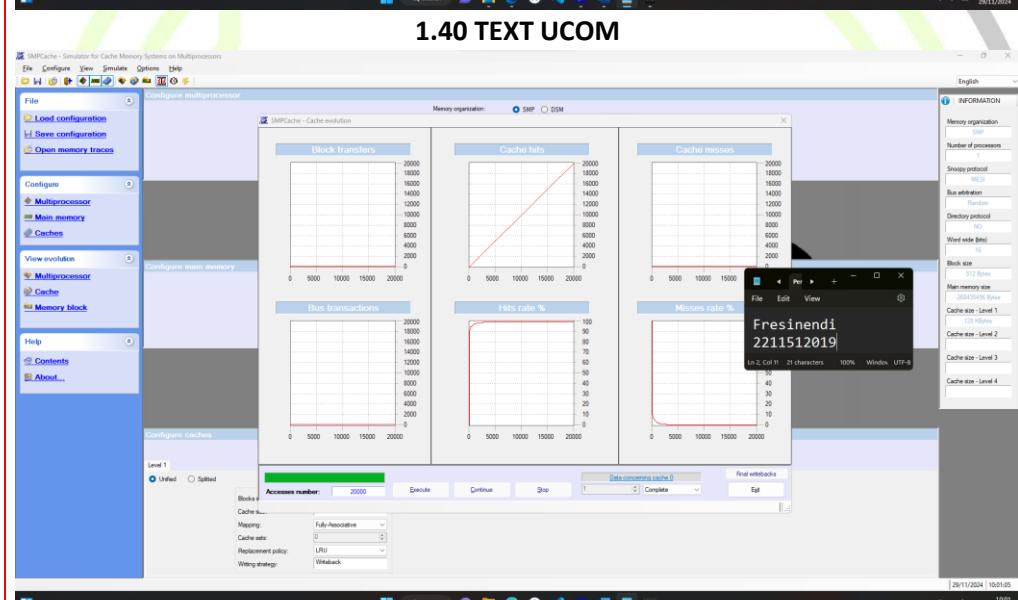
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1.38 GRAPHIC SWM



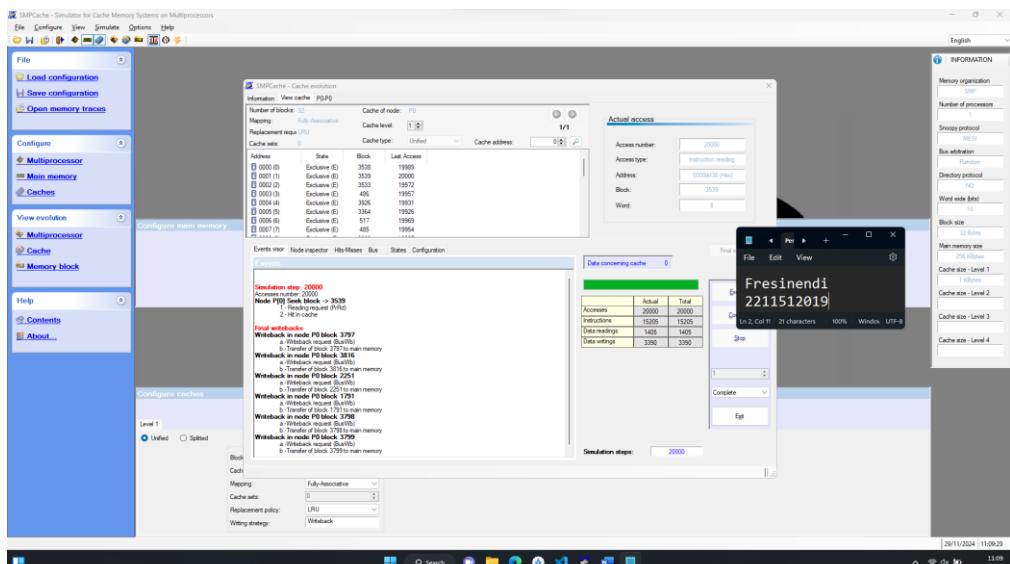
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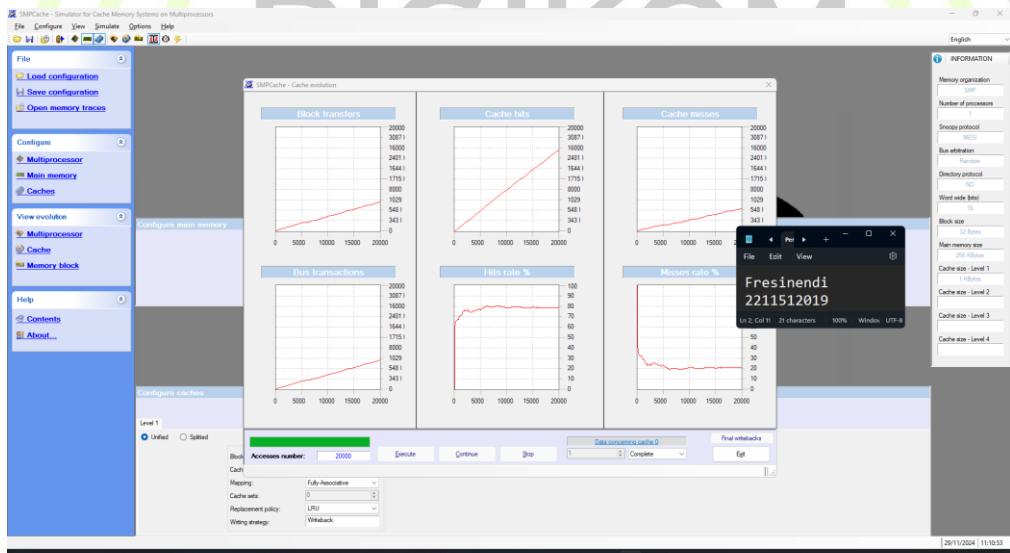
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PERCOBAAN 2

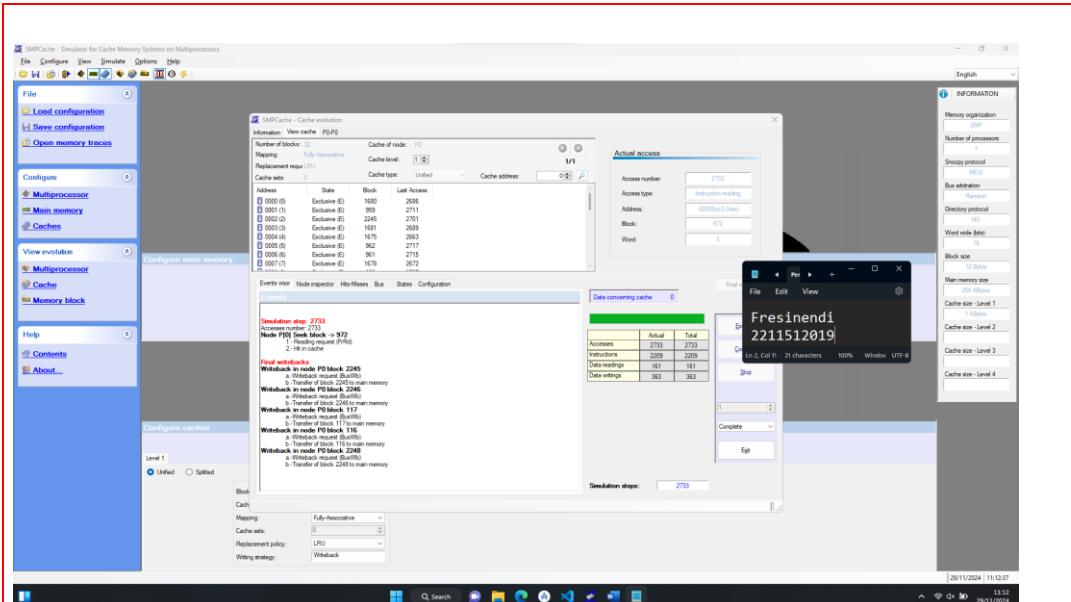
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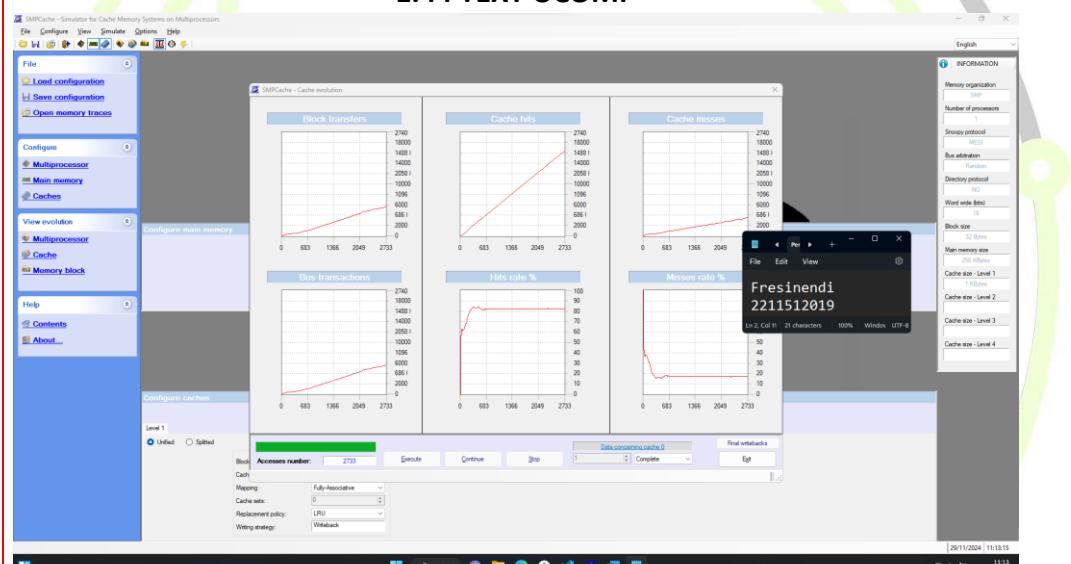
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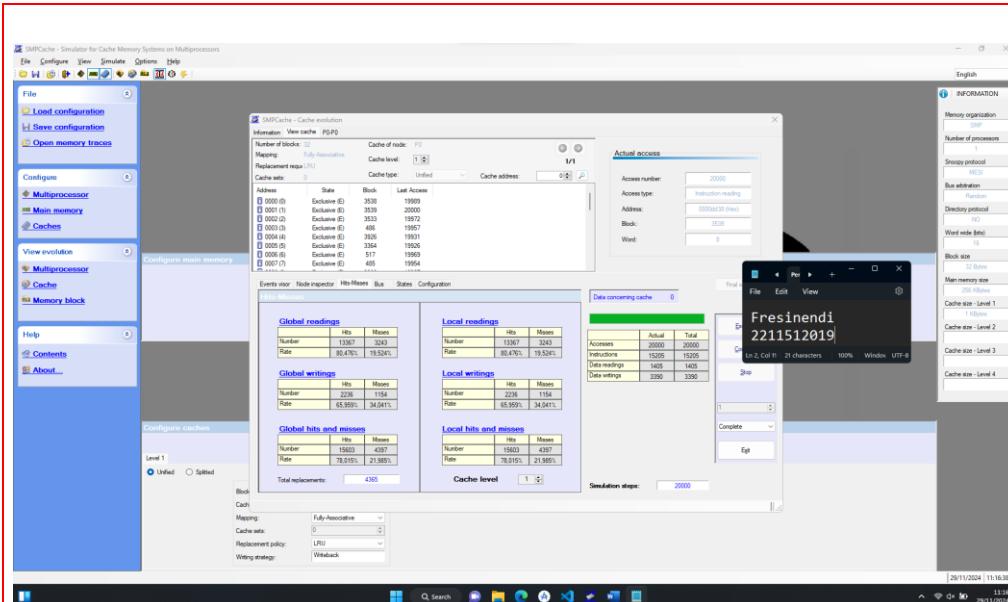


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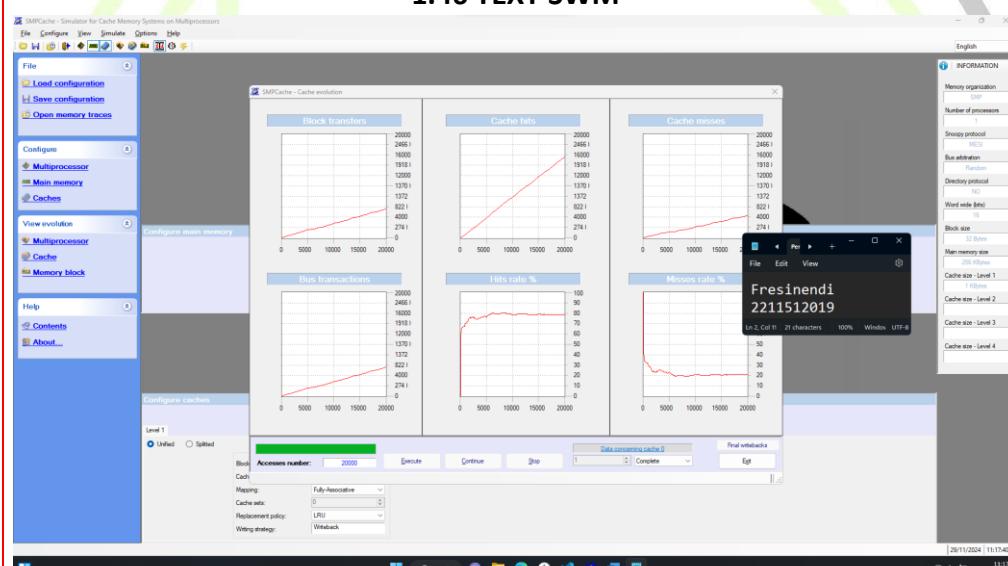


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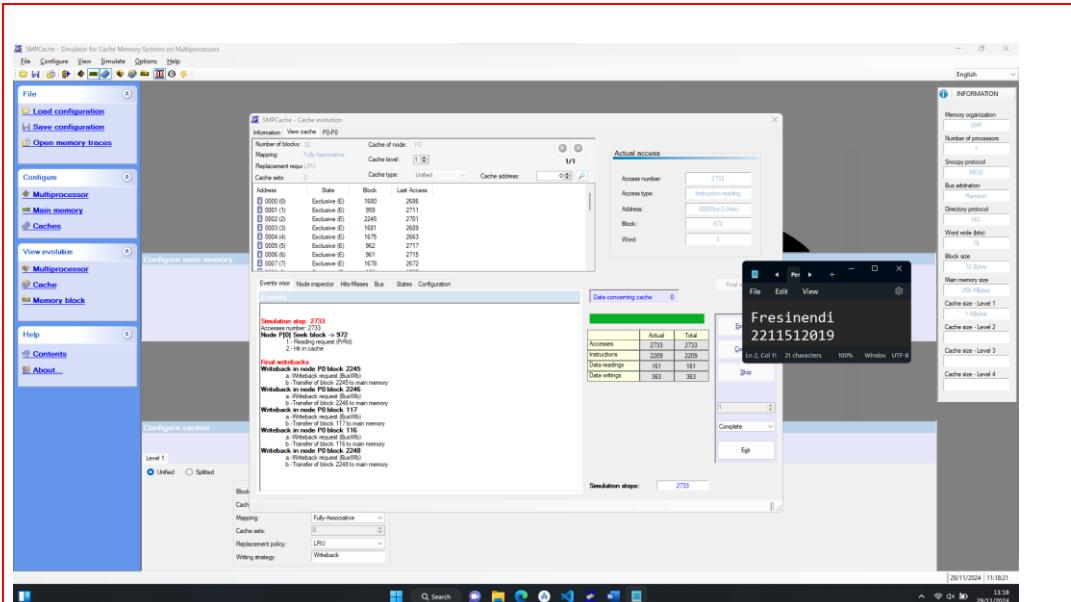
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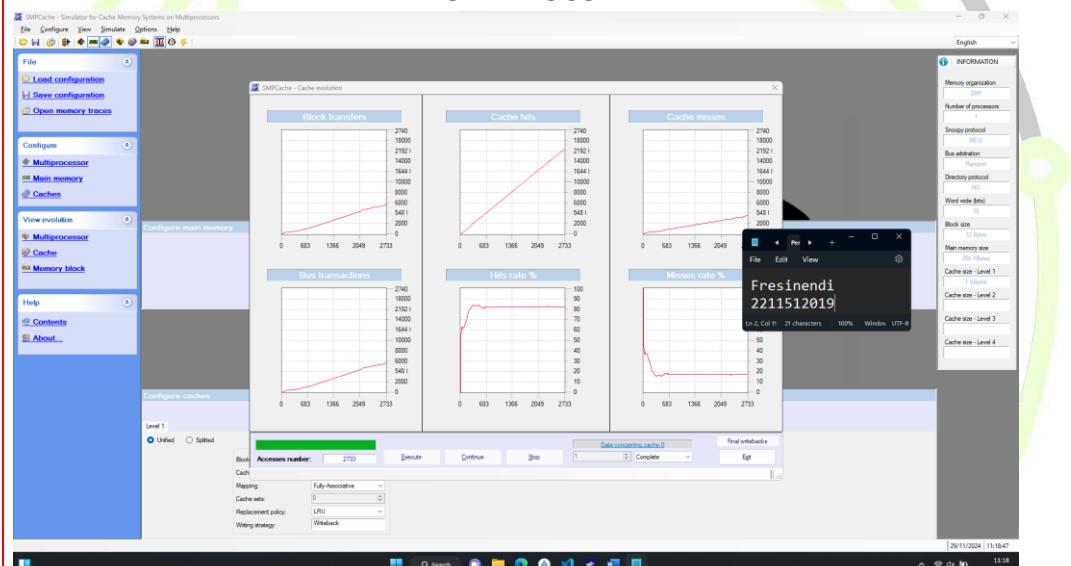
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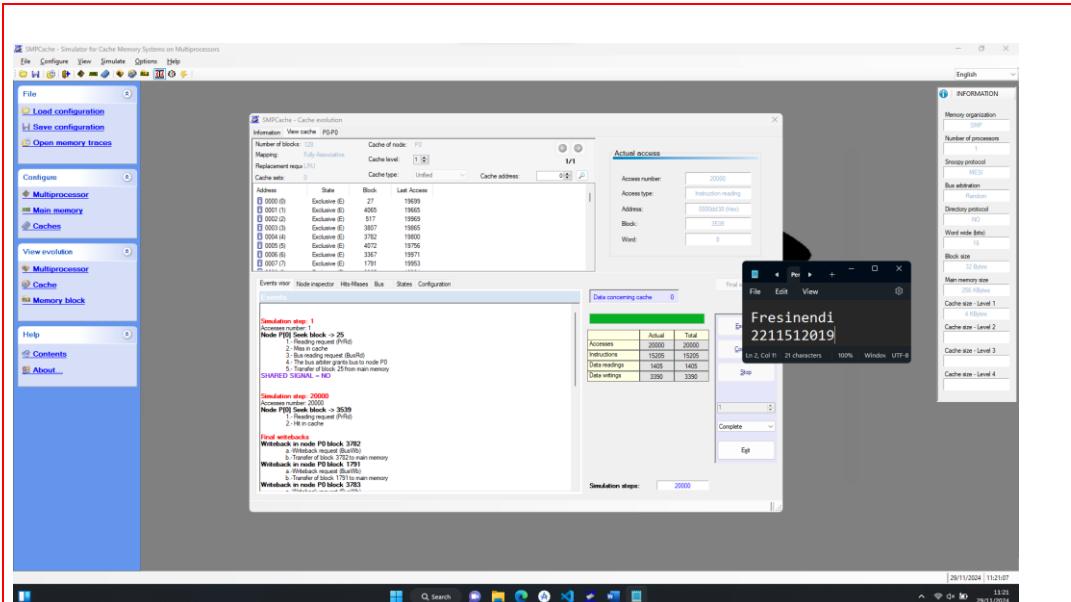


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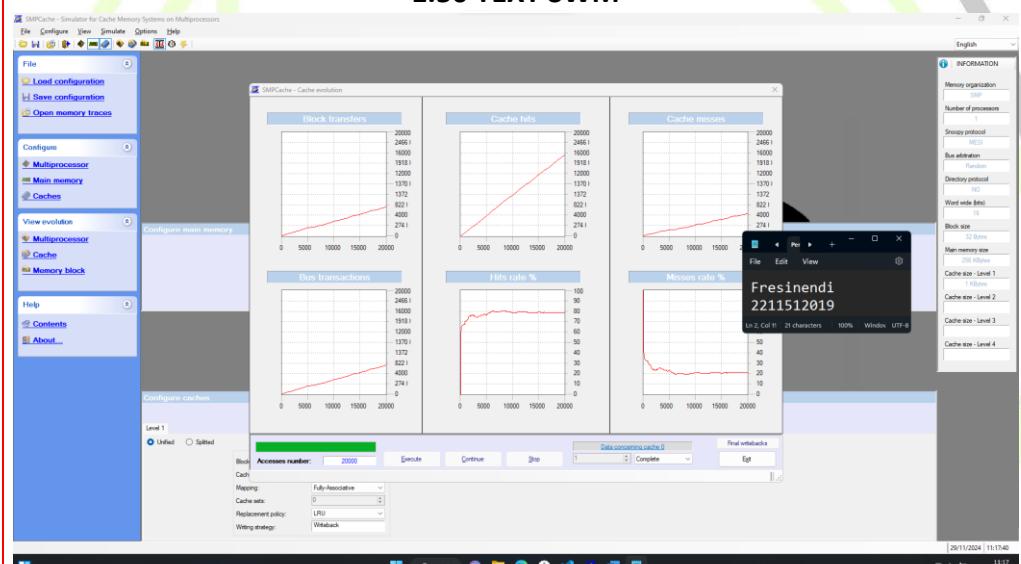


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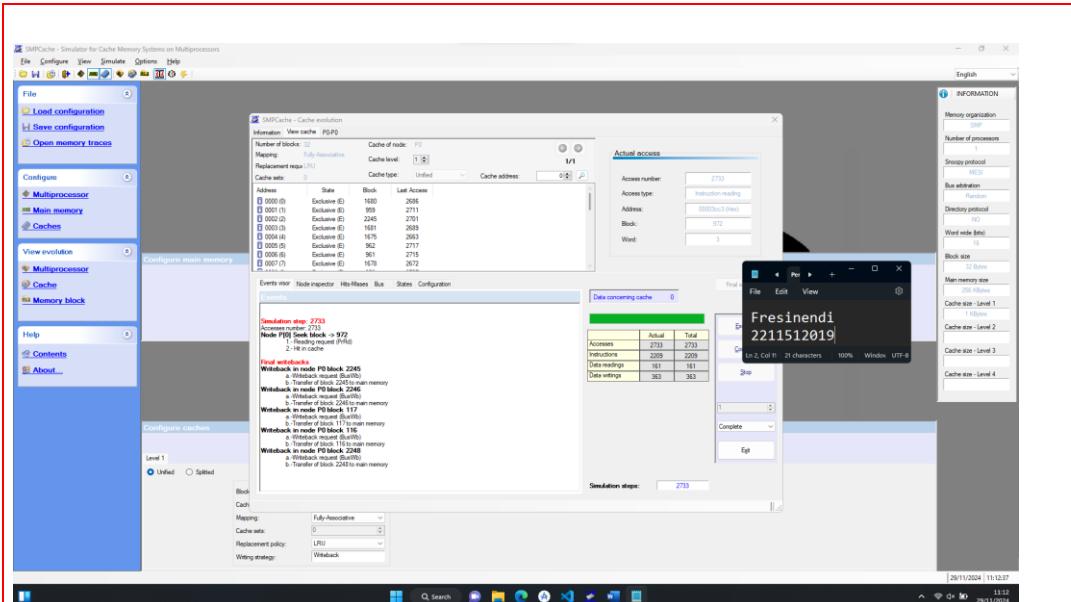
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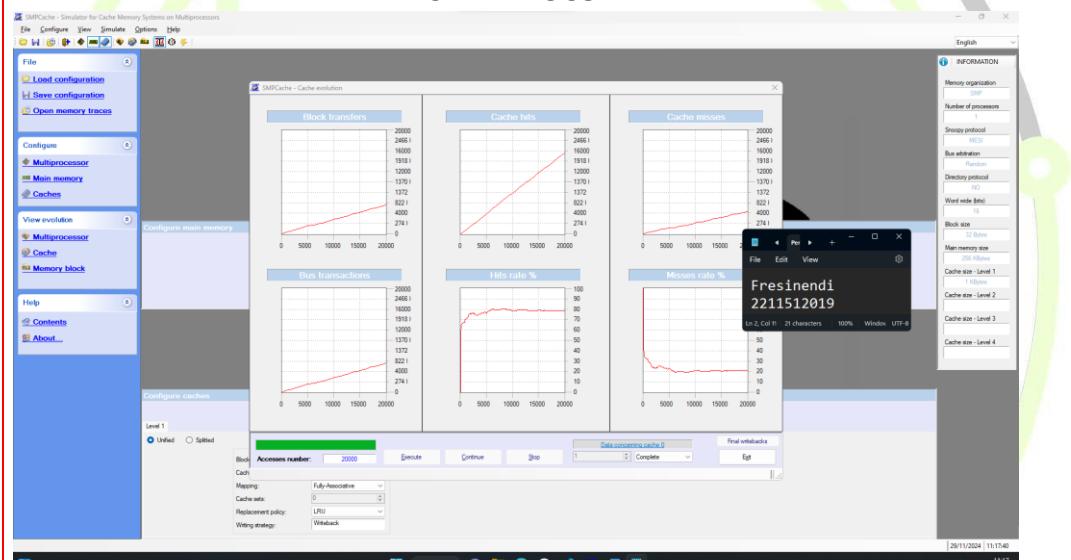
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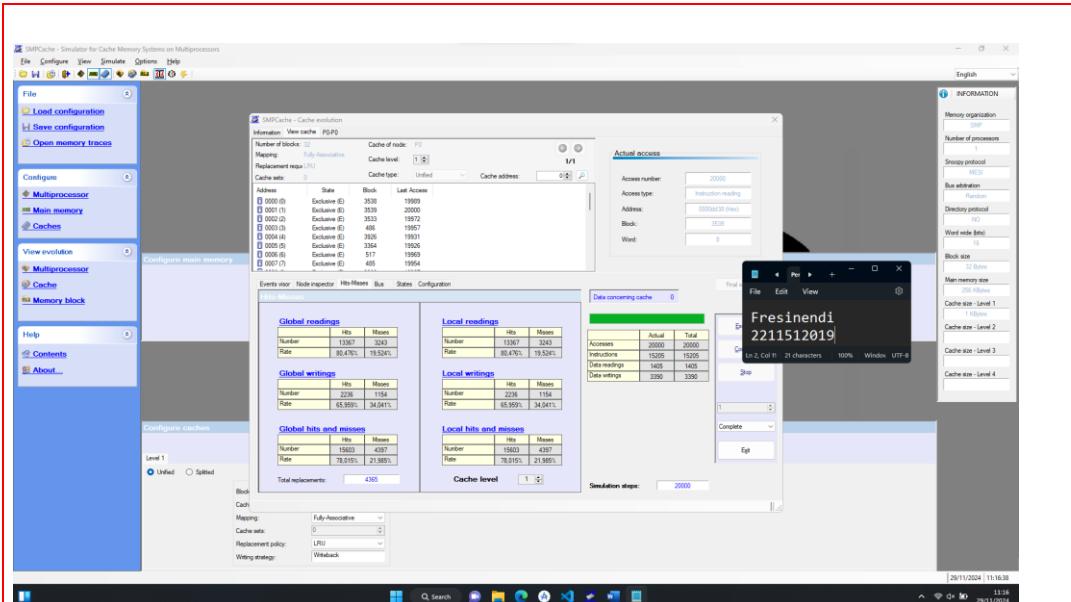


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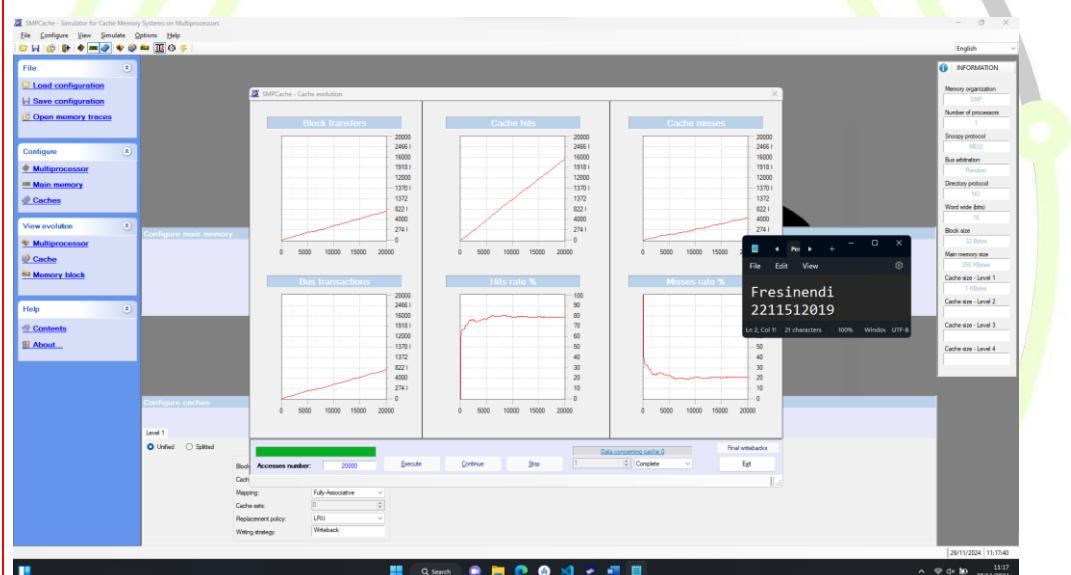


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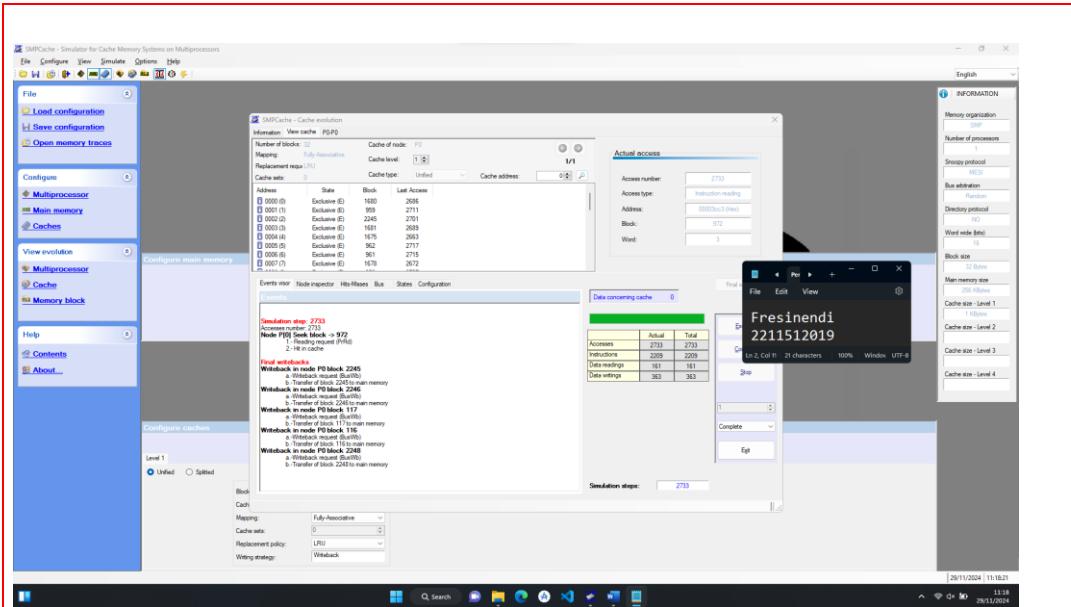
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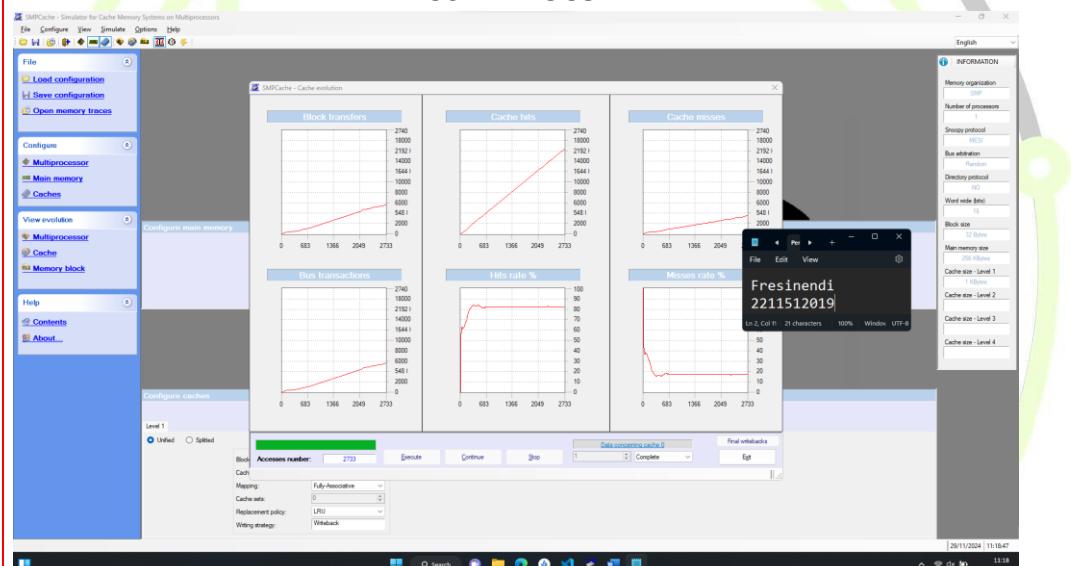
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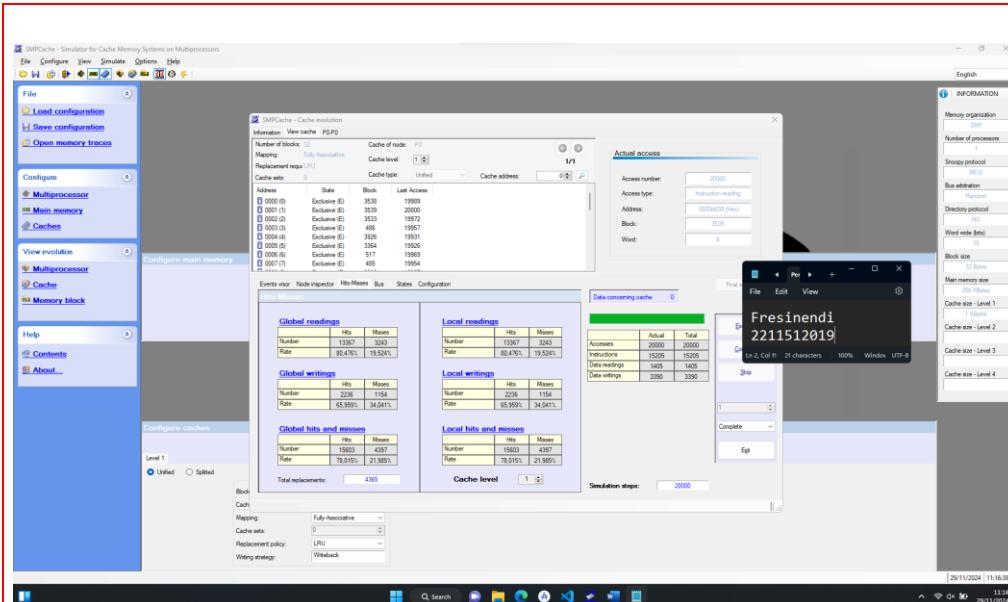


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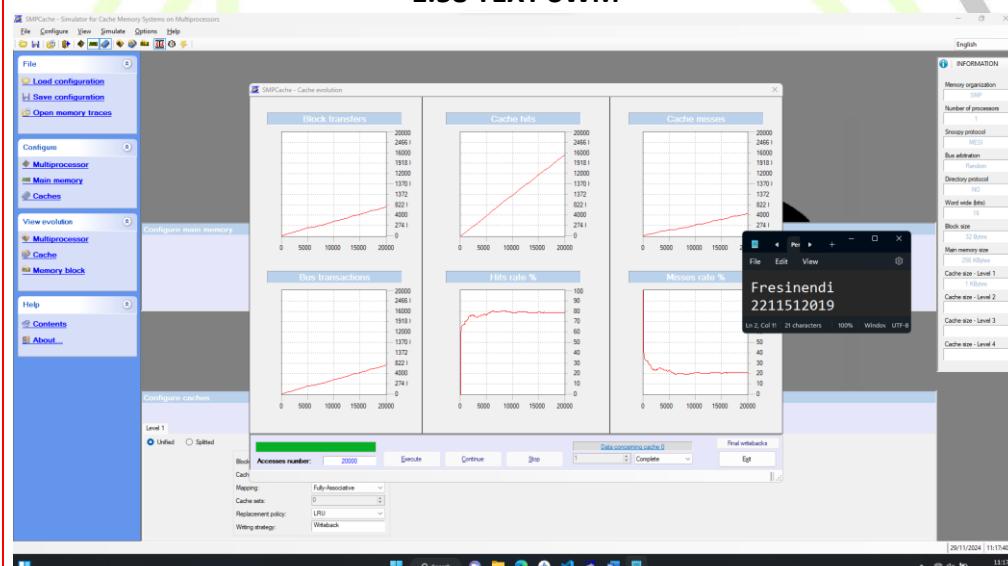


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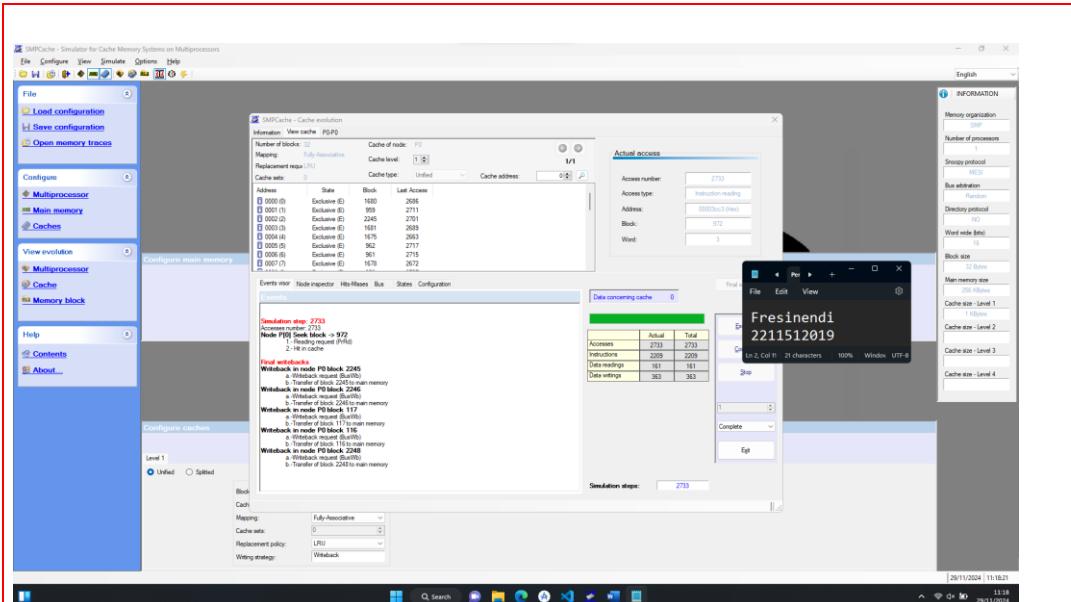
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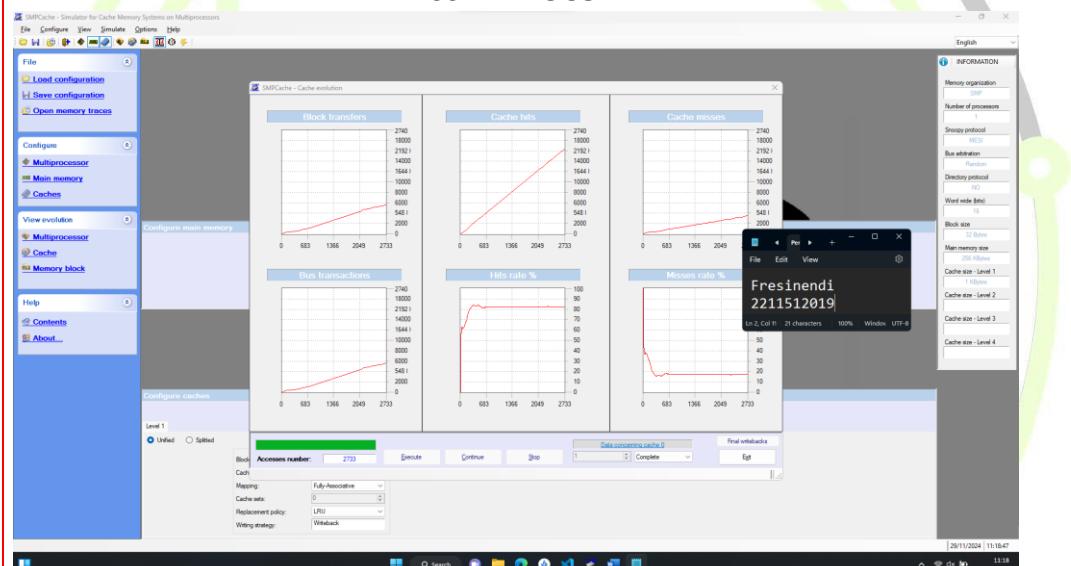
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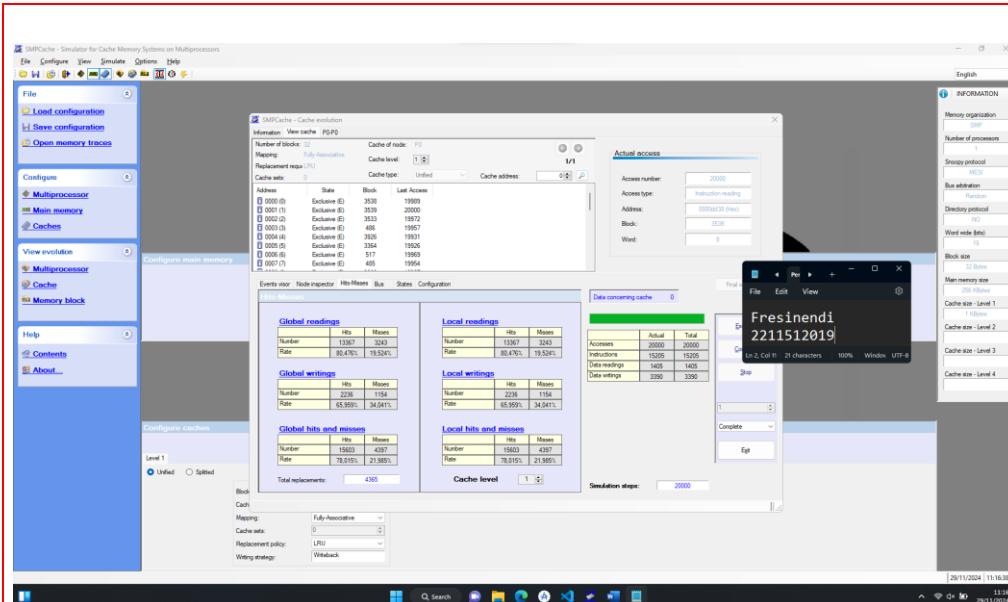


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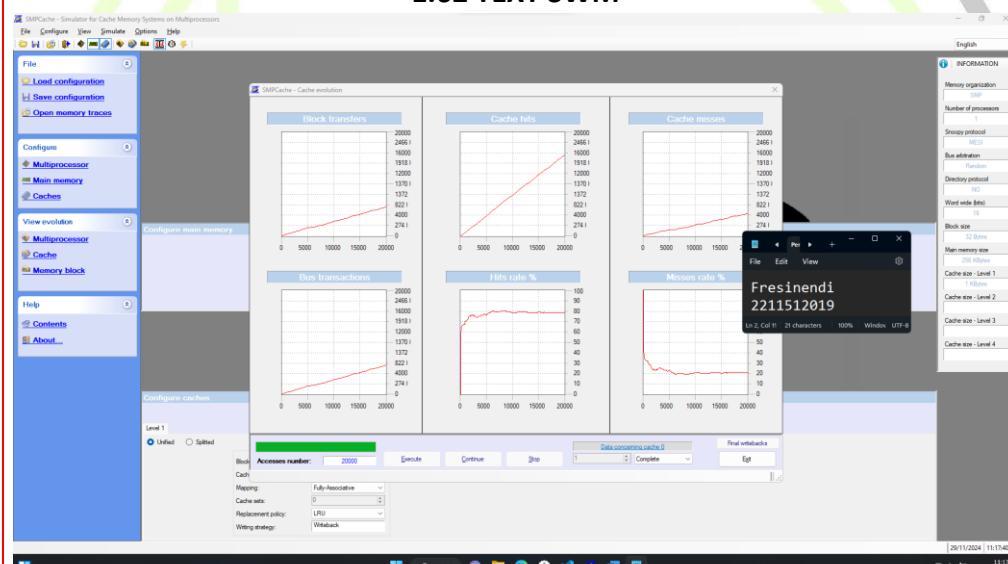


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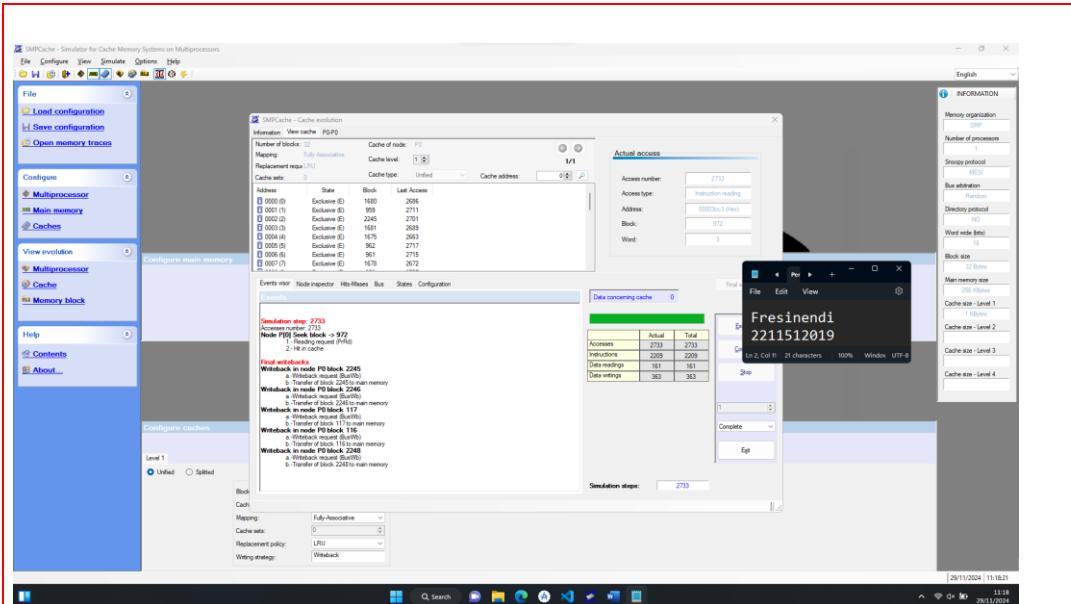
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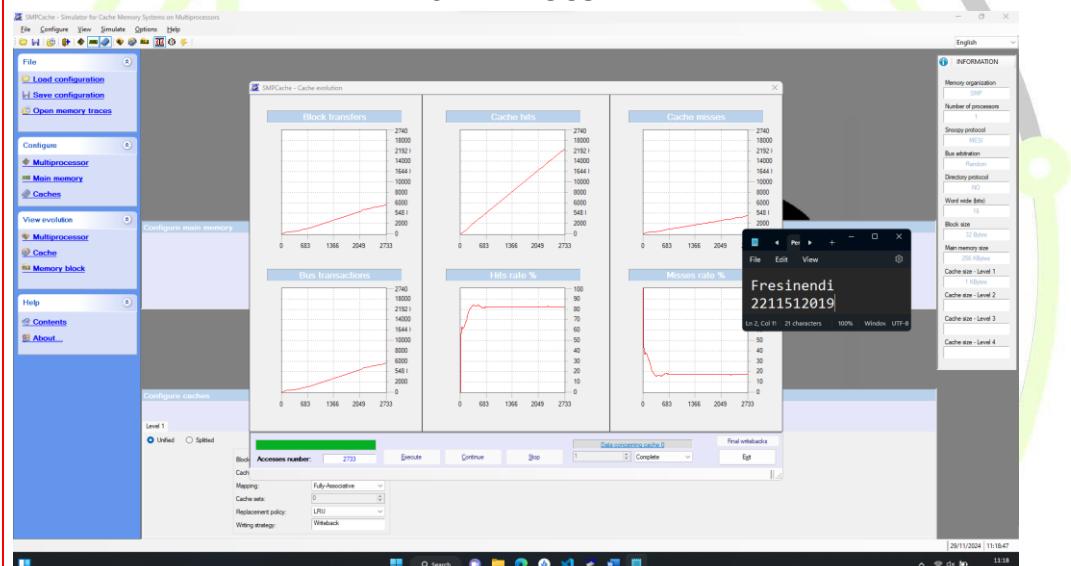
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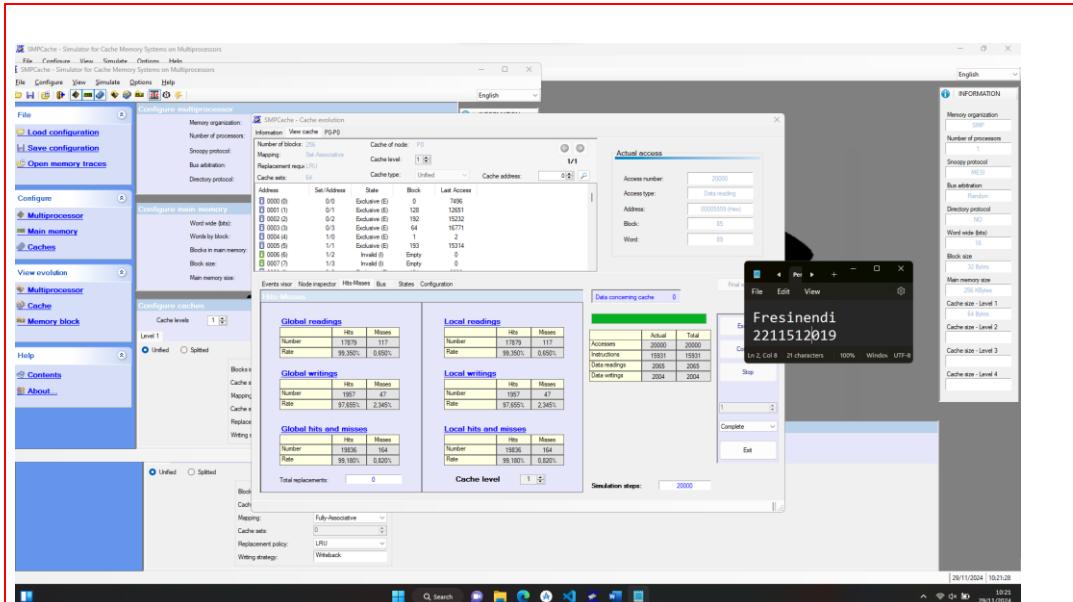


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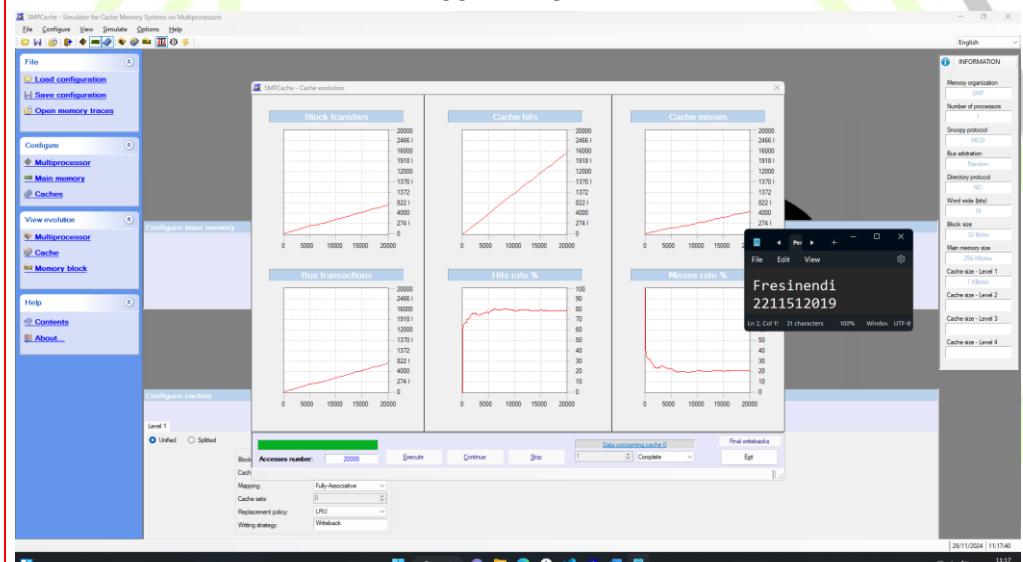


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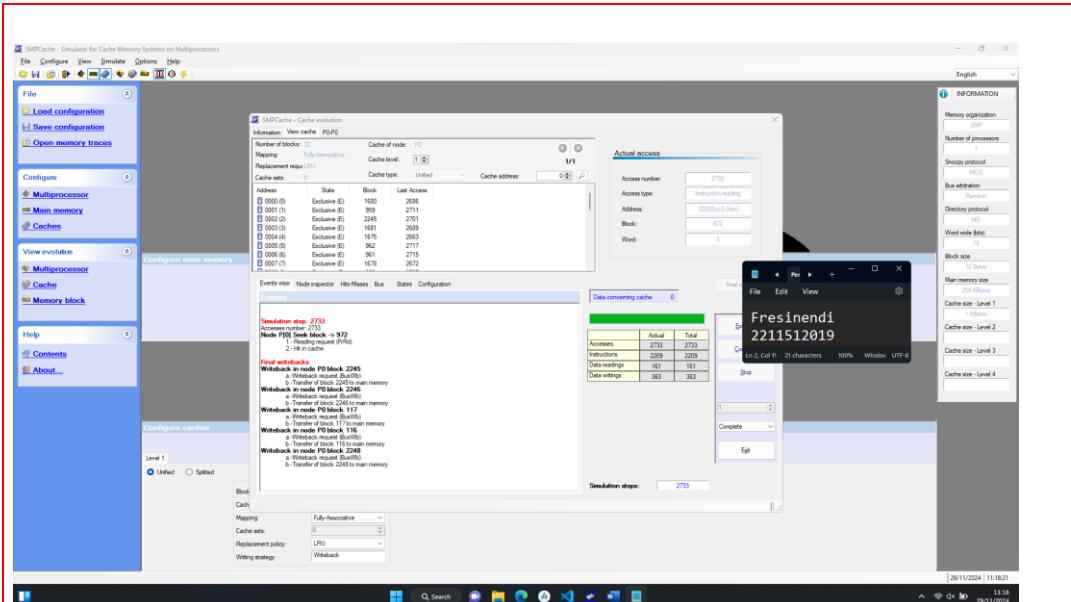
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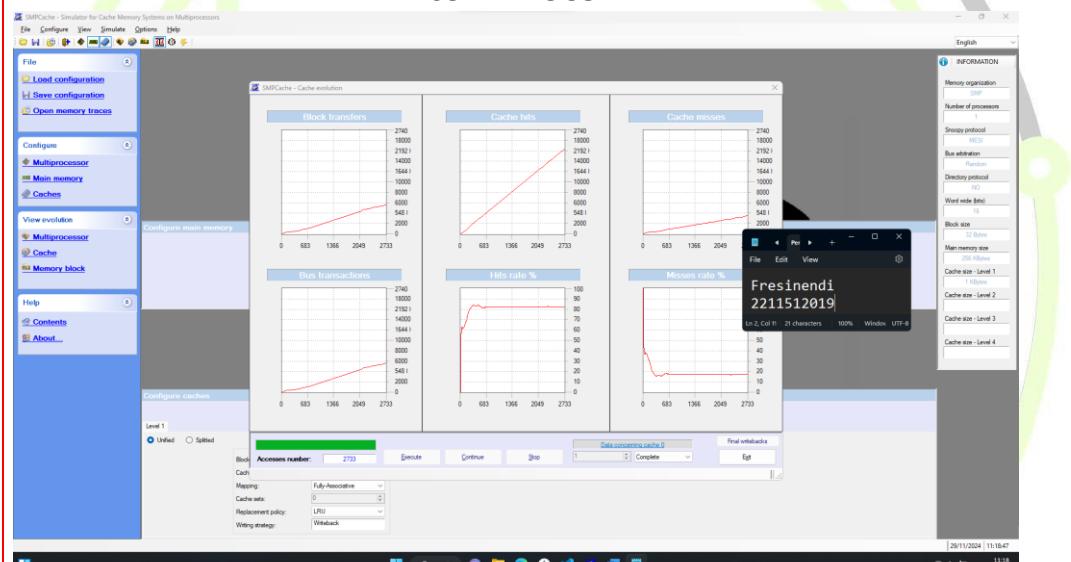
1.66 TEXT SWM



1.67 GRAPHIC SWM



1.68 TEXT UCOM



1.69 GRAPHIC SWM

PERTANYAAN

1.5.1 PERCOBAAN 1: PENGARUH UKURAN CACHE

- a. Miss rate menurun seiring meningkatnya ukuran cache karena lebih banyak data dapat disimpan, mengurangi *capacity misses*. Penurunan ini bergantung pada pola lokalitas tiap program. Program dengan lokalitas tinggi akan lebih signifikan.
- b. Saat cache membesar:
 - *Capacity misses* menurun karena lebih banyak data tertampung.
 - *Conflict misses* tidak ada dalam *fully-associative mapping* yang digunakan di eksperimen ini, karena blok dapat ditempatkan di mana saja.
- c. Miss rate stabil saat cache cukup besar untuk menyimpan data yang sering diakses. Hal ini menunjukkan bahwa semua data penting sudah tertampung.
- d. Perbedaan miss rate besar terjadi saat ukuran cache mencapai titik di mana kapasitas cukup untuk mengurangi *misses* signifikan. Titik ini dapat berbeda antar program karena pola akses data berbeda.
- e. Ya, peningkatan ukuran cache meningkatkan kinerja dengan menurunkan *miss rate*, tetapi manfaatnya akan berkurang setelah mencapai ukuran tertentu.

1.5.2 PERCOBAAN 1: PENGARUH UKURAN BLOCK

- a. Miss rate awalnya menurun karena ukuran block yang lebih besar meningkatkan *spatial locality*. Namun, setelah titik tertentu, miss rate dapat meningkat karena *cache pollution*.
- b. Penurunan atau kenaikan bergantung pada nilai lokalitas program. Program dengan *spatial locality* tinggi lebih diuntungkan oleh block besar.
- c. *Compulsory misses* menurun karena block yang lebih besar membawa lebih banyak data yang relevan dalam sekali fetch.
- d. **Pollution point** terjadi saat block terlalu besar sehingga data yang jarang diakses menggantikan data penting, meningkatkan miss rate. Ini dapat muncul dalam eksperimen jika block terlalu besar untuk pola akses tertentu.
- e. Peningkatan ukuran block meningkatkan kinerja hingga batas tertentu, tetapi setelah melewati *pollution point*, kinerja dapat menurun.