浙江大学
ZHEJIANG UNIVERSITY

Computer Architecture Experiment

Topic 5. Dynamically Scheduled Pipelines using Scoreboarding

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Outline

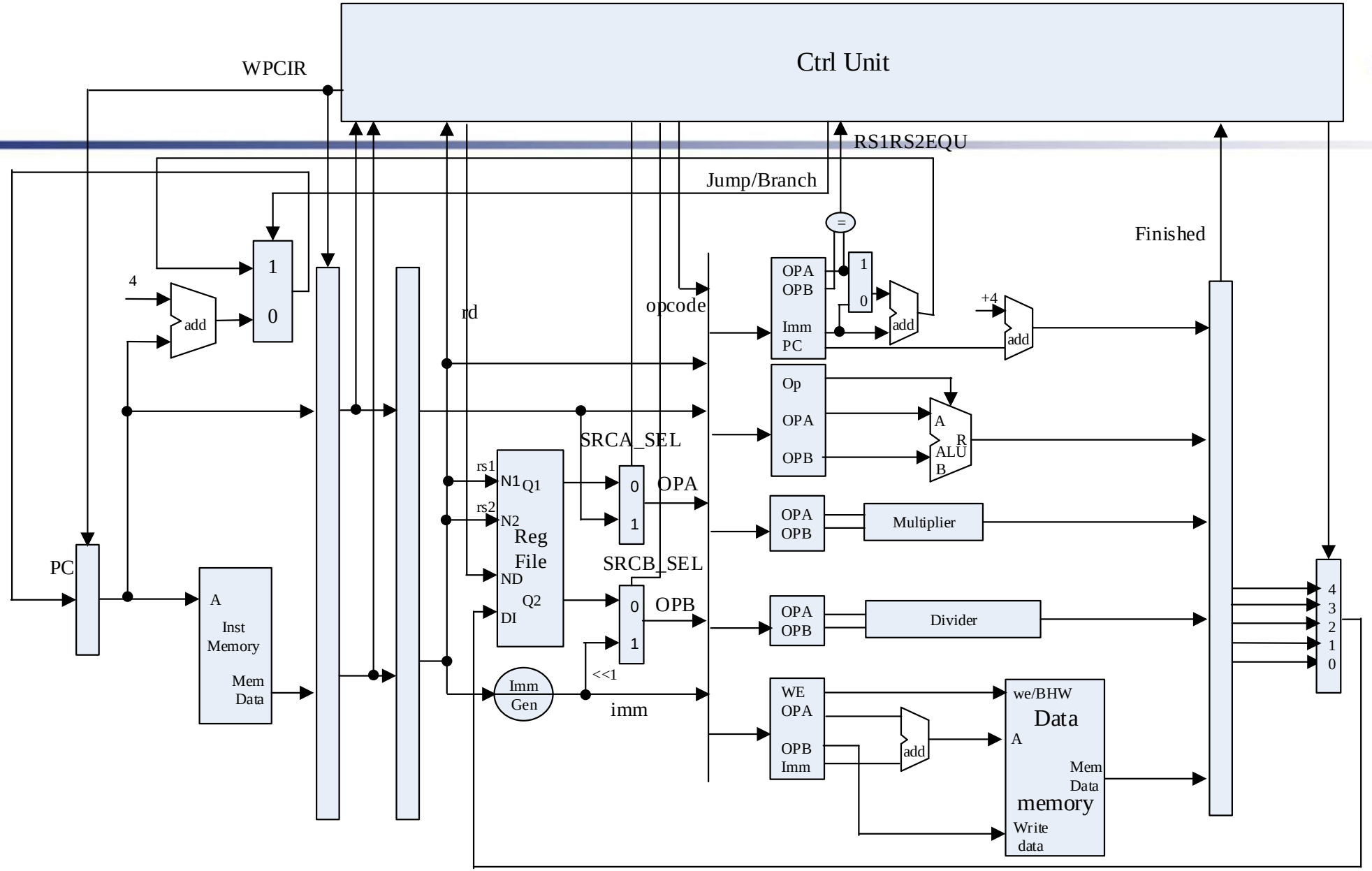
- Experiment Purpose
- Experiment Task
- Basic Principle
- Operating Procedures
- Checkpoints

Experiment Purpose

- Understand the principle of piplines that support multicycle operations.
- Understand the principle of Dynamic Scheduling With a Scoreboard.
- Master the design methods of piplines that support multicycle operations.
- Master the design methods of Dynamically Scheduled Pipelines using Scoreboarding.
- Master verification methods of Dynamically Scheduled Pipelines using Scoreboarding.

Experiment Task

- **Redesign the pipelines with IF/IS/RO/FU/WB stages and supporting multicycle operations.**
- **Design of a scoreboard and integrate it to CPU.**
- **Verify the Pipelined CPU with program and observe the execution of program.**


Ctrl Unit
WPCIR
RS1RS2EQU
Jump/Branch
Finished
4
add
1
0
rd
opcode
OPA
OPB
Imm
PC
=
+4
Op
A
ALU
R
B
SRCA_SEL
SRCB_SEL
rs1
rs2
N1
Q1
N2
Reg
File
ND
Q2
DI
OPA
OPB
PC
A
Inst
Memory
Mem
Data
Imm
Gen
<<1
imm
Multiplier
Divider
WE
we/BHW
Data
memory
Write
data
4
3
2
1
0

Instr. Mem.(1)

NO.	Instruction	Addr.	Label	ASM	Comment
0	00000013	0	__start:	addi x0, x0, 0	
1	00402103	4		lw x2, 4(x0)	
2	00802203	8		lw x4, 8(x0)	Structural Hazard
3	004100b3	C		add x1, x2, x4	
4	fff08093	10		addi x1, x1, -1	WAW
5	00c02283	14		lw x5, 12(x0)	
6	01002303	18		lw x6, 16(x0)	
7	01402383	1C		lw x7, 20(x0)	
8	402200b3	20		sub x1,x4,x2	
9	ffd50093	24		addi x1,x10,-3	
10	00520c63	28		beq x4,x5,label0	
11	00420a63	2C		beq x4,x4,label0	
12	00000013	30		addi x0,x0,0	
13	00000013	34		addi x0,x0,0	
14	00000013	38		addi x0,x0,0	

Instr. Mem.(2)

NO.	Instruction	Addr.	Label	ASM	Comment
15	00000013	3C		addi x0,x0,0	
16	000040b7	40	label0:	lui x1,4	
17	00c000ef	44		jal x1,12	
18	00000013	48		addi x0,x0,0	
19	00000013	4C		addi x0,x0,0	
20	ffff0097	50		auipc x1, 0xffff0	
21	0223c433	54		div x8, x7, x2	
22	025204b3	58		mul x9, x4, x5	
23	022404b3	5C		mul x9, x8, x2	St. Ha./RAW/WAW
24	00400113	60		addi x2, x0, 4	WAR
25	000000e7	64		jalr x1,0(x0)	
26	00000013	68		addi x0,x0,0	
27	00000013	6C		addi x0,x0,0	

Data Mem.

NO.	Data	Addr.	Comment
0	000080BF	0	
1	00000008	4	
2	00000010	8	
3	00000014	C	
4	FFFF0000	10	
5	0FFF0000	14	
6	FF000F0F	18	
7	F0F0F0F0	1C	
8	00000000	20	
9	00000000	24	
10	00000000	28	
11	00000000	2C	
12	00000000	30	
13	00000000	34	
14	00000000	38	
15	00000000	3C	

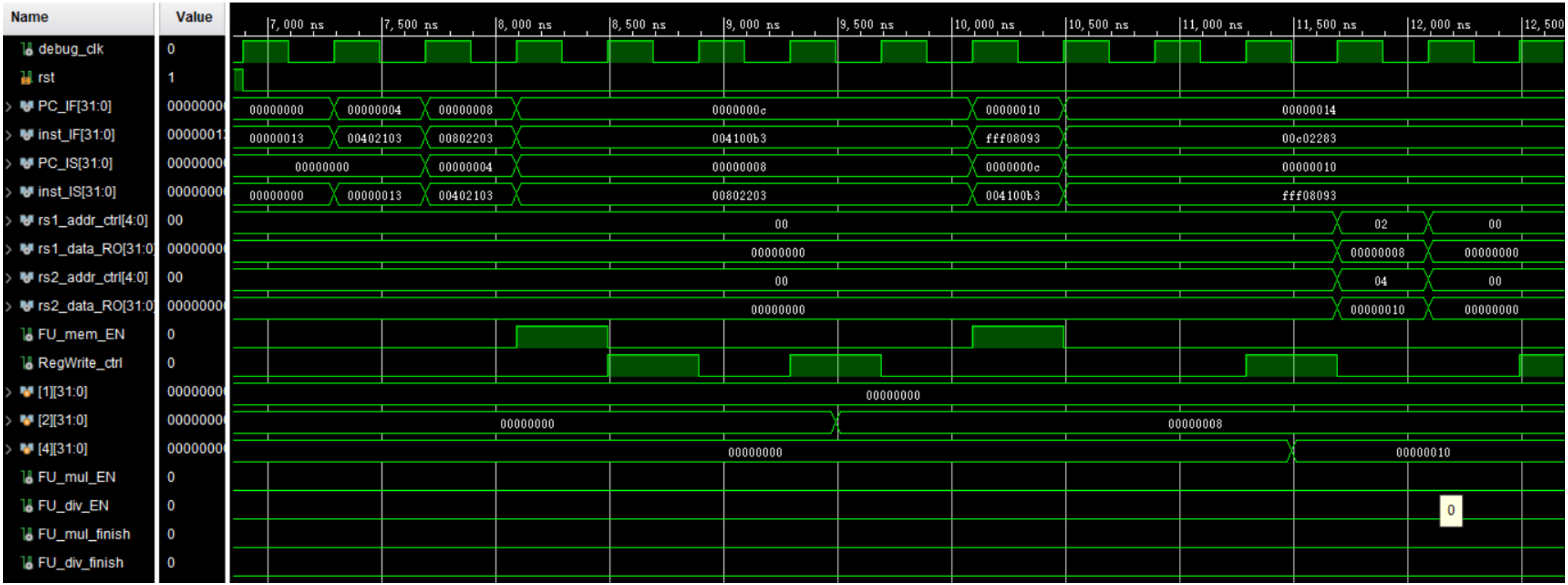
NO.	Instruction	Addr.	Comment
16	00000000	40	
17	00000000	44	
18	00000000	48	
19	00000000	4C	
20	A3000000	50	
21	27000000	54	
22	79000000	58	
23	15100000	5C	
24	00000000	60	
25	00000000	64	
26	00000000	68	
27	00000000	6C	
28	00000000	70	
29	00000000	74	
30	00000000	78	
31	00000000	7C	

Test Bench

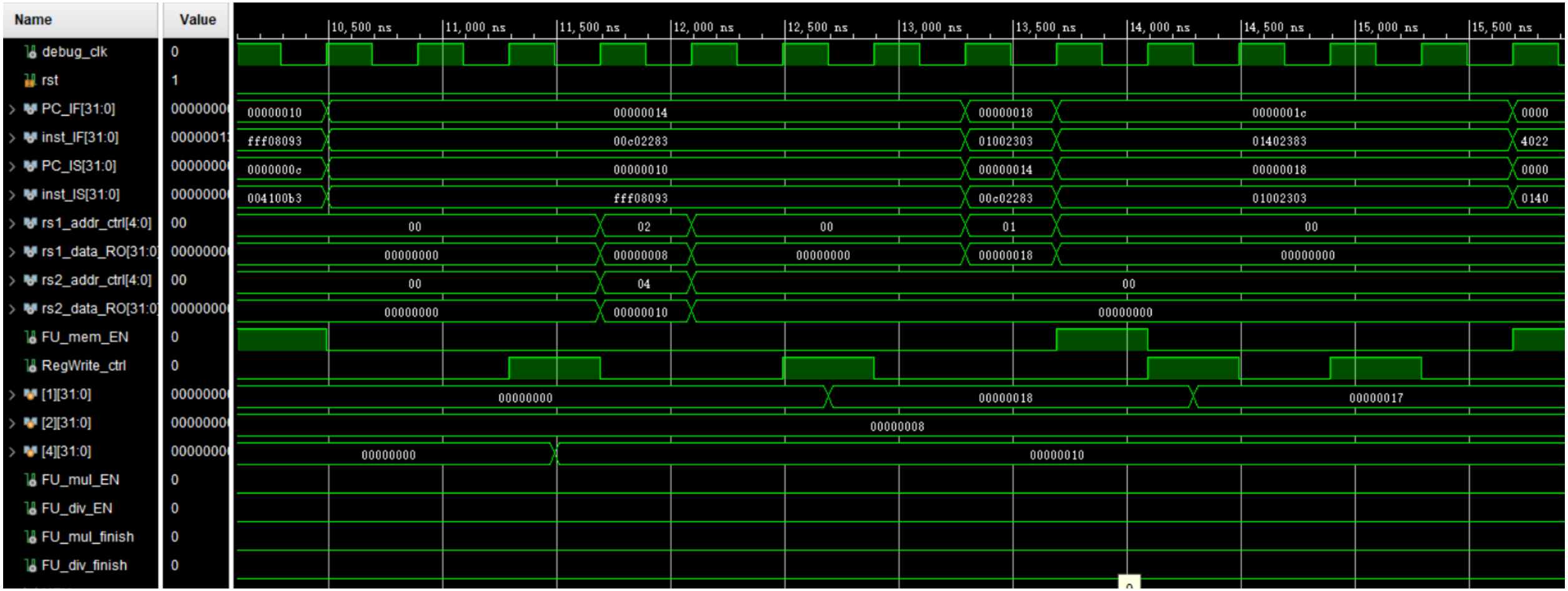
```
RV32core core(
    .debug_en(1'b0),
    .debug_step(1'b0),
    .debug_addr(7'b0),
    .debug_data(),
    .clk(clk),
    .rst(rst),
    .interrupter(1'b0)
);

initial begin
    clk = 0;
    rst = 1;
    #2 rst = 0;
end
always #1 clk = ~clk;
```

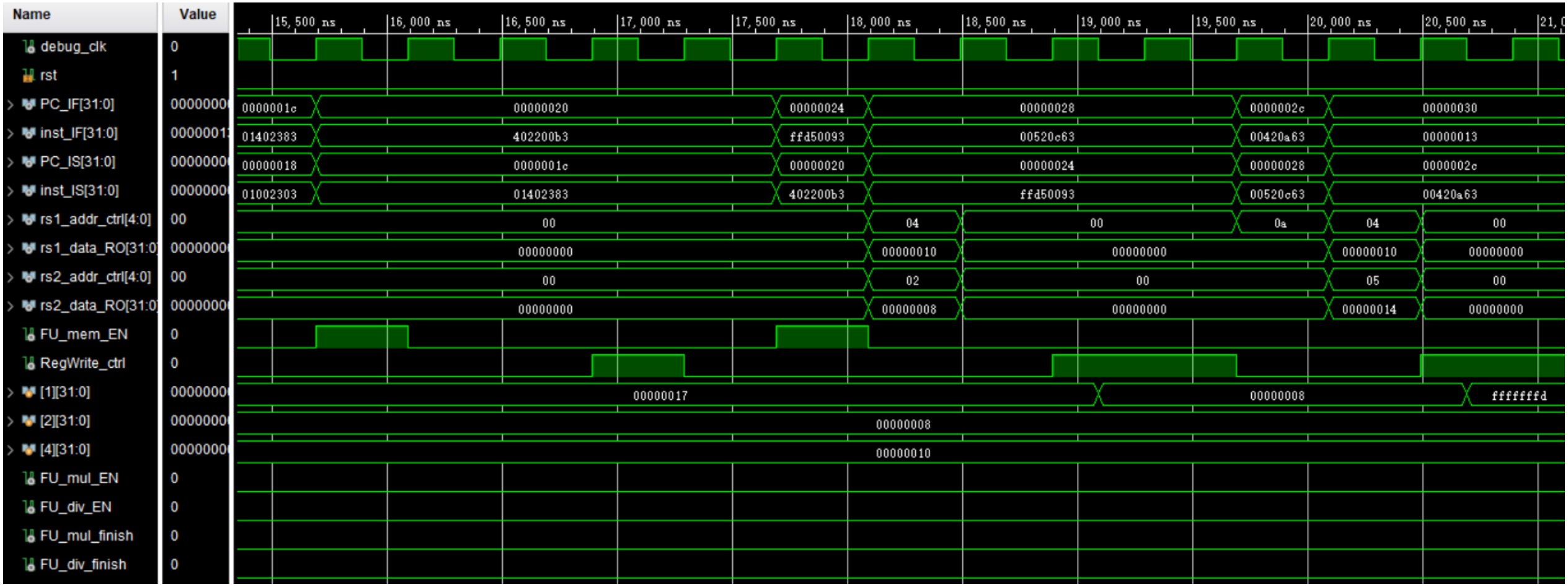
Simulation (1)



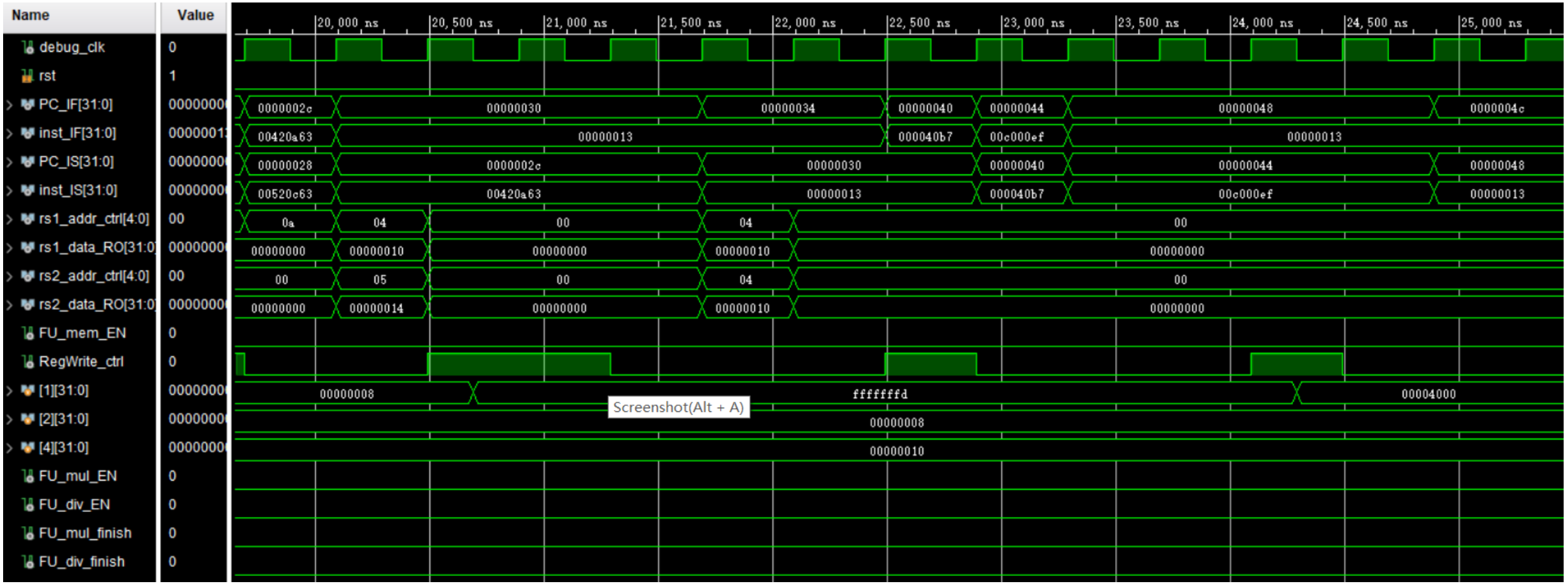
Simulation (2)



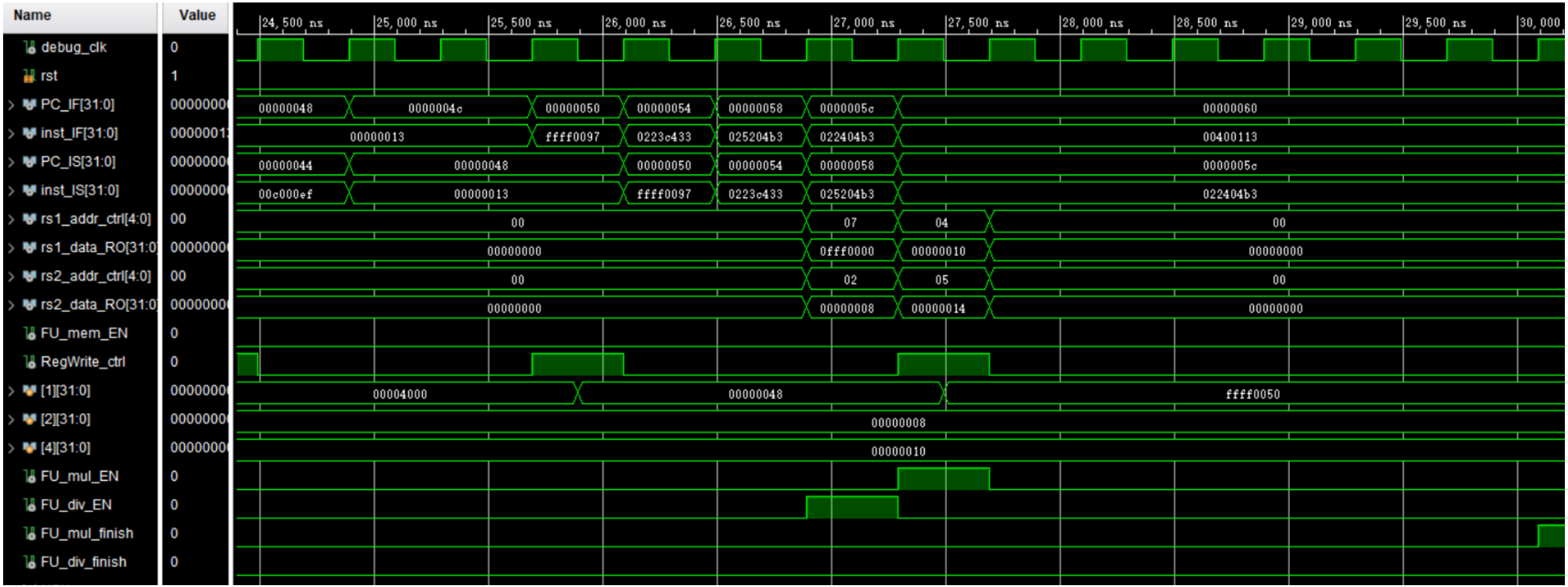
Simulation (3)



Simulation (4)

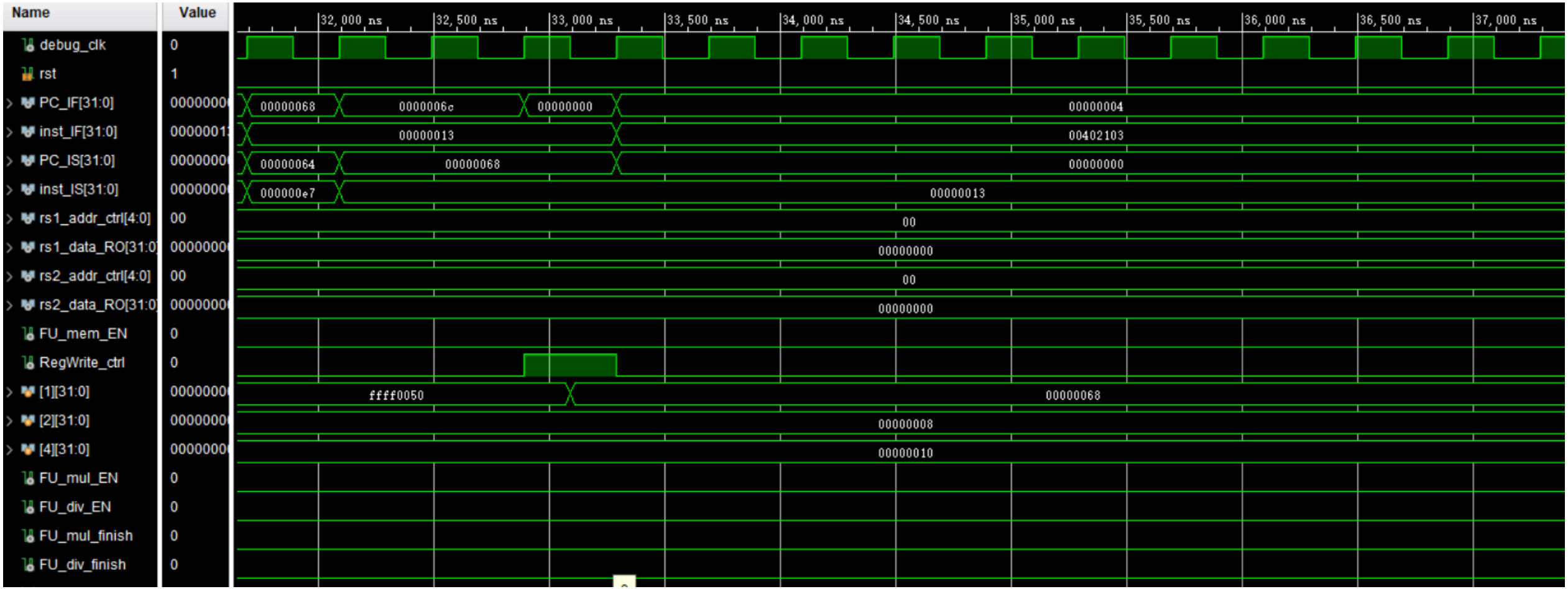


Simulation (5)

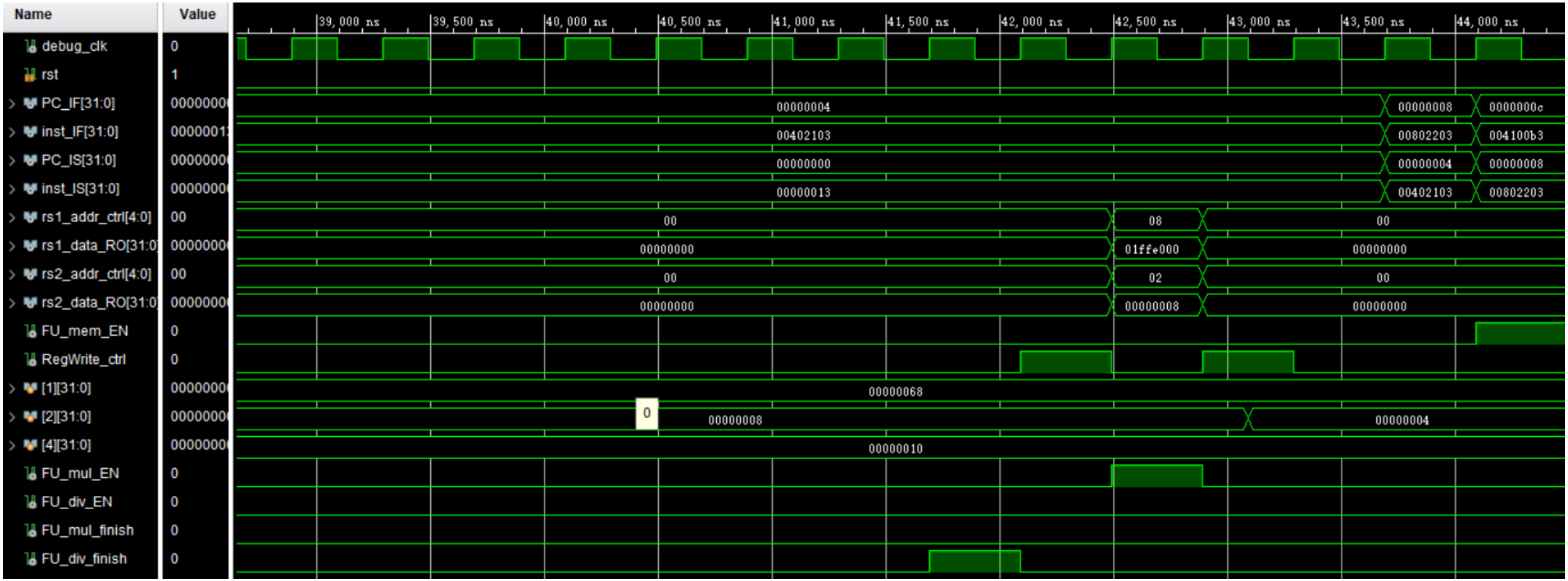


Simulation (6)

Simulation (7)



Simulation (8)



Checkpoints

- **CP 1:**

  Waveform Simulation of the Pipelined CPU with the verification program

- **CP 2:**

  FPGA Implementation of the Pipelined CPU with the verification program

Thanks!