1

(a)
Baseline performance = 36 cycles per loop iteration
(b)
depencency:

- `I1` depends on `I0` (register `f2`).
- `I2` is independent.
- `I3` depends on `I2` (register `f4`).
- `I4` depends on `I1` (register `f8`) and `I3` (register `f10`).
- `I5` depends on `I4` (register `f4`).
- `I6`, `I7`, and `I8` are independent.
- `I9` depends on `I8` (register `x20`).

Instruction	IF/IS	FU Start	WB
I0	0	1	5
I1	0	5	15
I2	0	6	9
I3	0	10	13
I4	0	14	16
I5	0	17	18
I6	0	18	19
I7	0	19	20
I8	0	20	21
I9	0	21	22

(c)

Instruction	Cycle Issued	Cycle FU Start	Cycle WB
I0	0	1	5
I1	0	1	11
I2	1	2	5
I3	1	2	4
I4	2	3	5
I5	3	4	5
I6	3	4	4
I7	4	5	5
I8	4	5	6
I9	5	6	7

2

(1) What is VLIW

VLIW, which is abbreviation of Very Long Instruction Word, is a computer architecture technique that allows multiple instructions to be issued and executed in parallel within a single clock cycle. It relies on the compiler to perform instruction scheduling and dependency analysis, rather than having complex hardware handle these tasks dynamically.

(2) How to solve RAW and WAR

It relies on compiler to schedule the instruction so that no RAW and WAR hazard would happens in one instruction sequence.

(3) Adavantages and Disadvantages

Adavantages: Reduce complexity of hardware design, The execution order is more predictable

Disadvantages: It highly depend on compiler, bigger Instruction size can leads to bigger binary size

3

(a)

Cycle	lw x3,0(x0)	lw x1,0(x3)	addi x1,x1,1	sub x4,x3,x2	sw x1,0(x3)	bnz x4,Loop
1	F					
2	D	F				
3	E	D	F			
4	M	E	D	F		
5	Stall	Stall	Stall	D	F	
6	Stall	Stall	Stall	Stall	D	F
7	W	M	Stall	Stall	Stall	D
8		Stall	Stall	Stall	Stall	Stall
9		Stall	Stall	Stall	Stall	Stall
10		W	E	Stall	Stall	Stall
11			M	E	Stall	Stall
12			W	M	E	Stall
13				W	M	E
14					Stall	M
15					Stall	Stall
16					W	Stall
17						W

over head = 14 - 7 - 1 = 6 cycles

(b) 1 cycle

(c) 0 cycle