1.You are tasked with designing a new processor microarchitecture and you are trying to determine how best to allocate your hardware resources. Which of the hardware and software techniques you learned in Chapter 3 should you apply? You have a list of latencies for the functional units and for memory, as well as some representative code. Your boss has been somewhat vague about the performance requirements of your new design, but you know from experience that, all else being equal, faster is usually better. Start with the basics. Figure below provides a sequence of instructions and list of latencies.

提示：假设取指、译码和发射共用同一个周期，WB需要一个周期，也就是说，下图I0指令假设在第5周期将结果写回f2，则I1指令的执行阶段从第六周期开始

Latencies beyond single cycle	
Memory LD	+3
Memory SD	+1
Integer ADD, SUB	+0
Branches	+1
fadd.d	+2
fmul.d	+4
fdiv.d	+10

```
Loop:   fld     f2,0(Rx)
I0:     fmul.d  f2,f0,f2
I1:     fdiv.d  f8,f2,f0
I2:     fld     f4,0(Ry)
I3:     fadd.d  f4,f0,f4
I4:     fadd.d  f10,f8,f2
I5:     fsd     f4,0(Ry)
I6:     addi    Rx,Rx,8
I7:     addi    Ry,Ry,8
I8:     sub     x20,x4,Rx
I9:     bnz     x20,Loop
```

a. What is the baseline performance (in cycles, per loop iteration) of the code sequence in the Figure if no new instruction's execution could be initiated until the previous instruction's execution had completed? Assume for now that execution does not stall for lack of the next instruction, but only one instruction/cycle can be issued. （假设所有的指令都在同一个FU执行，但是不同指令有不同的latency，因此，每条指令都是等待前一条的FU执行完写回之后再去进入，比如I0指令在第五周期进入WB，那I1就从第六周期开始）

Instruction	IF/IS	FU	WB
I0	0	1	.....
I1	1	...	
...			

b. List the dependency relation of previous code list,
(for example, f2 in I1 depends on the outcome of I0)

and consider if there are different and infinitely function unit, what's the table below will look like?

(假设有无限个Function unit，重新填写上面那张表)

c. suppose your machine can issue two instruction at one time, what will the table look like? (假设一次能发射两条指令，FU数量仍为无限个)

2. 介绍一下VLIW技术，谈一下他是怎么解决RAW和WAR冒险的，他的优缺点在哪（发现照抄GPT的视为0分）

3. Assume a five-stage single-pipeline microarchitecture (fetch, decode, execute, memory, write-back) and the code. All ops are one cycle except LW and SW, which are 1+2 cycles, and branches, which are 1+1 cycles. There is no forwarding. 本题需要给出过程，否则不给分。

Loop:

lw x3,0(x0)

lw x1,0(x3)

addi x1,x1,1

sub x4,x3,x2

sw x1,0(x3)

bnz x4, Loop

a. [10] Show the phases of each instruction per clock cycle for one iteration of the loop. How many clock cycles per loop iteration are lost to branch overhead?

提示：画表，每行代表一条指令，每列代表一个cycle，内容填写FDEMW五种阶段和 - (stall)，这里WB和EX可以同时发生，比如假设第一条指令在第七周期WB，则依赖于其结果的第二条指令第7周期直接进入execute阶段。

在表中要包括代码进入新一轮循环的第一条指令，其应该在跳转指令EX阶段结束后开始执行。

cycles per loop iteration are lost to branch overhead，是指跳转指令的fetch周期和第二轮循环第一条指令的fetch周期之间的差值减1，即若跳转指令fetch后第二轮循环第一条指令在下一周期立马fetch，视为0 overhead.

b. [10] Assume a static branch predictor, capable of recognizing a backward branch in the Decode stage. Now how many clock cycles are wasted on branch overhead?

c. [10] Assume a dynamic branch predictor. How many cycles are lost on a correct prediction?