

Lab3&4 勘误

2024.10.21

Lab3&4\lab3\design_sources\cache.v

此处应该是set to the not recent

```
88 always @ (*) begin
89     valid <= TO_BE_FILLED; // if both not hit, set to the recent value
90     dirty <= TO_BE_FILLED; // if both not hit, set to the recent value
91     tag <= TO_BE_FILLED; // if both not hit, set to the recent value
92     hit <= hit1 | hit2;
93     if (load & hit1) begin
94         dout <= u_b_h_w[1] ? word1 :
95             u_b_h_w[0] ? {u_b_h_w[2] ? 16'b0 : {16{half_word1[15]}}, half_word1} :
96             {u_b_h_w[2] ? 24'b0 : {24{byte1[7]}}, byte1};
97     end
98     else if (load & hit2) begin
99         dout <= u_b_h_w[1] ? word2 :
100             u_b_h_w[0] ? {u_b_h_w[2] ? 16'b0 : {16{half_word2[15]}}, half_word2} :
101             {u_b_h_w[2] ? 24'b0 : {24{byte1[7]}}, byte2};
102     end
103     else begin
104         dout <= recent1 ? word2 : word1;
105     end
106 end
```

Lab3&4\lab4\riscv_sources\riscv.txt

漏写了loop标号
可以在第一行补上

<pre>addi x0, x0, 0 lb x1, 0x01C(x0) lh x2, 0x01C(x0) lw x3, 0x01C(x0) lbu x4, 0x01C(x0) lhu x5, 0x01C(x0) lw x0, 0x210(x0) lui x1 0xABCDE sub x1, x4, x2 addi x1, x1, 0x71C sb x1, 0x0(x0) sh x1, 0x4(x0) sw x1, 0x8(x0) lw x6, 0x200(x0) lw x7, 0x400(x0) lw x8, 0x410(x0) ori x16, x0, 0xED jal x0, loop addi x0, x0, 0 addi x0, x0, 0 addi x0, x0, 0 addi x0, x0, 0 addi x0, x0, 0</pre>	<pre>loop: addi x0, x0, 0 lb x1, 0x01C(x0) lh x2, 0x01C(x0) lw x3, 0x01C(x0) lbu x4, 0x01C(x0) lhu x5, 0x01C(x0) lw x0, 0x210(x0) lui x1 0xABCDE sub x1, x4, x2 addi x1, x1, 0x71C sb x1, 0x0(x0) sh x1, 0x4(x0) sw x1, 0x8(x0) lw x6, 0x200(x0) lw x7, 0x400(x0) lw x8, 0x410(x0) ori x16, x0, 0xED jal x0, loop addi x0, x0, 0 addi x0, x0, 0 addi x0, x0, 0 addi x0, x0, 0 addi x0, x0, 0</pre>
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Lab3&4 Bonus

2024.10.21

4-way set associative

```
assign addr_element1 = {addr_index, 2'b00};  
assign addr_element2 = {addr_index, 2'b01};  
assign addr_element3 = {addr_index, 2'b10};  
assign addr_element4 = {addr_index, 2'b11};
```

```
assign addr_wordr = recent1==0?addr_word1  
:recent1==1?addr_word2  
:recent1==2?addr_word3  
:addr_word4;
```

```
assign recent1 = inner_recent[addr_element1];  
assign recent2 = inner_recent[addr_element2];  
assign recent3 = inner_recent[addr_element3];  
assign recent4 = inner_recent[addr_element4];
```

```
if(recent3==0) begin  
    inner_recent[addr_element3]<=recent4;  
end  
else if(recent2==0) begin  
    inner_recent[addr_element2]<=recent3;  
    inner_recent[addr_element3]<=recent4;  
end  
else if(recent1==0) begin  
    inner_recent[addr_element1]<=recent2;  
    inner_recent[addr_element2]<=recent3;  
    inner_recent[addr_element3]<=recent4;  
end  
inner_recent[addr_element4]<=0;
```