



Ve270 Introduction to Logic Design

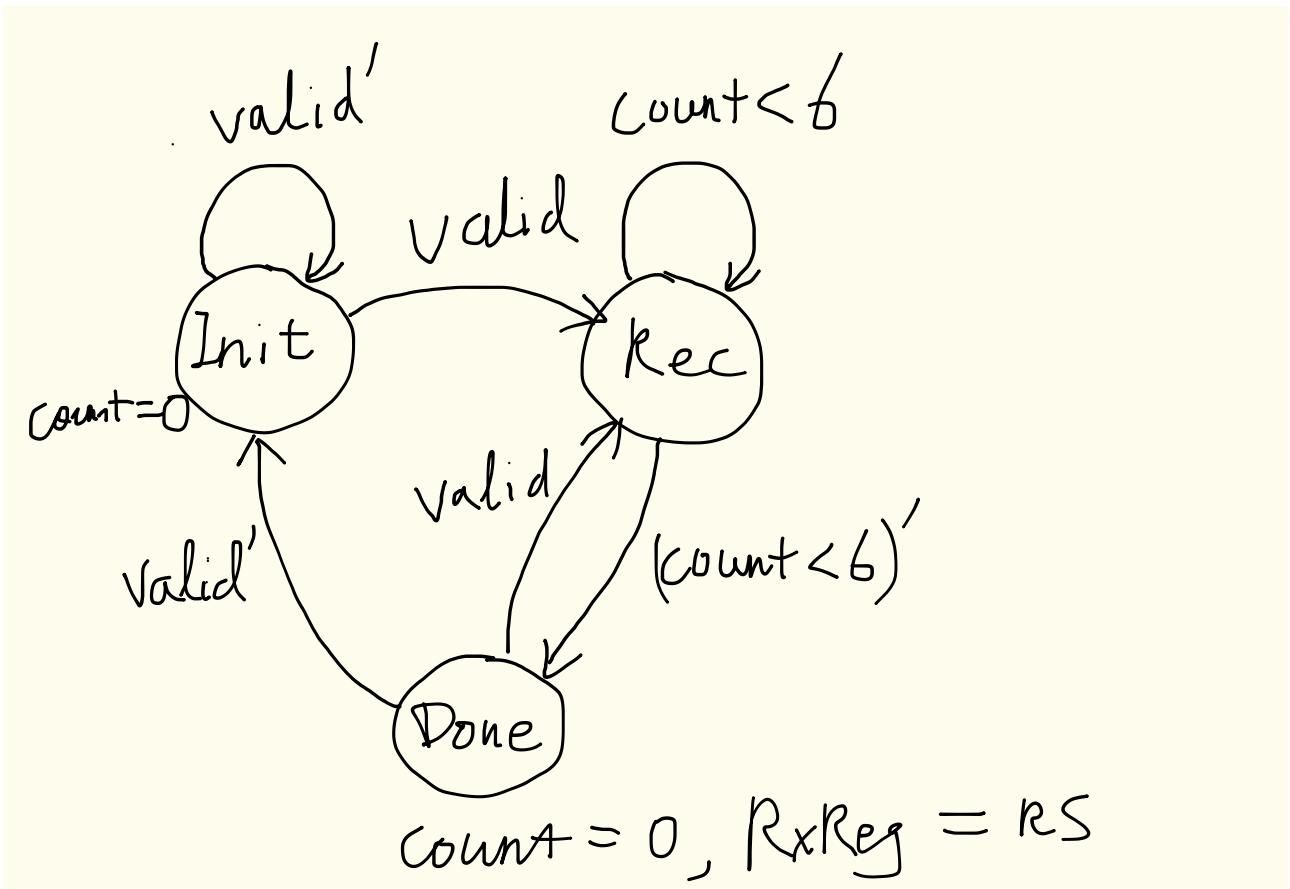
Homework 9

Assigned: November 21, 2019

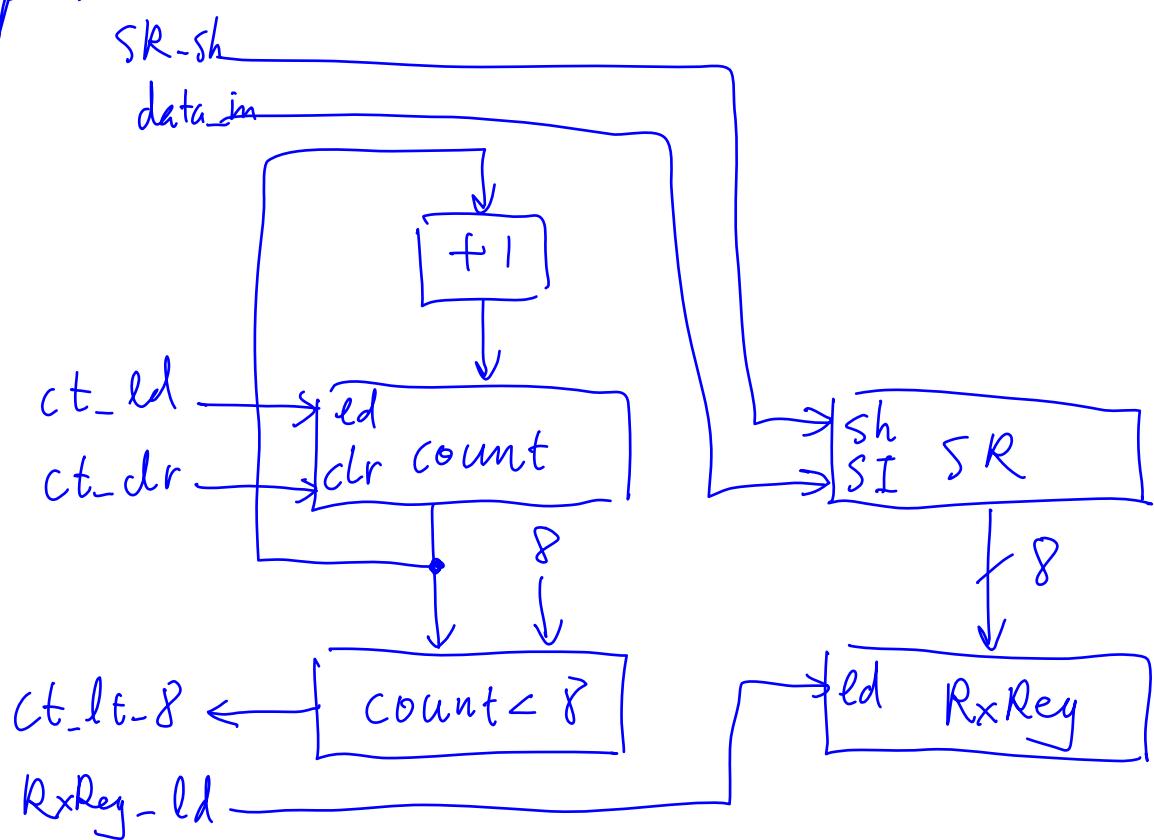
Due: November 28, 2019, 4:00pm.

The homework should be submitted in hard copies.

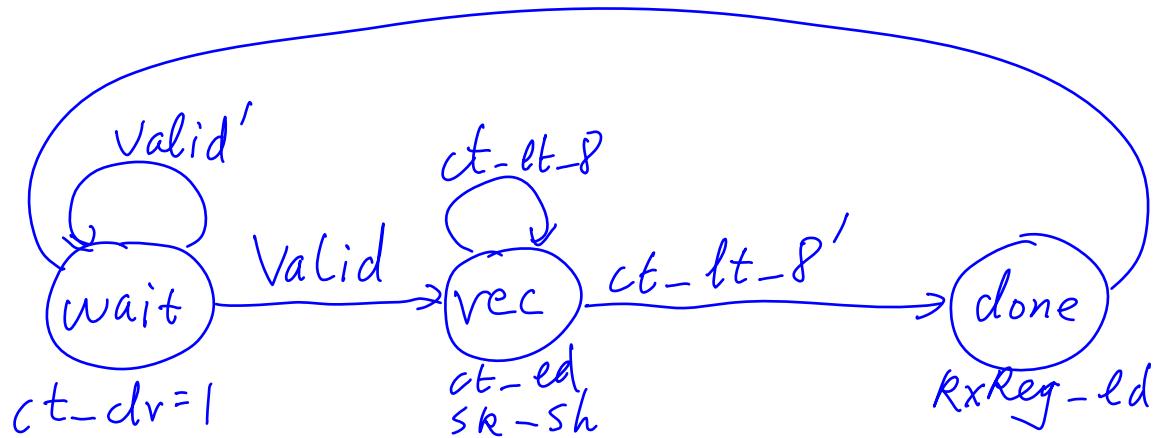
1. Design a circuit called **Receiver** that receives two single bit signals, **Valid** and **Data\_in**, from another device called **Transmitter**. The **Valid** signal sent from the **Transmitter** will be a 1-clock cycle pulse. After the **Receiver** receives the **Valid** pulse, it will start receiving 8 bits through port **Data\_in**, bit by bit. After the 8 bits of data is received, they should be copied into an 8-bit register called **RxReg**. (25 points)



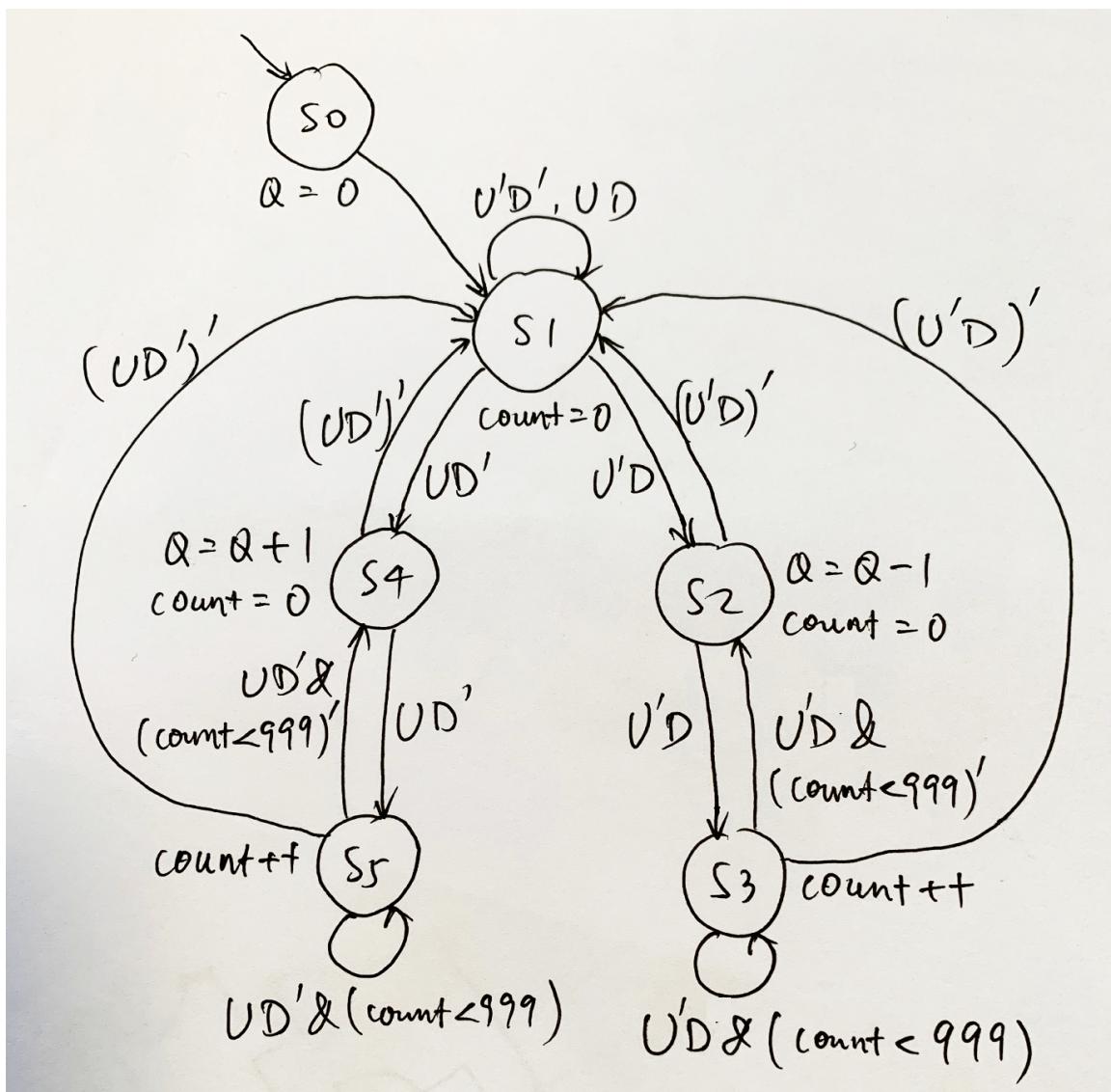
step2:



Step 3



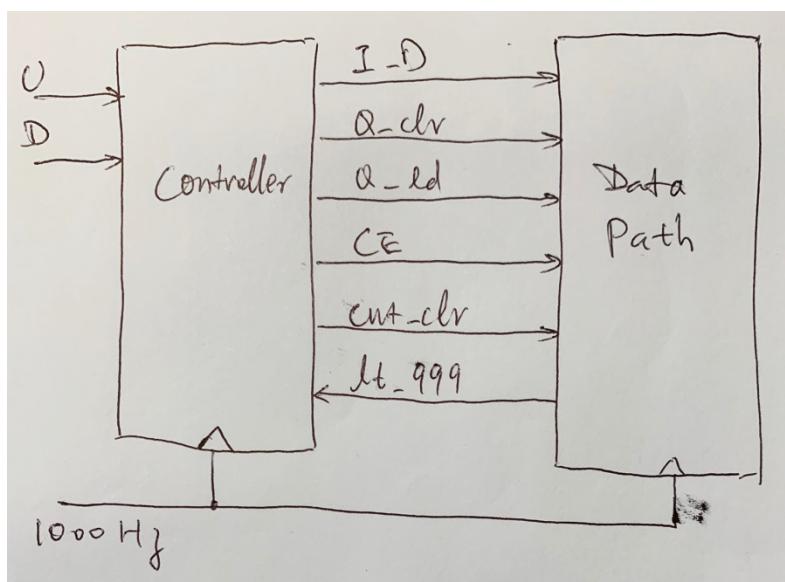
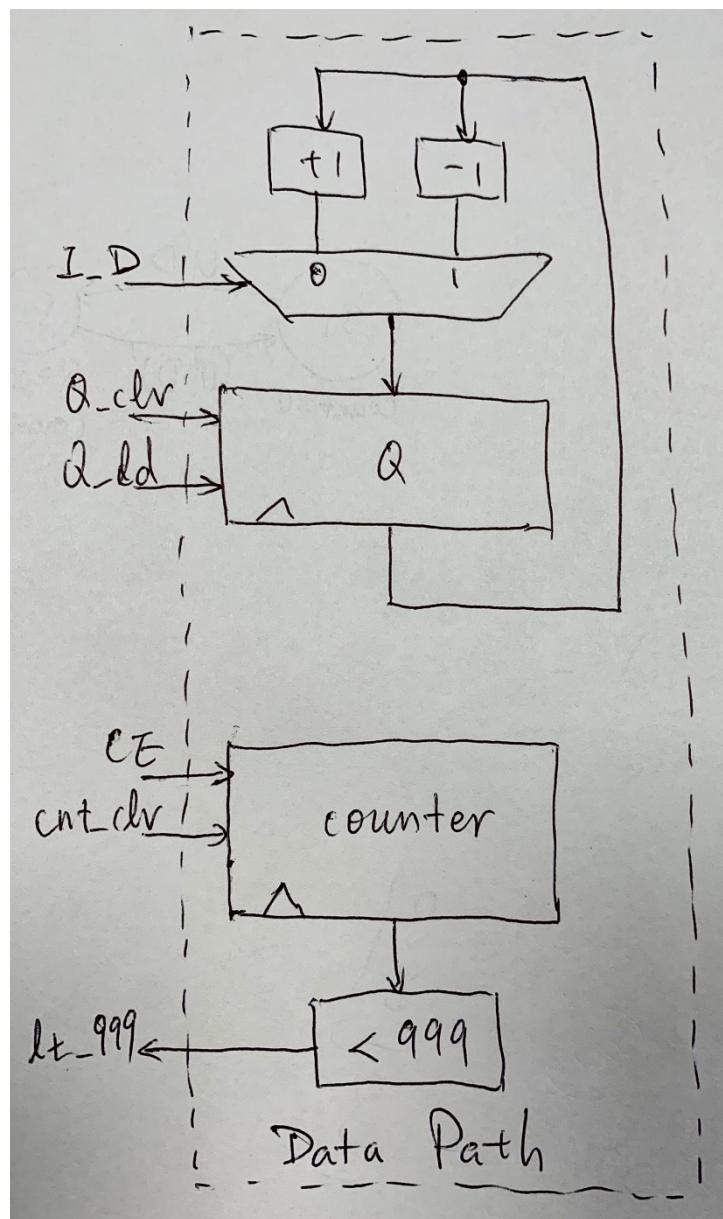
2. Problem 5.19 (25 points)

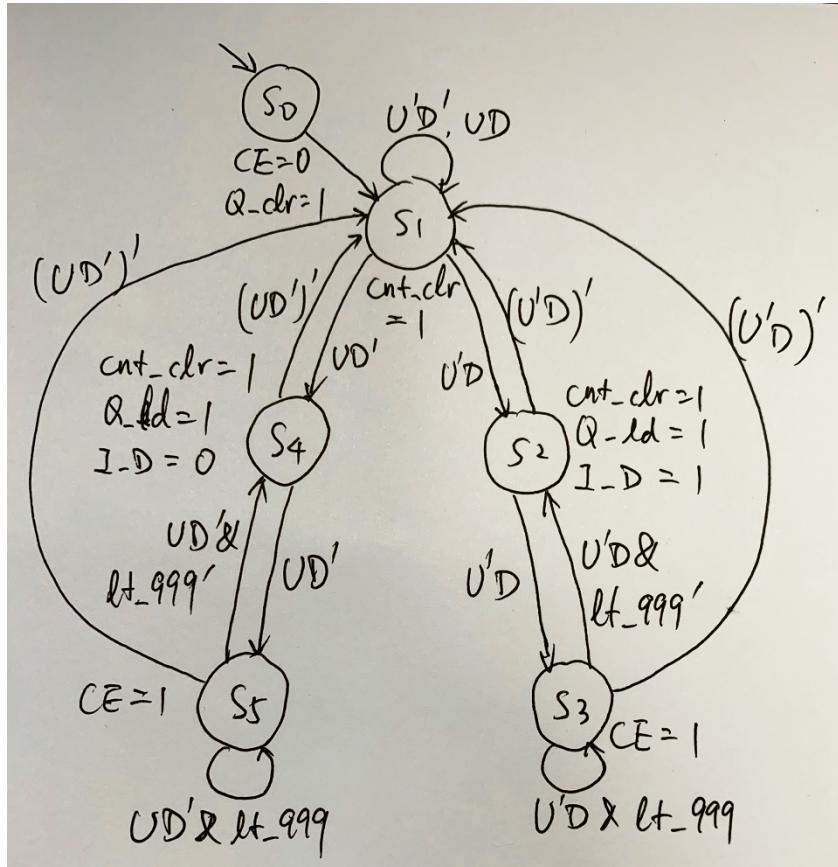




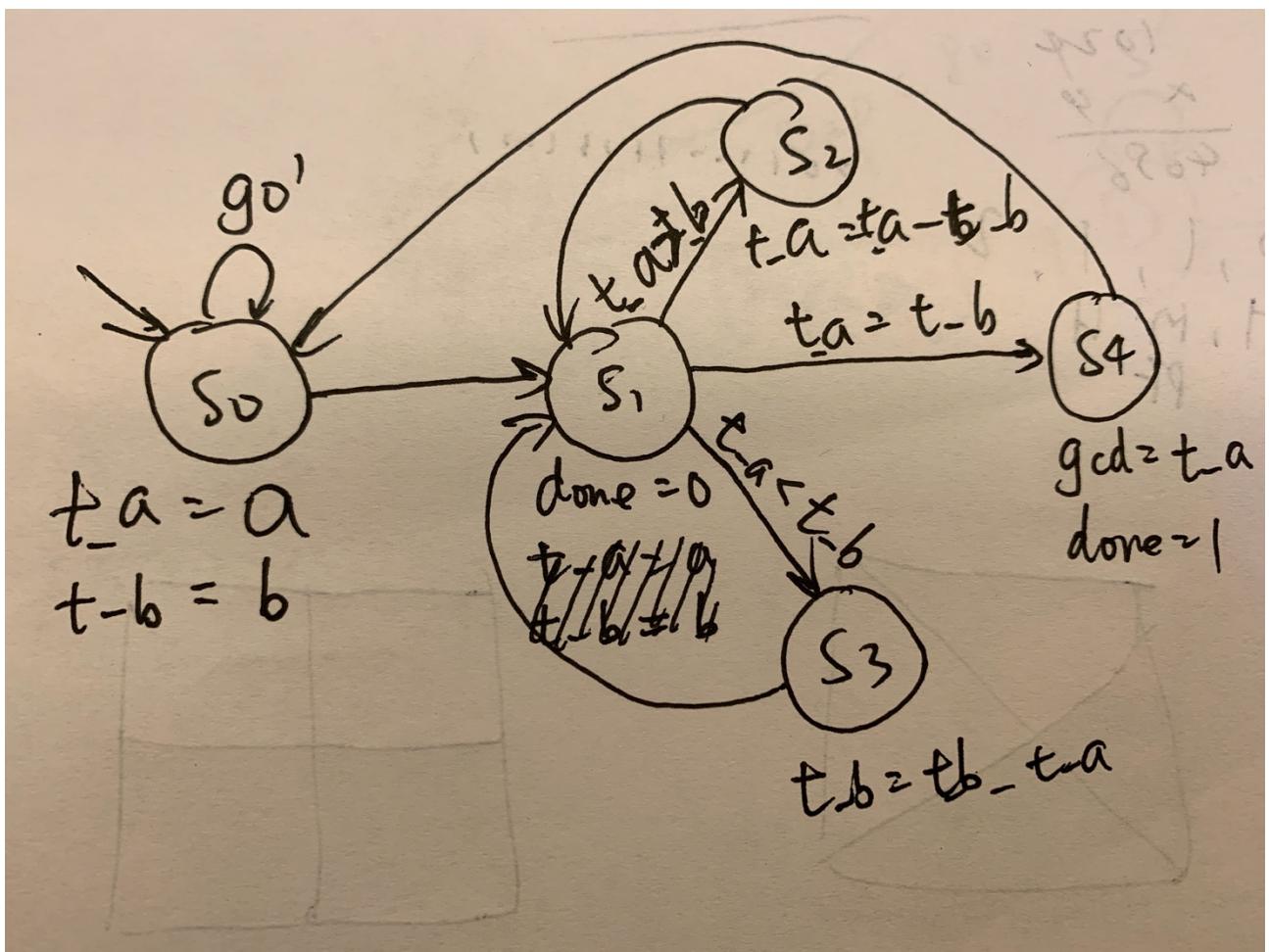
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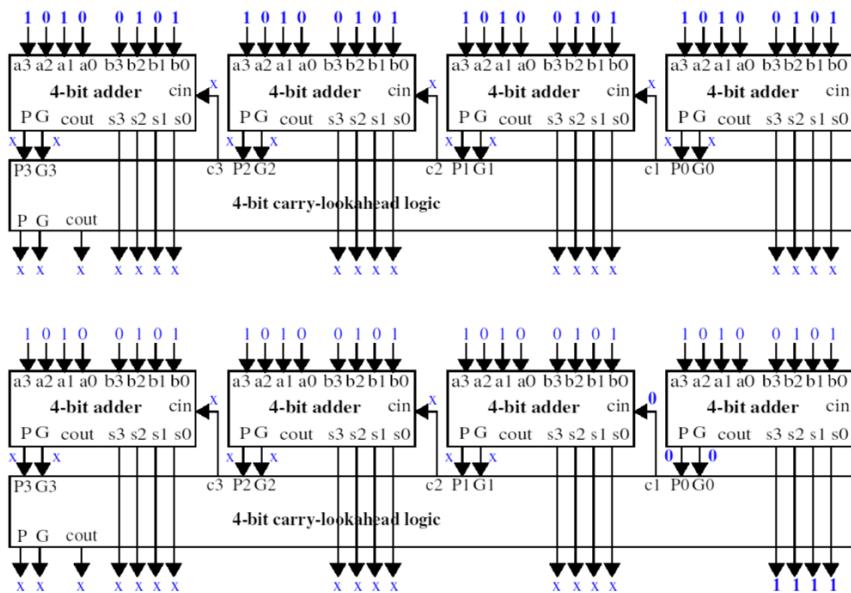


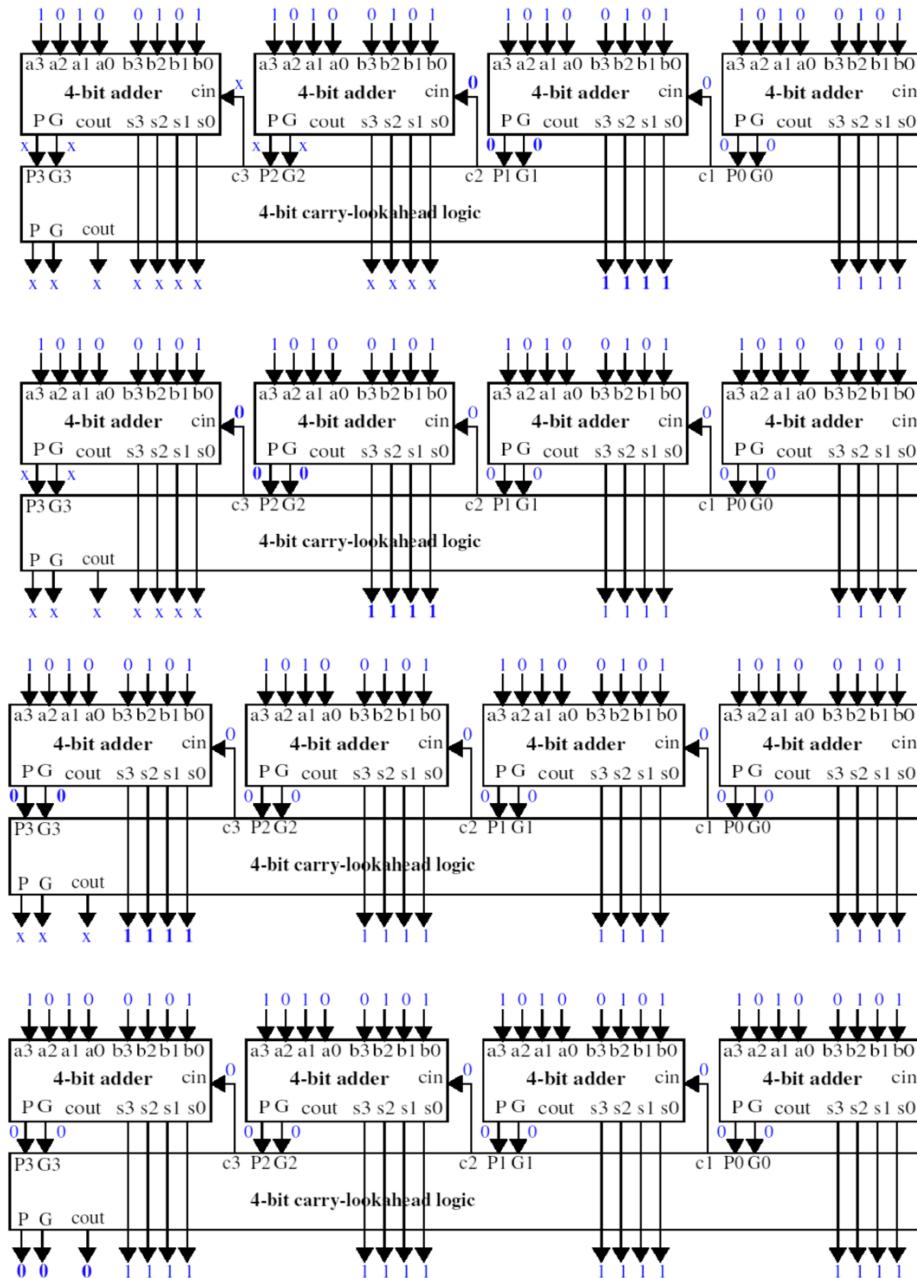
3. Problem 5.27 (15 points)



4. Problem 5.28 (15 points)

5. Problem 6.27 (10 points)



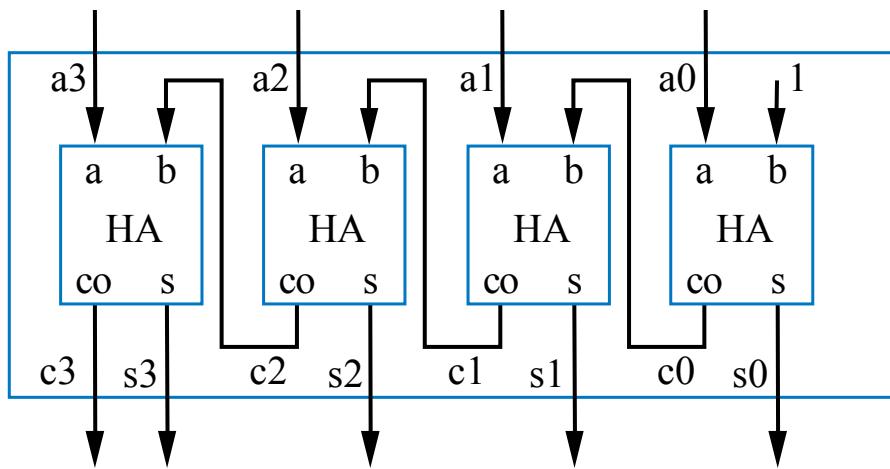


6. Following circuit is a carry-ripple style incrementor. Redesign the circuit as a carry-lookahead structure using the same Half Adders (HA). (10 points)



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$$C_0 = a_0$$

$$C_1 = a_1 a_0$$

$$C_2 = a_2 a_1 a_0$$

$$C_3 = a_3 a_2 a_1 a_0$$