JOINT INSTITUTE
交大密西根学院

## Ve270 Introduction to Logic Design

# Homework 10

**Assigned: November 28, 2019**

**Due: December 5, 2019, 4:00pm.**

**The homework should be submitted in hard copies.**

1. Problem 5.25 (20 points)

5.25 Assuming an inverter has a delay of 1 ns, and all other gates have a delay of 2 ns, determine the critical path for the 8-bit carry-ripple adder, assuming a design following Figure 4.31 and Figure 4.30, and: (a) assuming wires have no delay, (b) assuming wires have a delay of 1 ns.

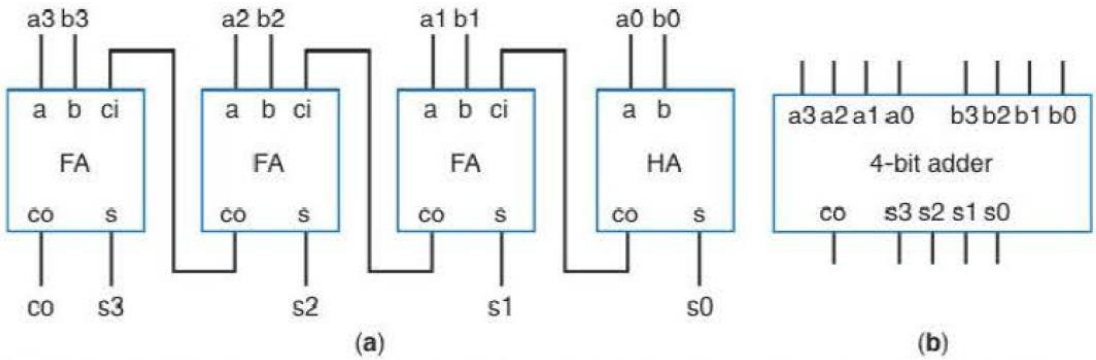



**Figure 4.31** 4-bit adder: (a) carry-ripple design with 3 full-adders and 1 half-adder, (b) block symbol.

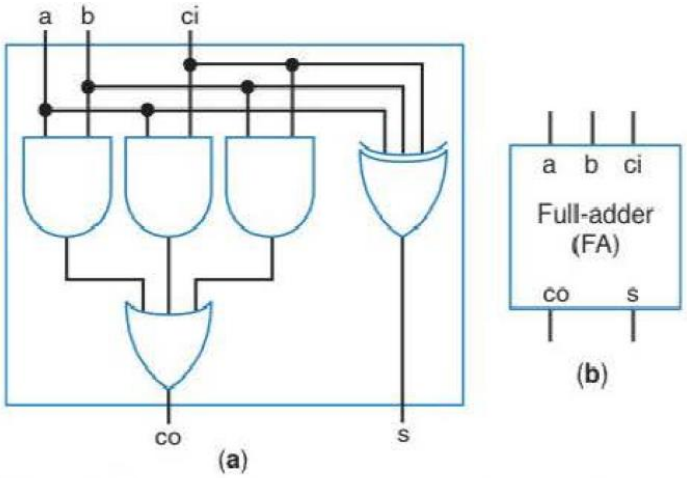
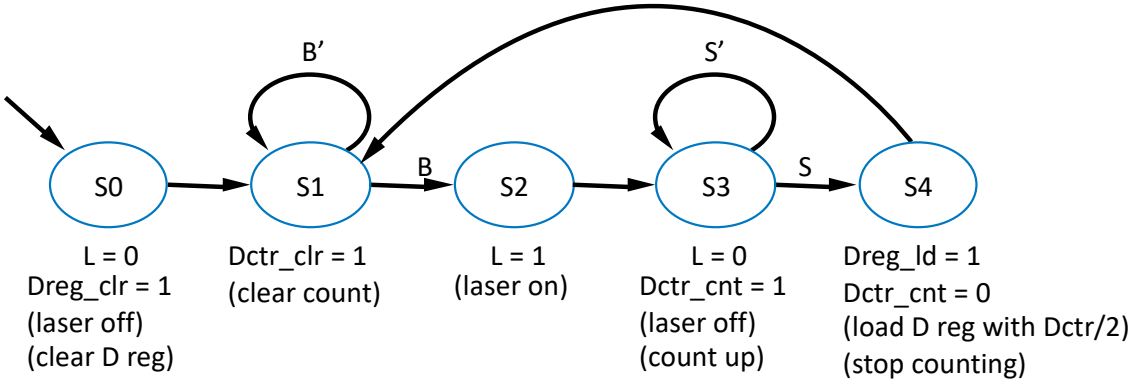



**Figure 4.30** Full-adder: (a) circuit, (b) block symbol.

2. Problem 5.26 (30 points)

5.26 (a) Convert the laser-based distance measurer's FSM in Figure 5.26 to a state register and logic. (b) Assuming all gates have a delay of 2 ns and the 16-bit up-counter has a delay of 5 ns, and wires have no delay, determine the critical path for the laser-based distance measurer. (c) Calculate the corresponding maximum clock frequency for the circuit.

Inputs: B, S  Outputs: L, Dreg_clr, Dreg_ld, Dctr_clr, Dctr_cnt

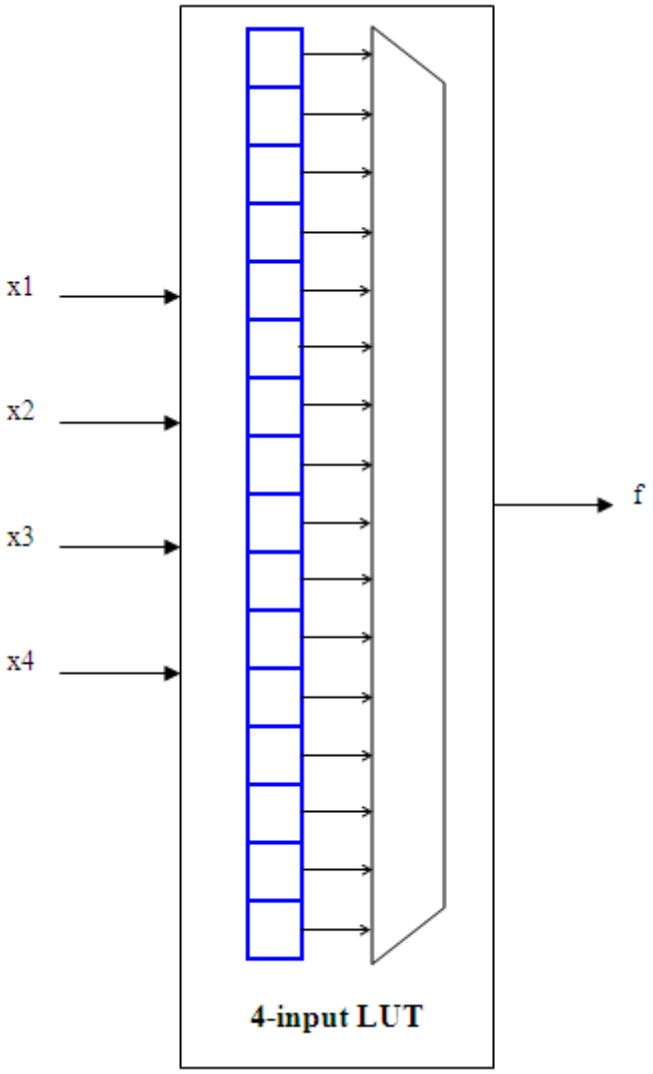



This is Figure 5.26

3. Given that an SRAM block has a 32-bit address input, each line of the memory has an address, how many lines does the memory have? (5 points)
   If each line is a 32-bit word, how many bytes (8 bits) does the memory have? (2 points)
   In that case, how many transistors does the memory have for storage? (3 points)
   If we use a decoder to decode the address, how big a decoder will be needed (e.g. a 3x8 decoder)? (2 points)
   If the memory is byte addressable, i.e. each byte has an address, how many bits does the memory have? (3 points)

4. Use one 4-input LUT to implement the following Boolean function (15 points)

   **f = x2x3'x4' + x1'x2x4 + x1'x2x3 + x1x2x3**




5. Problem 7.20 (20 points)

7.20 Show how to implement on two 3-input 2-output lookup tables the following function: `F(a, b, c, d) = a'bd + b'cd'`. Assume the two lookup tables are connected in the manner shown in Figure 7.47. You may not need to use every lookup table output.

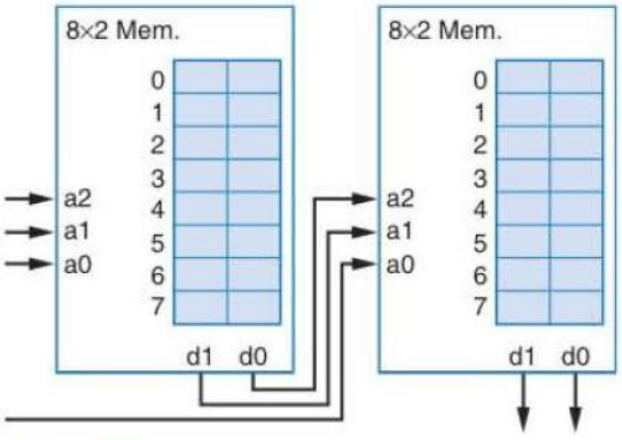



**Figure 7.47** Two 3-input 2-output lookup tables implemented using 8x2 memory.