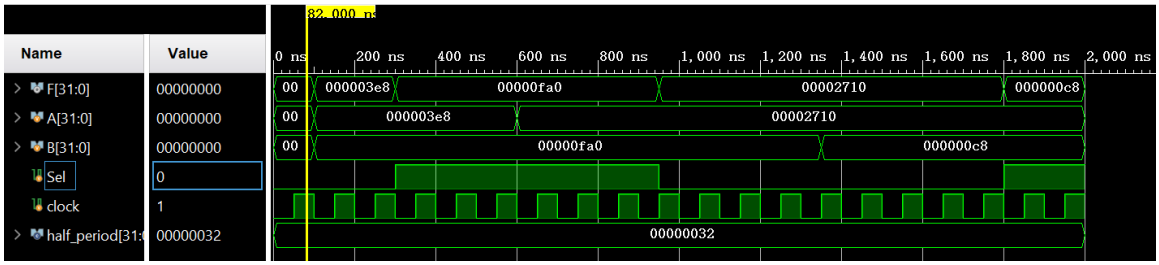
HW5 Report

Q1.

Verilog Code:

```
23      module Q1(F, A, B, Sel);
24          input [31:0] A, B;
25          input Sel;
26          output [31:0] F;
27          reg [31:0] F;
28
29          always @(A, B, Sel) begin
30              case (Sel)
31                  1'b0: F = A;
32                  1'b1: F = B;
33                  default F = 0;
34              endcase
35          end
36      endmodule
```

Simulation Result:



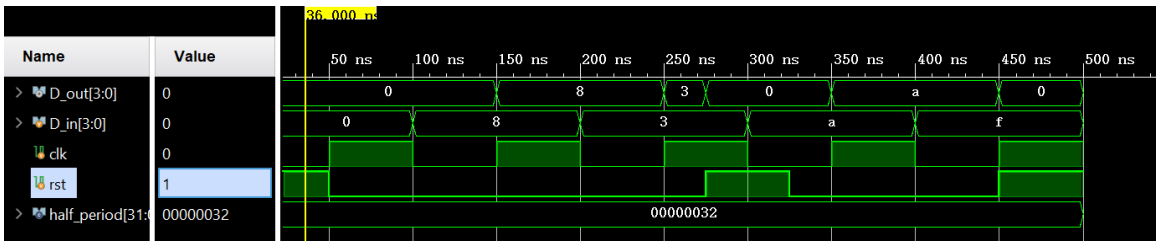
Q2.

Verilog Code:

```
1       module D_ff(Data_out, Data_in, clock, reset);
2           input Data_in, clock, reset;
3           output Data_out;
4           reg Data_out;
5
6           always @(posedge reset or posedge clock)
7           begin
8               if (reset == 1) Data_out <= 0;
9               else Data_out <= Data_in;
10          end
11      endmodule
```

```
13      module Q2(D_out, D_in, clk, rst);
14          input [3:0] D_in;
15          input clk, rst;
16          output [3:0] D_out;
17          // reg [3:0] D_out;
18
19          D_ff D0 (D_out[0], D_in[0], clk, rst);
20          D_ff D1 (D_out[1], D_in[1], clk, rst);
21          D_ff D2 (D_out[2], D_in[2], clk, rst);
22          D_ff D3 (D_out[3], D_in[3], clk, rst);
23
24      endmodule
```

Simulation Result:

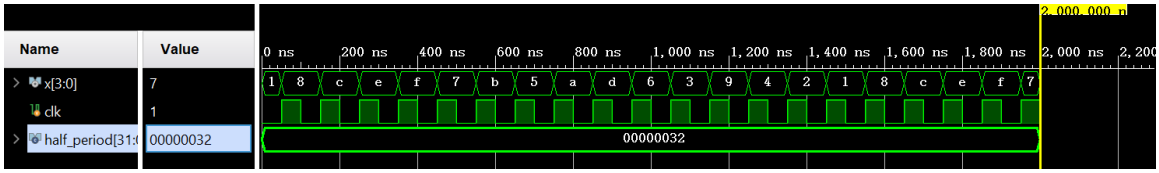


Q3.

Verilog Code:

```
1       module Q3(x, clk);
2           input clk;
3           output [3:0] x;
4           reg [3:0]x;
5           wire f;
6
7           xor(f, x[0], x[3]);
8
9           initial x = 4'b0001;
10
11          always @(posedge clk)
12          begin
13              x[3] <= f;
14              x[2] <= x[3];
15              x[1] <= x[2];
16              x[0] <= x[1];
17          end
18      endmodule
```

Simulation Result:



Q4.

Verilog Code:

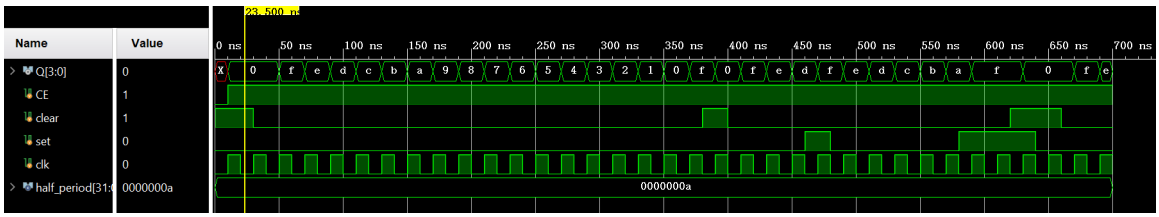
```
23      module MUX (Out, I0, I1, Sel);
24          input I0, I1, Sel;
25          output Out;
26          reg Out;
27
28          always @(I0, I1, Sel)
29          begin
30              case (Sel)
31                  1'b0: Out = I0;
32                  1'b1: Out = I1;
33                  default Out = 0;
34              endcase
35          end
36      endmodule

38      module DFF(Out, In, clk);
39          input In, clk;
40          output Out;
41          reg Out;
42
43          always @(posedge clk) Out <= In;
44
45      endmodule

47      module Q4(Q, CE, clear, set, clk);
48          input CE, clear, set, clk;
49          output [3:0] Q;
50          wire w0, w1, w2, w3, w4, w5, w6, w7, w8, w9, w10, w11, w12, w13, w14, w15;
51
52          assign w3 = Q[3]&(Q[0] | Q[1] | Q[2]) | (~Q[3])&(~Q[2])&(~Q[1])&(~Q[0]);
53          assign w2 = Q[2]&(Q[0] | Q[1]) | (~Q[2])&(~Q[1])&(~Q[0]);
54          assign w1 = Q[1]&Q[0] | (~Q[1])&(~Q[0]);
55          assign w0 = ~Q[0];
56
57          MUX M3(w7, Q[3], w3, CE);
58          MUX M2(w6, Q[2], w2, CE);
```

```
59          MUX M1(w5, Q[1], w1, CE);
60          MUX M0(w4, Q[0], w0, CE);
61
62          MUX M7(w11, w7, 1, set);
63          MUX M6(w10, w6, 1, set);
64          MUX M5(w9, w5, 1, set);
65          MUX M4(w8, w4, 1, set);
66
67          MUX M11(w15, w11, 0, clear);
68          MUX M10(w14, w10, 0, clear);
69          MUX M9(w13, w9, 0, clear);
70          MUX M8(w12, w8, 0, clear);
71
72          DFF D3(Q[3], w15, clk);
73          DFF D2(Q[2], w14, clk);
74          DFF D1(Q[1], w13, clk);
75          DFF D0(Q[0], w12, clk);
76
77      endmodule
```

Simulation Result:



Q5.

Verilog Code:

```
1   module Q5(Q, upper, CE, load, clk, rst);
2       input CE, load, clk, rst; //load = 4'b0011;
3       output upper;
4       output [3:0] Q;
5       reg upper;
6
7       wire w0, w1, w2, w3, w4, w5, w6, w7, w8, w9, w10, w11, w12, w13, w14,
8            w15, w16, w17, w18, w19;
9
10      assign w3 = Q[3]&(~(Q[2]&Q[1]&Q[0])) | (~Q[3])&(Q[2]&Q[1]&Q[0]);
11      assign w2 = Q[2]&(~(Q[1]&Q[0])) | (~Q[2])&(Q[1]&Q[0]);
12      assign w1 = Q[1]&(~Q[0]) | (~Q[1])&Q[0];
13      assign w0 = ~Q[0];
```

```
15          MUX M3(w7, Q[3], w3, CE);
16          MUX M2(w6, Q[2], w2, CE);
17          MUX M1(w5, Q[1], w1, CE);
18          MUX M0(w4, Q[0], w0, CE);
19
20          MUX M7(w11, w7, 0, load);
21          MUX M6(w10, w6, 1, load);
22          MUX M5(w9, w5, 1, load);
23          MUX M4(w8, w4, 0, load);
24
25          MUX M11(w15, w11, 0, rst);
26          MUX M10(w14, w10, 0, rst);
27          MUX M9(w13, w9, 0, rst);
28          MUX M8(w12, w8, 0, rst);
29
30          DFF D3(Q[3], w15, clk);
31          DFF D2(Q[2], w14, clk);
32          DFF D1(Q[1], w13, clk);
33          DFF D0(Q[0], w12, clk);

35          always @(Q)
36          begin
37              if (Q[3] == 1) upper = 1;
38              else upper = 0;
39          end
40
41      endmodule
```

Simulation Result: