Q6.

Verilog Code:

```
23  module MUX(Q, I0, I1, I2, I3, S0, S1);
24      output Q;
25      input I0, I1, I2, I3, S0, S1;
26      reg Q;
27
28      always @(I0, I1, I2, I3, S0, S1)
29      begin
30          case ({S1, S0})
31              2'b00: Q = I0;
32              2'b01: Q = I1;
33              2'b10: Q = I2;
34              2'b11: Q = I3;
35              default Q = 0;
36          endcase
37      end
38  endmodule
40  module Dff(Q, D, clk);
41      output Q;
42      input D, clk;
43      reg Q;
44
45      always @(negedge clk)
46      begin
47          Q <= D;
48      end
49  endmodule
51  module ex6(Q, D, SI, Sh, L, clk);
52      output [3:0] Q;
53      input [3:0] D;
54      input SI, Sh, L, clk;
55
56      wire w0, w1, w2, w3;
57
58      MUX M3(w3, Q[3], D[3], SI, SI, L, Sh);
59      MUX M2(w2, Q[2], D[2], Q[3], Q[3], L, Sh);
60      MUX M1(w1, Q[1], D[1], Q[2], Q[2], L, Sh);
61      MUX M0(w0, Q[0], D[0], Q[1], Q[1], L, Sh);
62
63      Dff D3(Q[3], w3, clk);
64      Dff D2(Q[2], w2, clk);
65      Dff D1(Q[1], w1, clk);
66      Dff D0(Q[0], w0, clk);
67
68  endmodule
```

Simulation Result: