



# CH32V203 Data Sheet

V2.5

## overview

The CH32V series is an industrial-grade general-purpose microcontroller based on the highland barley 32-bit RISC-V design. The whole series of products join the hardware stack area, fast Compared with the standard, the interrupt response speed is greatly improved. CH32V203 is a tool designed based on 32-bit RISC-V core Industry-level enhanced low-power general-purpose microcontroller, high performance, supports 144MHz main frequency zero-wait operation in terms of product functions, equipped with V4B core, Work and sleep power consumption dropped significantly year-on-year. The CH32V203 series integrates dual USB interfaces and supports USB Host and USB Device Device function, with 1 channel CAN interface (2.0B active), dual OPA operational amplifier, 4 groups of USART, dual I<sub>2</sub>C, 12-bit ADC, 10 channels Rich peripheral resources such as Touchkey.

## Product Features

### I Kernel Core:

- Highland barley 32-bit RISC-V core, a variety of instruction set combinations
- Fast programmable interrupt controller + hardware interrupt stack
- Branch prediction, conflict handling mechanism
- Single cycle multiplication, hardware division
- The main frequency of the

system is 144MHz

- Memory:** - It can be equipped with a maximum 64KB volatile data storage area SRAM - It can be equipped with a 224KB program storage area CodeFlash (zero waiting application area + non-zero waiting data area)
- 28KB system boot memory area BootLoader
  - 128B system non-volatile configuration information storage area
  - 128B user-defined information storage area

### I Power management and low power consumption:

- System power supply VDD rating: 3.3V
  - GPIO unit independent power supply VIO rating: 3.3V -
- Low power consumption mode:** sleep, stop, standby
- VBAT supply independently powers RTC and backup registers

### I System clock, reset

- Embedded factory tuned 8MHz RC oscillator
  - Embedded 40KHz RC oscillator
  - Embedded PLL, optional CPU clock up to 144MHz -
- External support** 3 ~ 25MHz high-speed oscillator
- External support 32.768KHz low-speed oscillator
  - Power On/Off Reset, Programmable Voltage Monitor
- I Real-time clock RTC:** 32-bit independent timer | 1 group of 8 general-purpose DMA controllers - 8 channels, support ring buffer management

### - Support TIMx/ADC/USART/I<sub>2</sub>C/SPI | 2 sets of

operational amplifiers and comparators: connect ADC and TIMx

### | 2 sets of 12-bit analog-to-digital conversion ADC

-Analog input range: VSSA~VDDA - 16

external signal channels + 2 internal signal channels

- On-chip temperature sensor

- Dual ADC conversion mode

### | 16-way TouchKey channel detection |

### Multiple timers

- 1 16-bit advanced timer with added dead-band control and emergency Brake, provides PWM complementary output for motor control
- Three 16-bit general-purpose timers with input capture/output ratio Comparing/PWM/pulse counting and incremental encoder input
- 1 32-bit general-purpose timer (for CH32V203RBx)
- 2 watchdog timers (independent and windowed)
- System time base timer: 64-bit counter

### | Multiple communication interfaces:

- 4 USART ports
- 2 I<sub>2</sub>C interfaces (support SMBus/PMBus)
- 2 SPI interfaces
- USB2.0 full speed device interface (full speed and low speed)
- USB2.0 full speed host/device interface
- 1 set of CAN interface (2.0B active)

### | Fast GPIO port - 37 I/O ports,

mirroring 16 external interrupts

### | Security features: CRC calculation unit, 96-bit chip unique ID | Debug

mode: serial 2-wire debug interface | Package types:

LQFP, QFN, TSSOP and QSOP

## Chapter 1 Series Product Description

CH32V series products are industrial-grade general-purpose enhanced MCUs based on 32-bit RISC-V instruction set and architecture design. its products according to function Resources are divided into categories such as General, Connectivity, Wireless, etc. Among them are package type, peripheral resources and quantity, pin number, device characteristics The differences between high and low extend each other, but they remain compatible with each other in terms of software, functions, and hardware pin configurations, which provides users with better solutions in product development. Product iteration and rapid application provide freedom and convenience.

Please refer to the data sheet for the device characteristics of this series of products.

Please refer to "CH32FV2x\_V3xRM" for detailed information about the function description, usage method and register configuration of each peripheral of the product.

Both the data sheet and the reference manual can be downloaded from [Qinheng's official](#)

website: [www.wch.cn](http://www.wch.cn) For information about the RISC-V instruction set and architecture, you can download it from the "<http://riscv.org>" website.

This manual is the data manual of CH32V203 series products. For V303\_305\_307 series, please refer to "CH32V307DS0", for V208 series, please refer to Refer to "CH32V208DS0".

Table 1-1 Overview of series products

Small and medium capacity universal type		Large capacity universal type (V303)		Connected type (V305)	Interconnected type (V307)	Wireless type (V208)
(V203) Highland barley V4B		Highland barley V4F				Highland barley V4C
32K Flash	64K Flash	128K Flash	256K Flash	128K Flash		
10K SRAM	20K FOR SHAME	32K RAM	64K SRAM	32K RAM	64K SRAM	64K SRAM
2*ADC(TKey)	2*ADC(TKey)	2*ADC(TKey)	2*ADC(TKey) 2*DAC 4*ADTM 4*GPTM	2*ADC(TKey) 2*DAC 4*ADTM 4*GPTM	2*ADC(TKey) 2*DAC 4*ADTM 4*GPTM	2*ADC(TKey) 2*DAC 4*ADTM 4*GPTM
ADTM	ADTM	2*DAC	4*ADTM 4*GPTM	4*ADTM 4*GPTM	2*BCTM 8*USART/UART	ADTM 3*GPTM
2*GPTM	3*GPTM	ADTM	2*BCTM 8*USART/UART	2*BCTM 5*USART/UART	3*SPI(2*I2S)	GPTM(32)
2*USART	4*USART	3*GPTM	3*SPI(2*I2S)	3*SPI(2*I2S)	2*I2C	4*USART/UART
SPI	2*SPI	3USART	2*I2C USBFS	2*I2C OTG_FS	OTG_FS	2*SPI
2C	2*I2C	2*SPI	USBFS	2*I2C	USBHS(+PHY)	2*I2C
USBD	USBD	2*I2C	CAN	OTG_FS	2*CAN	USBD
USBFS	USBFS	USBFS	RTC	USBHS(+PHY)	RTC	USBFS
CAN	CAN	CAN	2*WDG	2*CAN	2*WDG	CAN
RTC	RTC	RTC	4*OPA	RTC	4*OPA	RTC
2*WDG	2*WDG	2*WDG	RNG	2*WDG	RNG	2*WDG
2*OPA	2*OPA	4*OPA	SDIO FSMC	4*OPA RNG SDIO	SDIO FSMC PAD	2*OPA ETH-10M(+PHY) BLE5.3

Note: The quantity or function of certain peripherals of the same type of product may be limited by the package, please confirm the product package when selecting.

### abbreviation

**ADTM:** Advanced Timer

**TKey:** touch key

**USBFS:** Full Speed Host/Device Controller

**GPTM:** General Purpose Timer

**OPA:** operational amplifier, comparator

**USBHS:** High Speed Host/Device Controller

**GPTM(32):** 32-bit general-purpose timer

**RNG:** Random Number Generator

**BCTM:** Basic Timer

**USBD:** Full Speed Device Controller

Table 1-2 Kernel comparison overview

kernel features	Instruction Set	hardware the stack series	to interrupt nesting series	fast to interrupt Number of channels	integer division cycle	vector table model	expand instruction	Memory Protect
V4B	IMAC	2	2	4	9 Address or command support None			
V4C	IMAC	2	2	4	5 Address or instruction support standard			
V4F	IMAFC	3	8	4	5 Address or instruction support standard			

Note: For related information about the kernel, please refer to the QingKeV4 microprocessor manual "QingKeV4\_Processor\_Manual".

## Chapter 2 Specification Information

CH32V203 series is a 32-bit RISC core MCU designed based on RISC-V instruction architecture, with a working frequency of 144MHz and built-in high-speed memory

In the system structure, multiple buses work synchronously, providing a wealth of peripheral functions and enhanced I/O ports. This series of products has built-in 2 12

Bit ADC module, multi-group timer, multi-channel touch key capacitance detection (TKey) and other functions, also includes standard and dedicated communication interfaces:

I2C, SPI, USART, CAN controller, USB2.0 full-speed host/device controller, USB2.0 full-speed device controller, etc.

The rated working voltage of the product is 3.3V, and the working temperature range is -40°C~85°C industrial grade. Support a variety of power-saving working modes to meet the needs of production

product low power application requirements. Each model in the series of products differs in terms of resource allocation, number of peripherals, peripheral functions, etc. You can choose according to your needs.

## 2.1 Model comparison

Table 2-1 Resource allocation of CH32V small and medium-capacity general-purpose products

Product number resource difference		CH32V203								
		F6	F8	G6	G8	K6	K8	C6	C8	RB
Chip Pin Count Flash		20	20	28	28	32	32	48	48	64
(bytes)	(1)	32K	64K	32K	64K	32K	64K	32K	64K 128K(2)	
SRAM (bytes)		10K	20K	10K	20K	10K	20K	10K	20K	64K
Number of GPIO ports		16	17	24	24	26	26	37	37	51
Certainty	Advanced (16-bit)	1 (3)	1 (3)	1 (3)	1 (3)	1	1	1	1	1
	Universal (16-bit) Universal	2 (3)	3 (3)	2 (3)	3 (3)	2	3	2	3	3
hour	(32-bit)									1
	Watchdog	2 (WWDG + IWDG) support								
device	System Time Base (64-bit)									
	RTC	support								
ADC/TKey (number of channels@unit) 9@2 op amp		comparator	9@2	10@2 10@2 10@2			10@2 10@2 10@2 16@1			
		1	2	2	2	2	2	2	2	2
Pass	USART/UART	1	2	2	2	2	2	2	4	4
	SPI	1	1	1	1	1	1	1	2	2
letter	2C	0	1	1	1	1	1	1	2	2
	CAN	1	-	1	1	1	1	1	1	1
catch	USB	1	-	1	1	1	1	1	1	1
	(FS)	-	1	-	1	-	-	1	1	1
mouth	USBHD	-	-	-	-	-	-	-	-	-
	Ethernet									10M
CPU main		Max 144MHz								
frequency rated		3.3V								
voltage operating temperature		Industrial grade: -40°C~85°C								
Package form		TSSOP20/QFN20 QFN28 QSOP28				LQFP32	LQFP48	LQFP QFN48	LQFP64M	

Note: 1. The flash memory byte represents the zero wait operation area ROWAIT, and the non-zero wait area for the model is V203 224K- ROWAIT

The product supports user-selected word configuration as (128K FLASH+64K SRAM), (144K FLASH+48K 2.128K FLASH+64K SRAM

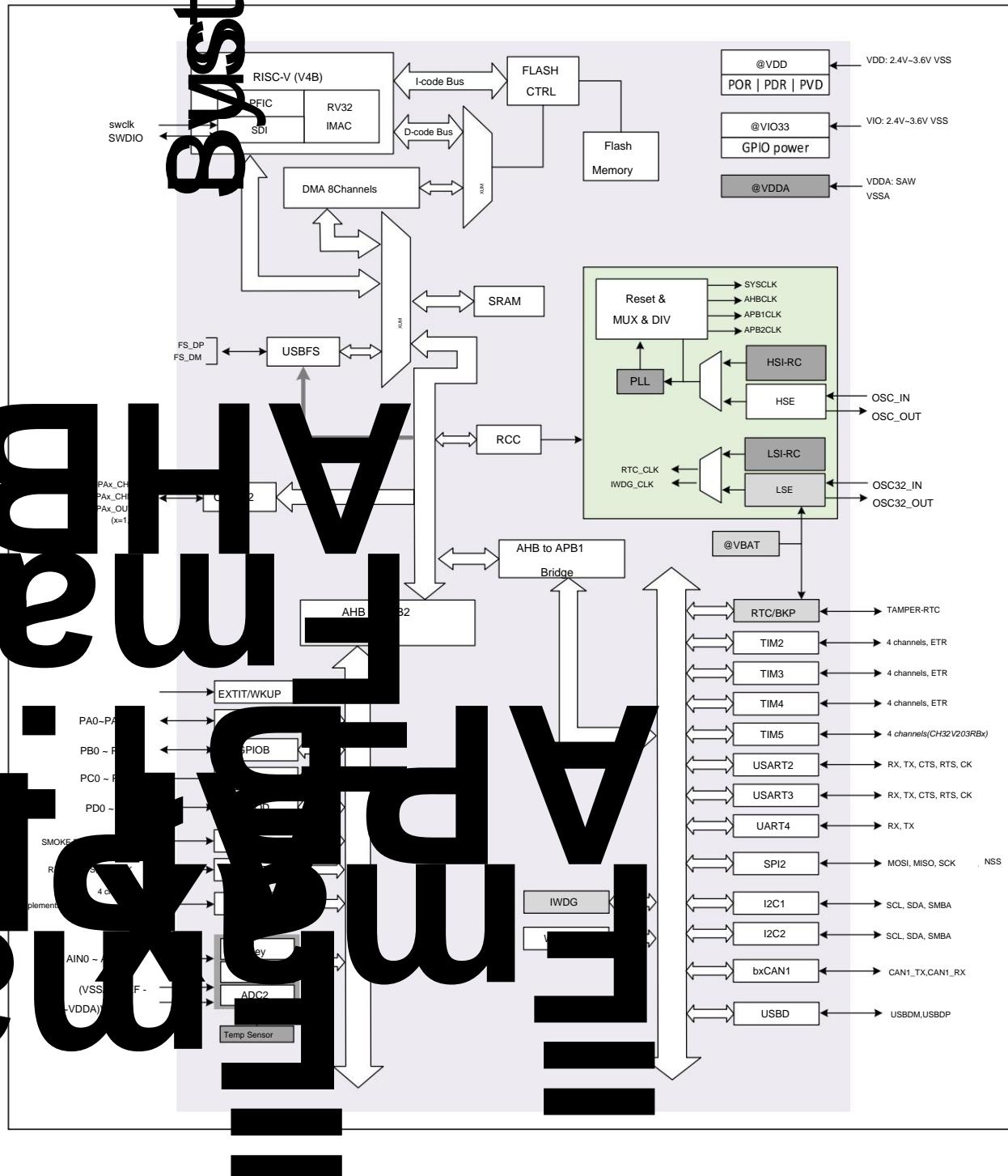
SRAM), (160K FLASH+32K SRAM) one of several combinations.

3. Functions involving pin signals such as PWM and capture in the timer need to be combined with the pins of the actual chip package. If some packaged chips do not have leads, such functions cannot be used.

## 2.2 System Architecture

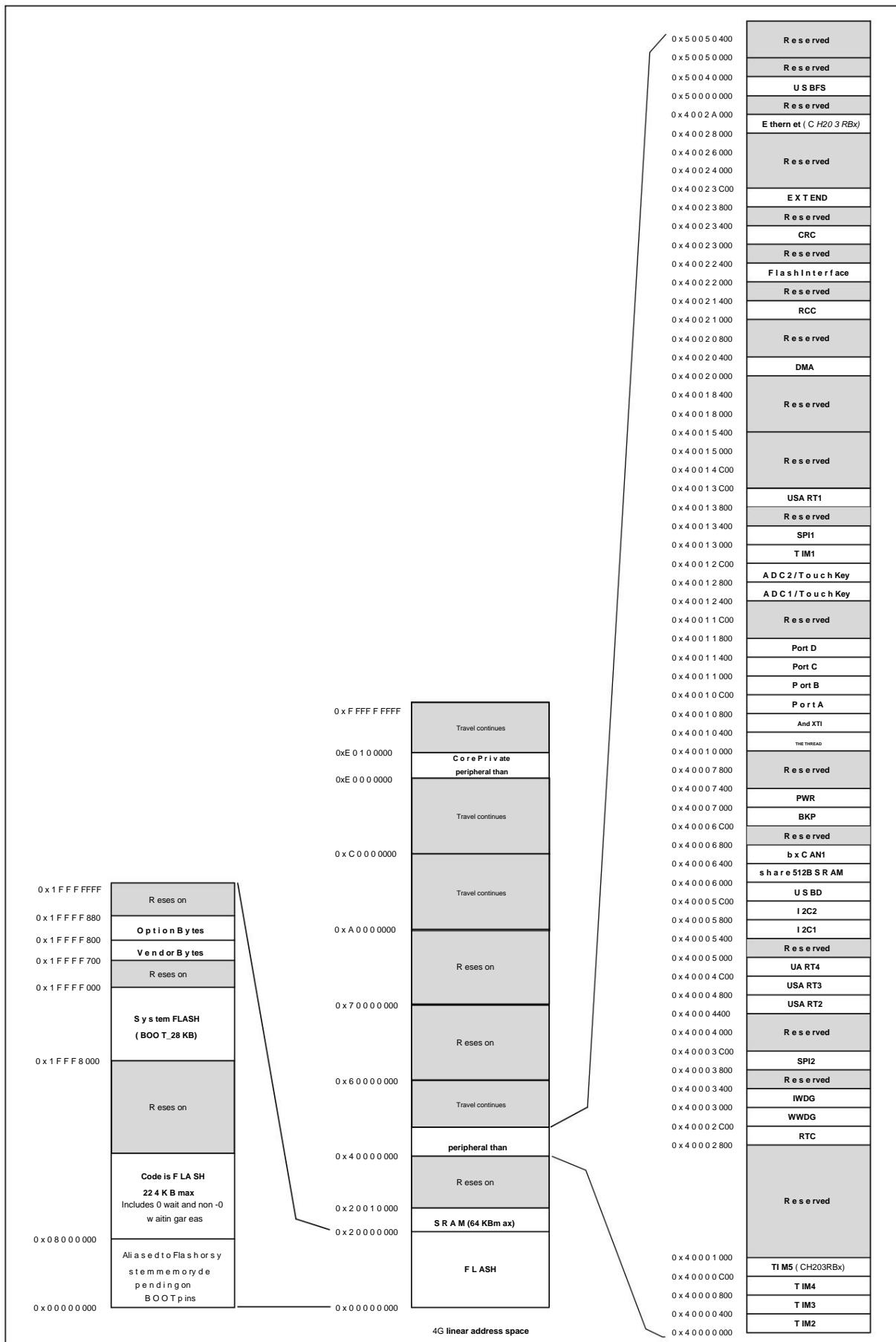
Microcontroller is designed based on RISC-V instruction set, and in its architecture, core, arbitration unit, DMA module, SRAM storage and other parts realize interaction through multiple groups of buses. The design integrates a general-purpose DMA controller to reduce the burden on the CPU and improve access efficiency. The multi-level clock management mechanism is used to reduce the operating power consumption of peripherals. At the same time, data protection mechanisms and clock automatic switching protection measures increase system stability. The figure below is a block diagram of the overall internal architecture of the series products.

Figure 2-1 System block diagram



## 2.3 Memory Map Table

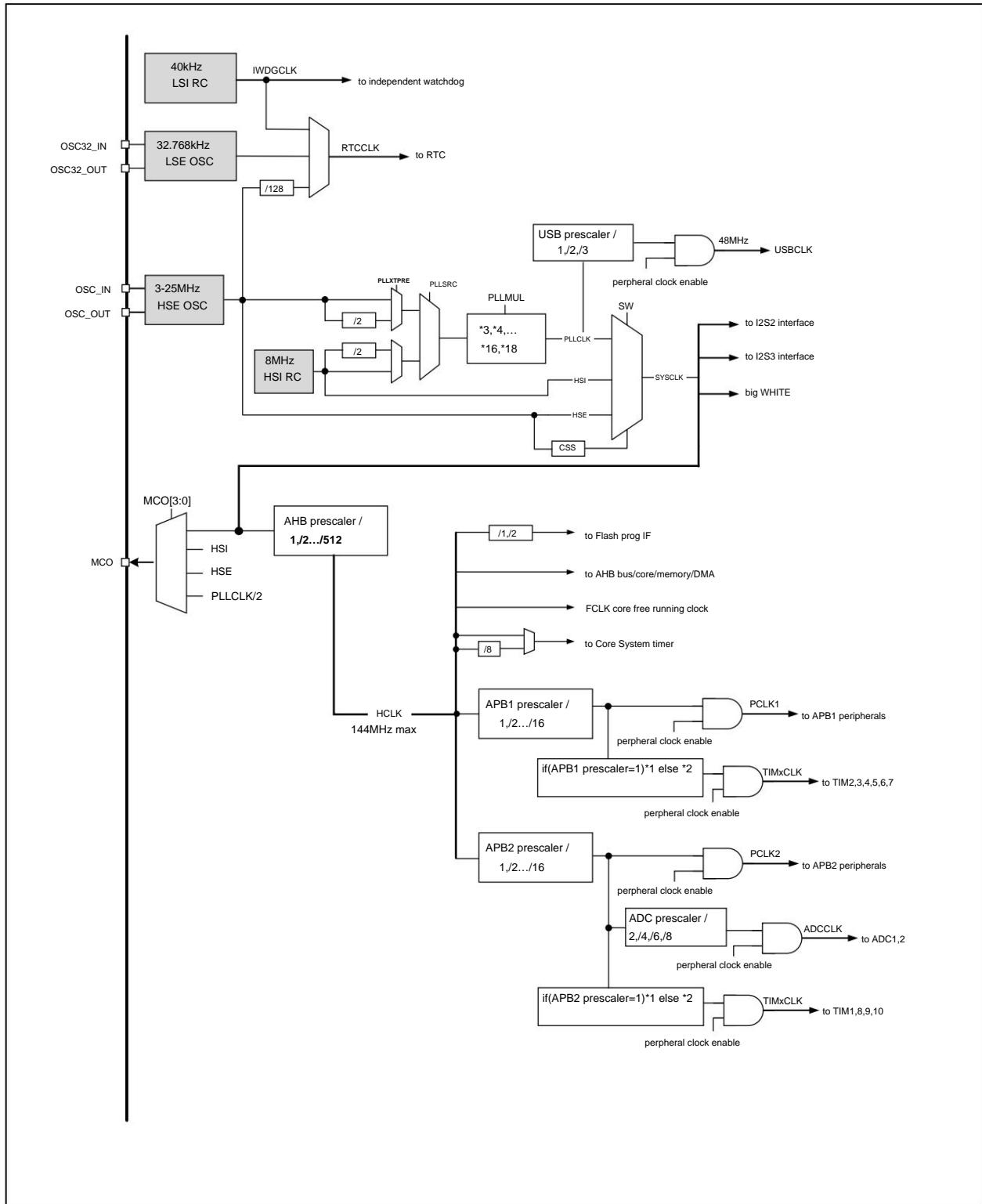
Figure 2-2 Memory address mapping



## 2.4 Clock tree

Four groups of clock sources are introduced into the system: internal high-frequency RC oscillator (HSI), internal low-frequency RC oscillator (LSI), external high-frequency oscillator (HSE), external low-frequency oscillator (LSE). Among them, the low-frequency clock source provides the clock reference for RTC and independent watchdog. The high-frequency clock source is directly or indirectly multiplied by the PLL and then output as the system bus clock (SYSCLK). The system clock is then provided by each prescaler to provide the AHB domain, APB1 domain, APB2 domain peripheral control clock and sampling or interface output clock. Part

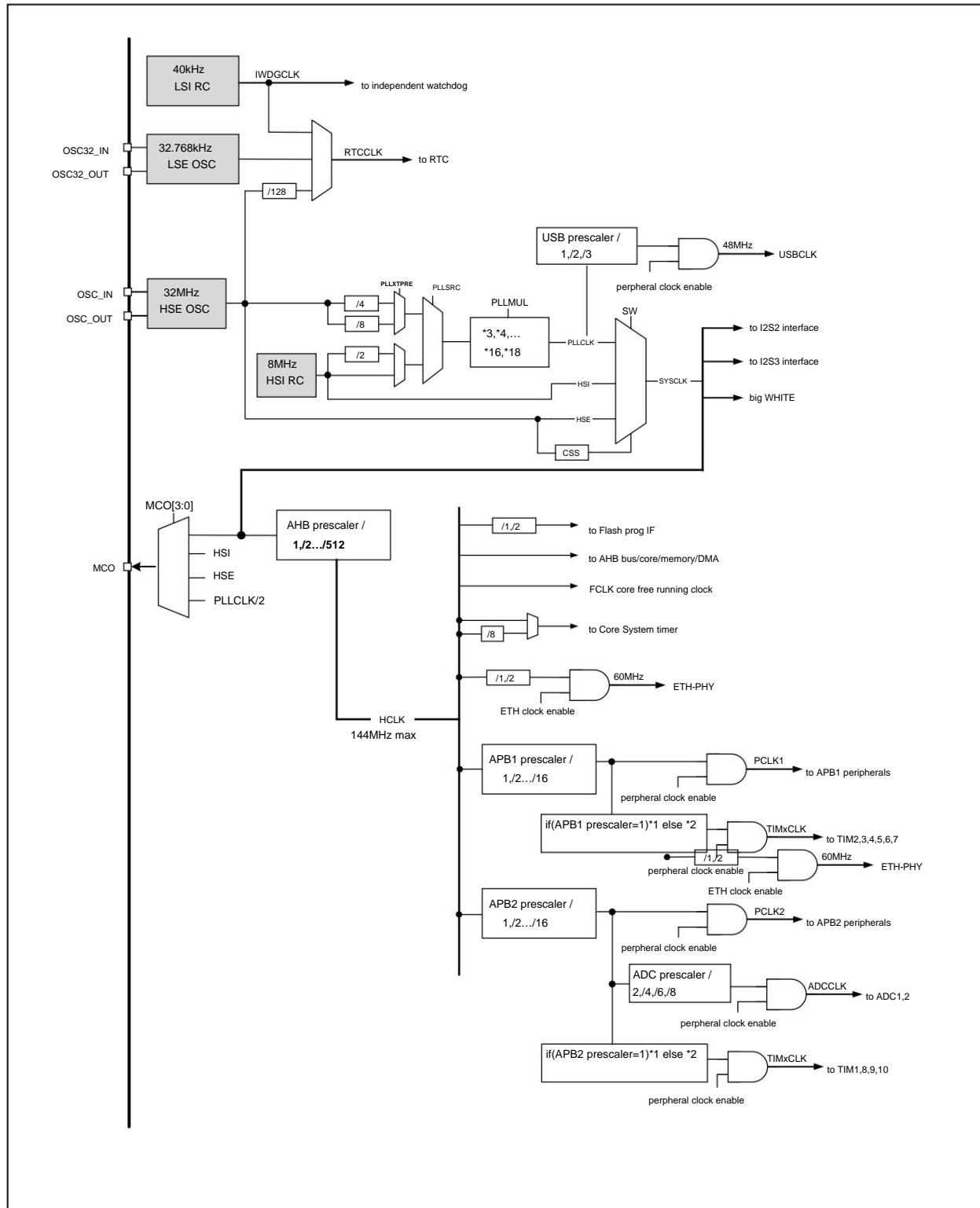
of the module work needs to be provided directly by the PLL clock. Figure 2-3 CH32V203 clock tree block diagram



Note: 1. When using the system with **HSI** as the primary clock source, it is recommended to use 8MHz for better stability. When the system wakes up from the shutdown or standby state with **USB 96MHz**, the

**HSI**

Figure 2-4 CH32V203RB clock tree block diagram



1. The external crystal or clock (HSE) of CH32V203RB is 32M. When using an external crystal, no load capacitor is required.

## 2.5 Function

### overview 2.5.1 RISC-V4B processor

RISC-V4B supports the IMAC subset of the RISC-V instruction set. The processor is managed in a modular manner, including fast programmable interrupt controller (PFIC), memory protection, branch prediction mode, extended instruction support and other units. Multiple groups of external buses are connected to external unit modules to realize interaction between external functional modules and the kernel. The processor can be flexibly applied to microcontrollers in different scenarios due to its minimalist instruction set, multiple working modes, and modular customization extensions. Design, such as small-area and low-power embedded scenarios, high-performance application operating system scenarios, etc. I Supports machine and user privilege modes I Fast programmable interrupt controller (PFIC) I Multi-level hardware interrupt stack I Serial 2-wire debugging interface I Standard memory protection design I Static or dynamic branch prediction, efficient jump, conflict detection mechanism I custom extension directive

### 2.5.2 On-chip memory and bootstrap mode

The built-in maximum 64K byte SRAM area is used to store data, and the data will be lost after power failure. The specific capacity should correspond to the chip model. Built-in maximum 224K bytes program flash storage area (Code FLASH), used for user's application program and constant data storage. These include zero-wait program run regions and non-zero-wait regions. The specific size of the area corresponds to the chip model.

Built-in 28K byte system storage area (System FLASH), used for system boot program storage (manufacturer solidified boot loader). 128 bytes are used for system non-volatile configuration information storage area, and 128 bytes are used for user selection word storage area. At start-up, one of three boot modes can be selected via the bootstrap pins (BOOT0 and BOOT1): I Boot from program flash memory I Boot from system memory I Boot from internal SRAM Boot load program storage In the system storage area, the contents of the program flash storage area can be reprogrammed through the USART1 and USB interface.

### 2.5.3 Power supply scheme I

VDD = 2.4~3.6V: supply power for some I/O pins and internal voltage regulator. I VIO = 2.4~3.6V: It supplies power for most I/O pins and the Ethernet module, and determines the pin output high voltage amplitude. normal

During operation, VIO voltage cannot be higher than VDD voltage.

I VDDA = 2.4~3.6V: supply power for high frequency RC oscillator, ADC, temperature sensor, DAC and analog part of PLL. The VDDA voltage must be the same as the VIO voltage (if VDD is powered off and VIO is powered, then VDDA must be powered and consistent with VIO). When using ADC , VDDA must not be less than 2.4V. I VBAT = 1.8 ~ 3.6V:

When VDD is turned off,

(through the internal power switcher) alone for RTC, external low frequency oscillator and post

Backup register power supply. (Pay attention to VBAT power supply)

### 2.5.4 Power supply monitor This

product integrates a power-on reset (POR)/power-down reset (PDR) circuit, which is always in the working state to ensure that the system works when the power supply exceeds 2.4V; when VDD is lower than the set threshold (VPOR/PDR), put the device in the reset state without using an external reset circuit. In addition, the system has a programmable voltage monitor (PVD), which needs to be turned on by software to compare the voltage of the VDD power supply with the set threshold VPVD. Turn on the corresponding edge interrupt of PVD, and when VDD drops to the PVD threshold or rises to the PVD threshold, the interrupt notification will be received. Refer to Chapter 4 for the values of VPOR/PDR and VPVD.

### 2.5.5 After the voltage regulator

is reset, the regulator is automatically turned on, and there are three operating modes according to the application

I On mode: normal running operation, providing stable core power | Low power

mode: when the CPU enters stop mode, the regulator can be selected for low power operation | Off

mode: automatically switches the regulator when the CPU enters standby mode In this mode, the voltage regulator output is in a high-impedance state, and the core

The power supply to the circuit is cut off, and the voltage regulator is in a state of zero consumption.

The regulator is always in on mode after reset, and is in shutdown mode when it is turned off in standby mode, which is a high impedance output.

#### 2.5.6 Low Power Mode The

system supports three low power modes, which can be selected to achieve the best balance under conditions such as low power consumption, short

startup time and

multiple wake-up events. | Sleep mode In sleep mode, only the CPU clock is stopped, but all peripheral clocks are powered normally, and the peripherals are in working state. This mode is the

shallowest low-power mode, but can achieve the

fastest wake-up. Exit

condition: Any interrupt or wakeup event. | Stop mode In this mode, FLASH enters low power consumption mode, and PLL, HSI RC oscillator and HSE crystal oscillator

Stop mode achieves the lowest power consumption without loss of register contents.

Exit conditions: any external interrupt/event (EXTI signal), external reset signal on NRST, IWDG reset, where the EXTI signal includes one of the 16 external I/O ports, PVD output, RTC alarm clock, and USB wake-up signal. | Standby mode In this mode,

the main LDO of the

system is turned off, the low-power LDO supplies power to the wake-up circuit, all other digital circuits are powered off, and the FLASH is in a power-off state. Waking up the system from standby mode will generate a reset and at the same time SBF (PWR\_CSR) will be set. After waking up, query the SBF status to know the low power consumption mode before waking up, and SBF is cleared by the CSBF (PWR\_CR) bit. In standby mode, the contents of the 32KB SRAM can be kept (depending on the program configuration

before sleep), and the contents of the backup registers are preserved. Exit conditions: Any external event (EXTI signal), external reset signal on NRST, IWDG reset, a Rising edge, where EXTI signal includes one of 16 external I/O ports, RTC alarm clock, USB wake-up signal.

#### 2.5.7 CRC (Cyclic Redundancy Check) calculation unit The

CRC (Cyclic Redundancy Check) calculation unit uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. In numerous applications, CRC-based techniques are used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC 60335-1 standard, which provides a means of detecting errors in flash memory, the CRC calculation unit can be used to calculate the signature of the software in real time and compare it with the signature produced when linking and generating the software.

#### 2.5.8 Fast Programmable Interrupt Controller (PFIC) The

product has a built-in Fast Programmable Interrupt Controller (PFIC), which supports up to 255 interrupt vectors and provides flexible interrupt management functions with minimum interrupt delay. The current product manages 8 core private interrupts and 88 peripheral interrupts, and other interrupt sources are reserved. PFIC's registers are accessible in both

user and machine privileged modes. |

88+3 individually maskable interrupts | Provide

a non-maskable interrupt NMI | Support hardware interrupt stack

(HPE), without instruction overhead |

Provide 4-way table-free interrupt (VTF) | Support vector

table mode of address or instruction module |

Interrupt Nesting depth can be configured up to 8 levels | Support interrupt tail link function

#### 2.5.9 External Interrupt/Event Controller (EXTI) The

external interrupt/event controller contains a total of 19 edge detectors for generating interrupt/event requests. Each interrupt line can be independently

Its trigger event (rising edge or falling edge or both edges) is configured independently and can be masked individually; the pending register maintains the status of all interrupt requests. EXTI can detect that the pulse width is less than the internal APB2 clock period. Up to 37 general-purpose I/O ports can optionally be connected to 16 external interrupt lines.

#### 2.5.10 General purpose DMA controller

The system has a built-in set of general-purpose DMA controllers to manage 8 channels, flexibly handle high-speed data transmission from memory to memory, peripheral to memory and memory to peripheral, and supports ring buffer mode. Each channel has dedicated hardware DMA request logic to support memory access requests from one or more peripherals. Access priority, transfer length, source address and destination address of transfer can be configured.

DMA is used for major peripherals including: general purpose/advanced timers TIMx, ADC, USART, I2C, SPI.

*Note: DMA and access CPU SRAM system after arbitration by the arbiter.*

#### 2.5.11 Clock and start system clock

source HSI is enabled by default. When no clock is configured or after reset, the internal 8MHz RC oscillator is used as the default CPU clock, and then an external 3~25MHz clock or PLL clock can be selected. When the clock security mode is enabled, if the HSE is used as the system clock (directly or indirectly), and the external clock failure is detected at this time, the system clock will automatically switch to the internal RC oscillator, and the HSE and PLL will be automatically turned off; In power mode, the system will automatically switch to the internal RC oscillator after waking up. If the clock interrupt is enabled, software can receive the corresponding interrupt.

Multiple prescalers are used to configure the frequency of AHB, and the high-speed APB (APB2) and low-speed APB (APB1) regions provide each peripheral clock, up to 144MHz, refer to the clock tree block diagram in Figure 2-3.

#### 2.5.12 RTC (Real Time Clock) and Backup Registers

The RTC and the backup register are in the backup power supply area inside the system. When VDD is valid, it is powered by VDD, and when VDD is invalid, it automatically switches to the VBAT pin for power supply.

The RTC real-time clock is a group of 32-bit programmable counters, and the time base supports 20-bit prescaler, which is used for the measurement of a long period of time. The clock reference source is a high-speed external clock divided by 128 (HSE/128), an external crystal low-frequency oscillator (LSE) or an internal low-power RC oscillator (LSI). The LSE also has a backup power supply area, so when the LSE is selected as the RTC time base, the RTC setting and time can remain unchanged after the system is reset or wakes up from standby mode. The backing registers contain up to 42 16-bit

registers that can be used to store 84 bytes of user application data. This data is called in standby After waking up, or when the system is reset or the power is reset, it can continue to be kept. When the intrusion detection function is enabled, once the intrusion detection signal is valid, all contents in the backup register will be cleared.

#### 2.5.13 ADC (analog/digital converter) and touch key capacitance detection (TKey)

The product is embedded with 2 12-bit analog/digital converters (ADC), sharing up to 16 external channels and 2 internal channel sampling, programmable channel sampling time, which can realize single, continuous, scan or intermittent conversion, And support dual ADC conversion mode. An analog watchdog function is provided to allow very precise monitoring of one or more selected channels for monitoring channel signal voltages. Supports external events to trigger conversions, and the trigger sources include internal signals of on-chip timers and external pins. Operations using DMA are supported.

ADC internal channel sampling includes one built-in temperature sensor sampling and one internal reference power sampling. A temperature sensor produces a voltage that varies linearly with temperature. The temperature sensor is internally connected to the IN16 input channel for converting the sensor output to a digital value. The touch key capacitive detection unit

provides up to 16 detection channels and multiplexes the external channels of the ADC module. The detection result is converted and output by the ADC module, and the state of the touch button is identified by the user software.

#### 2.5.14 Timer and Watchdog

Timers in the system include advanced timers, general-purpose timers, watchdog timers, and system time-base timers. different in series

The number of timers included in different products is different, please refer to Table 2-2 for details.

Table 2-2 Timer comparison

Timer Resolution		Count Type	Time	Base		DMA	function
advanced timer	TIM1	16 bit	up down up/down	APB2 time domain 16-bit divider		support	PWM complementary output, single pulse output input capture output compare Timing count
universal timer	TIM2	16 bit	up down up/down	APB1 time domain 16-bit divider		support	input capture output compare Timing count
	TIM3						
	TIM4						
	TIM5(1) 32-bit						
Window watchdog		7 bit	down		APB1 time domain 4 crossovers	not support	timing Reset the system (works normally)
Independent watchdog		12 bit	down		APB1 time domain 7 crossovers	not support	timing Reset system (normal + low power operation)
System time base timer		64-bit	up or down		SYSCLK or SYSCLK/8	Does not support timing	

Note 1: Applicable to CH32V203RBx.

#### I Advanced Control Timer The

advanced control timer is a 16-bit autoload up/down counter with a 16-bit programmable prescaler. except for the end

In addition to the integrated general-purpose timer function, it can be regarded as a three-phase PWM generator distributed to 6 channels, with complementary PWM with dead-time insertion

An output function that allows the timer to be updated after a specified number of counter cycles for repeated count cycles, brake functions, etc. advanced control

Many functions of the timer are the same as the general timer, and the internal structure is also the same, so the advanced control timer can be linked through the timer

The function cooperates with other TIM timers to provide synchronization or event chaining functions.

#### I General-purpose timer

The general-purpose timer is a 16-bit or 32-bit autoload up/down counter with a programmable 16-bit prescaler

and 4 independent channels, each supporting input capture, output compare, PWM generation, and single-pulse mode output. still pass

The timer chaining feature works in conjunction with advanced control timers to provide synchronization or event chaining. In debug mode, the counter can

is frozen and the PWM outputs are disabled, cutting off the switches controlled by these outputs. Any general purpose timer can be used to generate PWM

output. Each timer has an independent DMA request mechanism. These timers are also capable of processing signals from incremental encoders, as well as 1

Digital output to 3 Hall sensors.

#### I Independent watchdog

The independent watchdog is a free-running 12-bit down counter that supports 7 frequency division factors. by an internal independent 40KHz

An RC oscillator (LSI) provides the clock; because the LSI is independent of the main clock, it can operate in stop and standby modes. IWDG in the main program

out of sequence and can work completely independently, therefore, for resetting the entire system in the event of a problem, or as a free-wheeling timer for applications

The program provides timeout management. It can be configured as a software or hardware enabled watchdog through the option byte. In debug mode, the counter can

is frozen.

#### I window watchdog

The window watchdog is a 7-bit down counter and can be set to free run. can be used to reset the entire

system. It is driven by the main clock and has an early warning interrupt function; in debug mode, the counter can be frozen.

I System time base timer This is

a 64-bit optional increment or decrement counter that comes with the core controller, which is used to generate SYSTICK exceptions (abnormal number: 15), which can be dedicated to real-time operating systems and provide "heartbeat" for the system Rhythm can also be used as a standard 64-bit counter. With automatic reload function and programmable clock source.

#### 2.5.15 Communication

##### Interface 2.5.15.1 Universal Synchronous/Asynchronous Transceiver (USART)

The product provides 4 sets of universal synchronous/asynchronous receivers and transmitters. Supports full-duplex asynchronous communication, synchronous one-way communication and half-duplex single-wire communication, also supports LIN (local interconnection network), compatible with ISO7816 smart card protocol and IrDA SIR ENDEC transmission codec specification, and modem (CTS/RTS hardware flow control) operate. Also allows multiprocessor communication. It adopts fractional baud rate generator system and supports DMA operation for continuous communication.

##### 2.5.15.2 Serial Peripheral Interface (SPI)

2 sets of serial peripheral SPI interfaces, providing master or slave operation, dynamic switching. Support multi-master mode, full-duplex or half-duplex synchronous transmission, support basic SD card and MMC mode. Programmable clock polarity and phase, data width provides 8 or 16-bit options, hardware CRC generation/verification for reliable communication, and supports DMA operation for continuous communication.

##### 2.5.15.3 I2C bus There are up

to 2 I2C bus interfaces, which can work in multi-master mode or slave mode, and complete all I2C bus-specific timing, protocol,

Arbitration etc. It supports two communication speeds, standard and fast, and is compatible with SMBus2.0.

The I2C interface provides 7-bit or 10-bit addressing, and supports dual-slave addressing in 7-bit slave mode. Built-in hardware CRC generator /validator. It can operate with DMA and supports SMBus version 2.0/PMBus.

##### 2.5.15.4 Controller Area Network (CAN)

The CAN interface is compatible with specifications 2.0A and 2.0B (active), the baud rate is up to 1Mbits/s, and supports time-triggered communication functions. It can receive and send standard frames with 11-bit identifiers and extended frames with 29-bit identifiers. Has 3 send mailboxes and 2 receive FIFOs with 3 levels of depth. With 1 set of

CAN controller products, there are only 14 configurable filters, and share a dedicated 512-byte SRAM memory with the USBD module for data transmission and reception. When USBD and CAN are used at the same time, in order to prevent access to SRAM conflicts , USBD can only use the lower 384 bytes of space.

##### 2.5.15.5 Universal Serial Bus (USBD)

The product is embedded with a USB2.0 full-speed controller, which complies with the USB2.0 Fullspeed standard. USBD provides 16 configurable USB device endpoints, supports low-speed devices and full-speed devices, supports control/bulk/isochronous/interrupt transfer, double buffer mechanism, USB suspend/resume operation, and has standby/wake-up function. The 48MHz clock dedicated to USB is directly generated by the internal main PLL frequency division.

##### 2.5.15.6 Universal Serial Bus USB2.0 Full Speed Host/Device Controller (USBFS)

USB2.0 full-speed host controller and device controller (USBFS), follow the USB2.0 Fullspeed standard. Provides 16 configurable USB device endpoints and a set of host endpoints. Support control/bulk/isochronous/interrupt transfer, double buffer mechanism, USB bus suspend/resume operation, and provide standby/wake-up function. The 48MHz clock dedicated to the USBFS module is directly generated by the internal main PLL frequency division (PLL must be 144MHz or 96MHz or 48MHz).

#### 2.5.16 General-purpose input and output interface (GPIO)

The system provides 4 groups of GPIO ports with a total of 37 GPIO pins. Each pin can be configured by software as an output (push-pull or open-drain), an input (with or without pull-up or pull-down), or a multiplexed peripheral function port. Most GPIO pins are shared with digital or analog multiplexed peripherals. Except for ports with analog input functions, all GPIO pins have high current capability. Provides a locking mechanism to freeze IO configuration,

to avoid accidental writes to I/O registers.

Most of the IO pin power supply in the system is provided by VIO. By changing the VIO power supply, the high value of the IO pin output level will be changed to adapt to the external Communication interface level. Please refer to the pin description for specific pins.

### 2.5.17 Op Amp Comparator (OPA)

The product has 2 sets of op amps/comparators built in, and the internal selection is associated with ADC and TIMx peripherals, and its input and output can be configured by changing Make selections for multiple channels. Supports the external analog small signal to be amplified and sent to the ADC to realize small signal ADC conversion, and can also complete the signal No. comparator function, the comparison result is output by GPIO or directly connected to the input channel of TIMx.

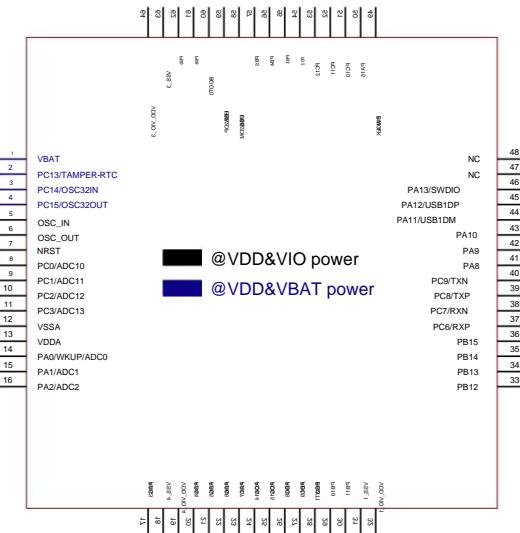
### 2.5.18 Serial 2-wire debug interface (SDI Serial Debug Interface)

The core comes with a serial 2-wire debug interface, including SWDIO and SWCLK pins. The default debugging interface after the system is powered on or reset The pin function is enabled.

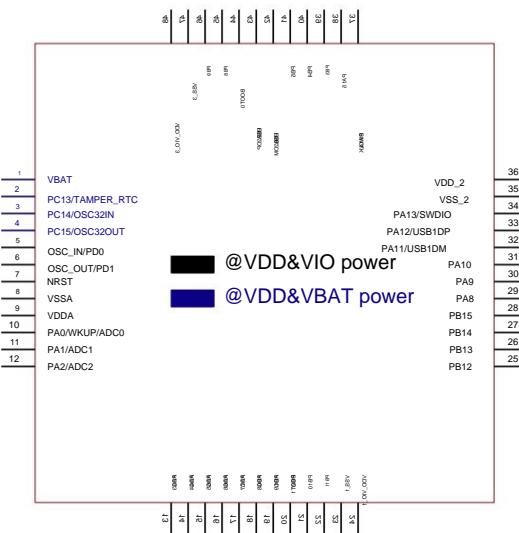
### Chapter 3 Pin Information

3.1 Pin arrangement of small and medium capacity general-purpose V203

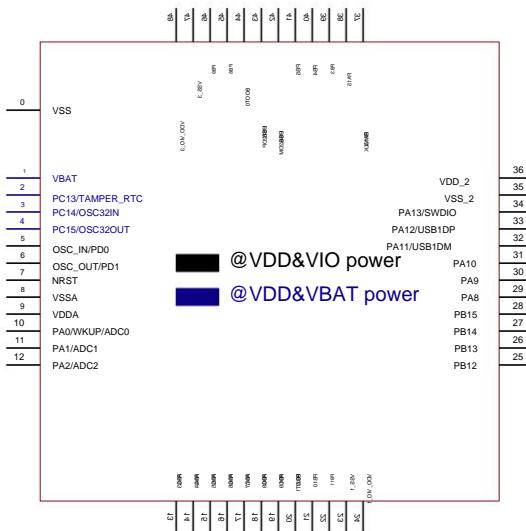
**CH32V203RBT6**



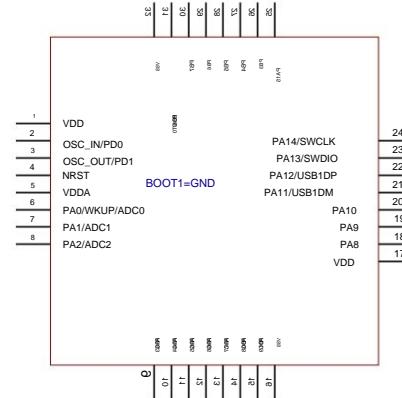
**CH32V203CxT6**



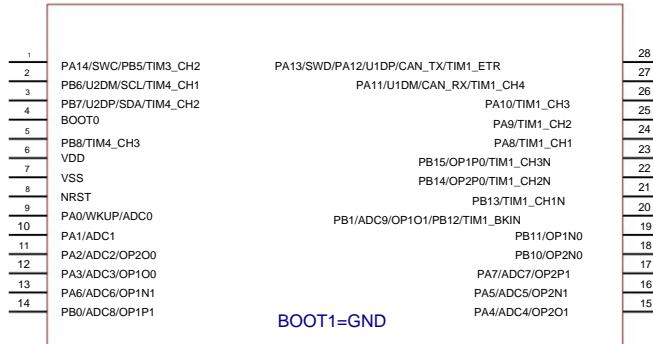
**CH32V203CxU6**



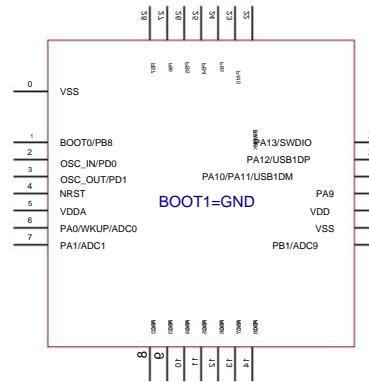
**CH32V203KxT6**



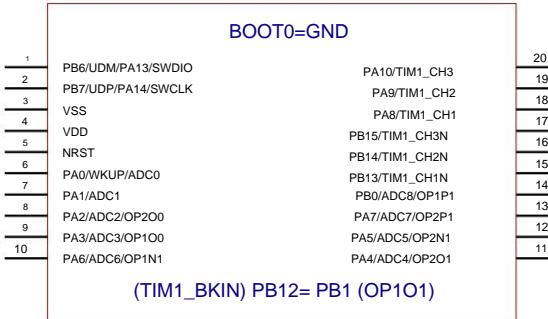
**CH32V203G8R6**



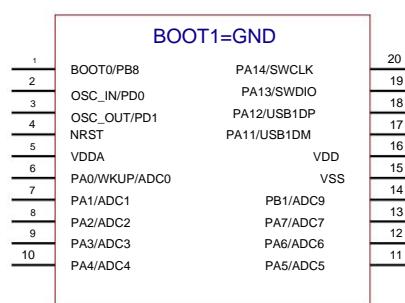
**CH32V203G6U6**



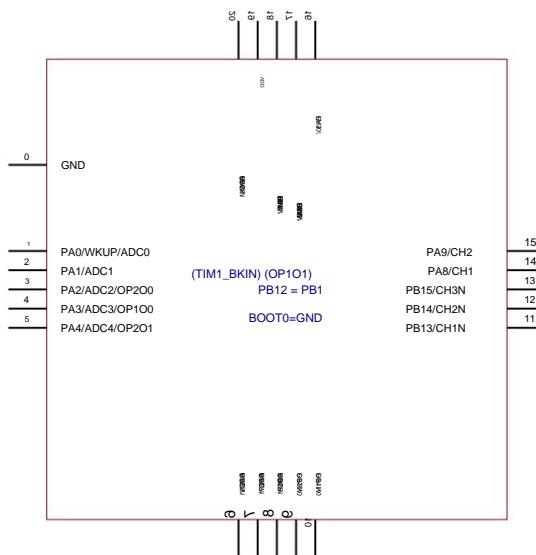
## CH32V203F8P6



## CH32V203F6P6



## CH32V203F8U6



### 3.2 Pin Description

**Table 3-1 CH32V203xx pin definition**

Note that the pin function descriptions in the following table are for all functions, not specific models. Peripheral resources vary between different models, please confirm whether this function is available according to the product model resource table before viewing.

**Table 3-1-1 QFN20/LQFP32/LQFP48/QFN48 pin definition**

pin number			pin name	pin type <sup>(1)</sup>	I/O electricity flat	main function (Reset back)	Default Multiplexing Function	Function Remapping Function
00NUD	01d01	02d01						
..		0	VSS	P	-	VSS		
..		1	VBAT	P	-	VBAT		
..		2	PC13- TAMPER-RTC(2)	I/O	-	PC13(3)	TAMPER-RTC	
..		3	PC14- OSC32_IN(2)	I/O/A	-	PC14(3)	OSC32_IN	
..		4	PC15- OSC32_OUT(2)	I/O/A	-	PC15(3)	OSC32_OUT	
-2		5	OSC_IN	I/A	- OSC_IN			PD0(4)
-3		6	OSC_OUT	O/A	- OSC_OUT			PD1(4)
-4		7	NRST	-	-	NRST		
..		8	VSSA	P	-	VSSA		
-5		9	VDDA	P	-	VDDA		
16		10	PA0-WKUP	I/O/A	-	PA0	BUY USART2_CTS ADC_IN0 TIM2_CH1 TIM2_ETR	TIM2_CH1_ETR_2
27		11	PA1	I/O/A	-	PA1	USART2_RTS ADC_IN1 TIM2_CH2	TIM2_CH2_2
3	8	12	PA2	I/O/A	-	PA2	USART2_TX ADC_IN2 TIM2_CH3 OPA2_OUT0	TIM2_CH3_1
49		13	PA3	I/O/A	-	PA3	USART2_RX ADC_IN3 TIM2_CH4 OPA1_OUT0	TIM2_CH4_1
510		14	PA4	I/O/A	-	PA4	SPI1_NSS USART2_CK ADC_IN4 OPA2_OUT1	

pin number			pin name	pin type <sup>(1)</sup> flat	main function (Reset back)	Default Multiplexing Function	Remapping Function
20ND	21GD1	21GD2					
6 11		15	PA5	I/O/A	PA5	SPI1_SCK ADC_IN5 OPA2_CH1N	USART4_TX_1
20 12		16	PA6	I/O/A	PA6	SPI1_MISO ADC_IN6 TIM3_CH1 OPA1_CH1N	TIM1_BKIN_1 USART4_CK_1
7 13		17	PA7	I/O/A	PA7	SPI1_MOSI ADC_IN7 TIM3_CH2 OPA2_CH1P	TIM1_CH1N_1 USART4_CTS_1
8 14		18	PB0	I/O/A	PB0	ADC_IN8 TIM3_CH3 OPA1_CH1P USART4_TX	TIM1_CH2N_1 TIM3_CH3_2
- 15		19	PB1	I/O/A	PB1	ADC_IN9 TIM3_CH4 OPA1_OUT1 USART4_RX	TIM1_CH3N_1 TIM3_CH4_2
		20	PB2(5)	I/O	FT BOOT1(5)	PB2 USART4_CK	
9 -		21	PB10	I/O/A	FT PB10	I2C2_SCL USART3_TX OPA2_CH0N	TIM2_CH3_2 TIM2_CH3_3
10 -		22	PB11	I/O/A	FT PB11	I2C2_SDA USART3_RX OPA1_CH0N	TIM2_CH4_2 TIM2_CH4_3
		23	VSS_1	P	VSS_1		
- 16			VSS	P	VSS		
		24	VDD_IO_1	P	VDD_IO_1		
- 17			VDD_	P	VDD_		
		25	PB12	I/O/A	FT PB12	SPI2_NSS I2C2_SMBA USART3_CK TIM1_BLOCK	
11 -		26	PB13	I/O/A	FT PB13	SPI2_SCK USART3_CTS TIM1_CH1WOMEN	

pin number			pin name	pin type <sup>(1)</sup> flat	main function (Reset back)	Default Multiplexing Function	Remapping Function	
20ND	21GD1	21GD2						
12		27	PB14	I/O/A	FT	PB14	SPI2_MISO TIM1_CH2N USART3_RTS OPA2_CH0P	
13		28	PB15	I/O/A	FT	PB15	SPI2_MOSI TIM1_CH3N OPA1_CH0P	
14 18 29			PA8	I/O	FT	PA8	USART1_CK TIM1_CH1 MCO	USART1_CK_1 TIM1_CH1_1
15 19		30	PA9	I/O	FT	PA9	USART1_TX TIM1_CH2	TIM1_CH2_1
16 20 31			PA10	I/O	FT	PA10	USART1_RX TIM1_CH3	TIM1_CH3_1
- 21		32	PA11	I/O/A	FT	PA11	USART1_CTS USBDM CAN1_RX TIM1_CH4	USART1_CTS_1 TIM1_CH4_1
	22 33		PA12	I/O/A	FT	PA12	USART1_RTS USBDP CAN1_TX TIM1_ETR	USART1_RTS_1 TIM1_ETR_1
17 23 34			PA13	I/O	FT SWDIO			PA13
..	35	VSS_2		P		VSS_2		
..	36	VDD_2		P		VDD_2		
18 24 37			PA14	I/O	FT SWCLK			PA14
- 25 38			PA15	I/O	FT	PA15		TIM2_CH1_ETR_1 TIM2_CH1_ETR_3 SPI1 NSS USART4_RTS_1
- 26 39			PB3	I/O	FT	PB3	USART4_CTS	TIM2_CH2_1 TIM2_CH2_3 SPI1_SCK
- 27 40			PB4	I/O	FT	PB4	USART4_RTS	TIM3_CH1_2 SPI1_MISO
- 28 41			PB5	I/O	FT	PB5	2C1_SMBA	TIM3_CH2_2 SPI1_MOSI USART4_RX_1
17 29 42			PB6	I/O	FT	PB6	I2C1_SCL TIM4_CH1	USART1_TX_1

pin number			pin name	pin type <sup>(1)</sup> electricity flat	main function (Reset back)	Default Multiplexing Function	Remapping Function
pin number	pin name	pin type <sup>(1)</sup> electricity flat					
						USBFS_DM	
18 30 43	PB7	I/O	FT	PB7	I2C1_SDA TIM4_CH2 USBFS_DP	USART1_RX_1	
	44	BOOT0		BOOT0			
	31	45	PB8	I/O/A	FT	PB8	I2C1_SCL CAN1_RX
	46	PB9	I/O/A	FT	PB9	TIM4_CH4	I2C1_SDA CAN1_TX
	47	VSS_3	P		VSS_3		
- 32		VSS	P		VSS		
	48	VDD_IO_3	P		VDD_IO_3		
19 1		VDD	P		VDD		

Table 3-1-2 TSSOP20(F8)/QSOP28(G8) pin definition

pin number		pin name	pin type <sup>(1)</sup> electricity flat	main function (Reset back)	Default Multiplexing Function	Remapping Function
(F8) (G8)	standard					
5	8	NRST		NRST		
6	9	PA0-WKUP	I/O/A		BUY USART2_CTS ADC_IN0 TIM2_CH1 TIM2_ETR	TIM2_CH1_ETR_2
7	10	PA1	I/O/A		USART2_RTS ADC_IN1 TIM2_CH2	TIM2_CH2_2
8	11	PA2	I/O/A		USART2_TX ADC_IN2 TIM2_CH3 OPA2_OUT0	TIM2_CH3_1
9	12	PA3	I/O/A		USART2_RX ADC_IN3 TIM2_CH4 OPA1_OUT0	TIM2_CH4_1
11	15	PA4	I/O/A		SPI1_NSS USART2_CK ADC_IN4	

pin number		pin name	pin type <sup>(1)</sup>	electricity flat	main function (Reset back)	Default reuse function remapping function
(F8) (G8)	STUO80					
					OPA2_OUT1	
12	16	PA5	I/O/A		PA5	SPI1_SCK ADC_IN5 OPA2_CH1N
10	13	PA6	I/O/A		PA6	SPI1_MISO ADC_IN6 TIM3_CH1 OPA1_CH1N
13	17	PA7	I/O/A		PA7	SPI1_MOSI ADC_IN7 TIM3_CH2 OPA2_CH1P
14	14	PB0	I/O/A		PB0	ADC_IN8 TIM3_CH3 OPA1_CH1P
	20	PB1	I/O/A		PB1	ADC_IN9 TIM3_CH4 OPA1_OUT1
	18	PB10	I/O/A	FT	PB10	OPA2_CH0N
	19	PB11	I/O/A	FT	PB11	OPA1_CH0N
	20	PB12	I/O/A	FT	PB12	TIM1_BLOCK
	20	PB1	I/O/A	FT	PB1	OPA1_OUT1
15	21	PB13	I/O/A	FT	PB13	TIM1_CH1WOMEN
16 22		PB14	I/O/A	FT	PB14	TIM1_CH2N OPA2_CH0P
17 23		PB15	I/O/A	FT	PB15	TIM1_CH3N OPA1_CH0P
18 24		PA8	I/O	FT	PA8	USART1_CK TIM1_CH1 MCO
19 25		PA9	I/O	FT	PA9	USART1_TX TIM1_CH2
20 26		PA10	I/O	FT	PA10	USART1_RX TIM1_CH3

pin number (F8) (G8)	pin name	pin type <sup>(1)</sup>	electricity flat	main function (Reset back)	Default Multiplexing Function	Remapping Function
STUOSS						
27	PA11	I/O/A	FT	PA11	USART1_CTS USBDM CAN1_RX TIM1_CH4	USART1_CTS_1 TIM1_CH4_1
28	PA12	I/O/A	FT	PA12	USART1_RTS USBDP CAN1_TX TIM1_ETR	USART1_RTS_1 TIM1_ETR_1
28	PA13	I/O	FT	SWDIO		PA13
3	VSS	P		VSS		
4	VDD	P		VDD		
2	PA14	I/O	FT	swclk		PA14
1	PB5	I/O	FT	PB5	2C1_SMBA	TIM3_CH2_2
1	PB6	I/O	FT	PB6	I2C1_SCL TIM4_CH1 USBFS_DM	USART1_TX_1
2	PB7	I/O	FT	PB7	I2C1_SDA TIM4_CH2 USBFS_DP	USART1_RX_1
4	BOOT0			BOOT0		
5	PB8	I/O/A	FT	PB8	TIM4_CH3	I2C1_SCL CAN1_RX

Table 3-1-3 TSSOP20(F6)/QFN28(G6) pin definition

pin number (F6) (G6)	pin name	pin type <sup>(1)</sup>	electricity flat	main function (Reset back)	Default Multiplexing Function	Remapping Function
0	VSS	P		VSS		
2	OSC_IN	I/A	-OSC_IN			PD0(4)
3	OSC_OUT	O/A	-OSC_OUT			PD1(4)
4	NRST			NRST		
5	VDDA	P		VDDA		
6	PA0-WKUP	I/O/A		PA0	BUY USART2_CTS ADC_IN0 TIM2_CH1 TIM2_ETR	TIM2_CH1_ETR_2

pin number		pin name	pin type <sup>(1)</sup>	level	main function (reset back)	Default Multiplexing Function	Remapping Function
(F6) (G6)	82NJD						
7	7	PA1	I/O/A	-	PA1	USART 2_RTS ADC_IN1 TIM2_C_H2	TIM2_CH2_2
8	8	PA2	I/O/A	-	PA2	USART 2_TX ADC_IN2 TIM2_C_H3 OPA2_OUT0	TIM2_CH3_1
9	9	PA3	I/O/A	-	PA3	USART 2_RX ADC_IN3 TIM2_C_H4 OPA1_OUT0	TIM2_CH4_1
10 10		PA4	I/O/A	-	PA4	SPI1_N_SS USART 2_CK ADC_IN4 OPA2_OUT1	
11	11	PA5	I/O/A	-	PA5	SPI1_S_CK ADC_IN5 OPA2_CH1N	
12	12	PA6	I/O/A	-	PA6	SPI1_MISO ADC_IN6 TIM3_C_H1 OPA1_CH1N	TIM1_BKIN_1
13 13		PA7	I/O/A	-	PA7	SPI1_MOSI ADC_IN7 TIM3_C_H2 OPA2_CH1P	TIM1_CH1N_1
	14	PB0	I/O/A	-	PB0	ADC_IN8 TIM3_C_H3 OPA1_CH1P	TIM1_CH2N_1 TIM3_CH3_2
14 15		PB1	I/O/A	-	PB1	ADC_IN9 TIM3_C_H4 OPA1_OUT1	TIM1_CH3N_1 TIM3_CH4_2
15	16	VSS	P	-	VSS		
16 17		VDD	P	-	VDD		
	18	PA9	I/O	FT	PA9	USART 1_TX TIM1_C_H2	TIM1_CH2_1
	19	PA10	I/O	FT	PA10	USART 1_RX TIM1_C_H3	TIM1_CH3_1

pin number		pin name	pin type <sup>(1)</sup>		main function (Reset back)	Default Multiplexing Function	Remapping Function
(F6) (G6)	82N20						
17 19		PA11	I/O/A	FT	PA11	USART1_CTS USBDM CAN1_RX TIM1_CH4	USART1_CTS_1 TIM1_CH4_1
18 20		PA12	I/O/A	FT	PA12	USART1_RTS USBDP CAN1_TX TIM1_ETR	USART1_RTS_1 TIM1_ETR_1
19	21	PA13	I/O	FT SWDIO			PA13
20 22		PA14	I/O	FT SWCLK			PA14
	23	PA15	I/O	FT	PA15		TIM2_CH1_ETR_1 TIM2_CH1_ETR_3 SPI1 NSS
	24	PB3	I/O	FT	PB3		TIM2_CH2_1 TIM2_CH2_3 SPI1_SCK
	25	PB4	I/O	FT	PB4		TIM3_CH1_2 SPI1_MISO
	26	PB5	I/O	FT	PB5	2C1_SMBA	TIM3_CH2_2 SPI1_MOSI
	27	PB6	I/O	FT	PB6	I2C1_SCL	USART1_TX_1
	28	PB7	I/O	FT	PB7	I2C1_SDA	USART1_RX_1
1 <sup>(6)</sup>	1 <sup>(6)</sup>	BOOT0			BOOT0		
		PB8	I/O/A	FT	PB8		I2C1_SCL CAN1_RX

Table 3-1-4 LQFP64M pin definition

pin number		pin name	pin type <sup>(1)</sup>		main function (Reset back)	Default Multiplexing Function	Remapping Function
LQFP64M							
1		VBAT	P		VBAT		
2		PC13-TAMPER-RTC(2)	I/O		PC13(3)	TAMPER-RTC	
3		PC14-OSC32_IN(2)	I/O/A		PC14(3)	OSC32_IN	
4		PC15-OSC32_OUT(2)	I/O/A		PC15(3)	OSC32_OUT	

pin number	pin name	pin type <sup>(1)</sup>	/ flat	main function (Reset back)	Default Multiplexing Function	Function Remapping Function
5	OSC_IN	I/A		OSC_IN		
6	OSC_OUT	O/A	- OSC_OUT			
7	NRST			NRST		
8	PC0	I/O/A		PC0	ADC_IN10	
9	PC1	I/O/A		PC1	ADC_IN11	
10	PC2	I/O/A		PC2	ADC_IN12	
11	PC3	I/O/A		PC3	ADC_IN13	
12	VSSA	P		VSSA		
13	VDDA	P		VDDA		
14	PA0-WKUP	I/O/A		PA0	BUY USART2_CTS ADC_IN0 TIM2_CH1 TIM2_ETR TIM5_CH1	TIM2_CH1_ETR_2
15	PA1	I/O/A		PA1	USART2_RTS ADC_IN1 TIM2_CH2 TIM5_CH2	TIM2_CH2_2
16	PA2	I/O/A		PA2	USART2_TX ADC_IN2 TIM2_CH3 OPA2_OUT0 TIM5_CH3	TIM2_CH3_1
17	PA3	I/O/A		PA3	USART2_RX ADC_IN3 TIM2_CH4 OPA1_OUT0 TIM5_CH4	TIM2_CH4_1
18	VSS_4	P		VSS_4		
19	VDD_IO_4	P		VDD_IO_4		
20	PA4	I/O/A		PA4	SPI1_NSS USART2_CK ADC_IN4 OPA2_OUT1	
21	PA5	I/O/A		PA5	SPI1_SCK ADC_IN5 OPA2_CH1N	USART1_CTS_2 USART1_CK_3

pin number	pin name	pin type <sup>(1)</sup>	/\ electricity flat	main function (Reset back)	Default Multiplexing Function	Function Remapping Function
LQFP64M						
22	PA6	I/O/A		PA6	SPI1_MISO ADC_IN6 TIM3_CH1 OPA1_CH1N	TIM1_BKIN_1 USART1_TX_3
23	PA7	I/O/A		PA7	SPI1_MOSI ADC_IN7 TIM3_CH2 OPA2_CH1P	TIM1_CH1N_1 USART1_RX_3
24	PC4	I/O/A		PC4	ADC_IN14	USART1_CTS_3
25	PC5	I/O/A		PC5	ADC_IN15	USART1_RTS_3
26	PB0	I/O/A		PB0	ADC_IN8 TIM3_CH3 OPA1_CH1P	TIM1_CH2N_1 TIM3_CH3_2 UART4_TX_1
27	PB1	I/O/A		PB1	ADC_IN9 TIM3_CH4 OPA1_OUT1	TIM1_CH3N_1 TIM3_CH4_2 UART4_RX_1
28	PB2(5)	I/O	FT	PB2 BOOT1(5)		
29	PB10	I/O/A	FT	PB10	I2C2_SCL USART3_TX OPA2_CH0N	TIM2_CH3_2 TIM2_CH3_3
30	PB11	I/O/A	FT	PB11	I2C2_SDA USART3_RX OPA1_CH0N	TIM2_CH4_2 TIM2_CH4_3
31	VSS_1	P		VSS_1		
32	VDD_IO_1	P		VDD_IO_1		
33	PB12	I/O/A	FT	PB12	SPI2_NSS I2C2_SMBA USART3_CK TIM1_BLOCK	
34	PB13	I/O/A	FT	PB13	SPI2_SCK USART3_CTS TIM1_CH1WOMEN	USART3_CTS_1
35	PB14	I/O/A	FT	PB14	SPI2_MISO TIM1_CH2N USART3_RTS OPA2_CH0P	USART3_RTS_1
36	PB15	I/O/A	FT	PB15	SPI2_MOSI TIM1_CH3N OPA1_CH0P	USART1_TX_2

pin number	pin name	pin type <sup>(1)</sup>	/  electricity flat	main function (Reset back)	Default Multiplexing Function Remapping Function	
37	PC6	I/O/A	FT	PC6	ETH_RXP	TIM3_CH1_3
38	PC7	I/O/A	FT	PC7	ETH_RXN	TIM3_CH2_3
39	PC8	I/O/A	FT	PC8	ETH_TXP	TIM3_CH3_3
40	PC9	I/O/A	FT	PC9	ETH_TXN	TIM3_CH4_3
41	PA8	I/O	FT	PA8	USART1_CK TIM1_CH1 MCO	USART1_CK_1 USART1_RX_2 TIM1_CH1_1
42	PA9	I/O	FT	PA9	USART1_TX TIM1_CH2	USART1_RTS_2 TIM1_CH2_1
43	PA10	I/O	FT	PA10	USART1_RX TIM1_CH3	USART1_CK_2 TIM1_CH3_1
44	PA11	I/O/A	FT	PA11	USART1_CTS USBDM CAN1_RX TIM1_CH4	USART1_CTS_1 TIM1_CH4_1
45	PA12	I/O/A	FT	PA12	USART1_RTS USBDP CAN1_TX TIM1_ETR	USART1_RTS_1 TIM1_ETR_1
46	PA13	I/O	FT	SWDIO		PA13
-	VSS_2	P	-	VSS_2		
-	VDD_2	P	-	VDD_2		
47	NC			NC		
48	NC			NC		
49	PA14	I/O	FT	swclk		PA14
50	PA15	I/O	FT	PA15		TIM2_CH1_ETR_1 TIM2_CH1_ETR_3 SPI1 NSS
51	PC10	I/O	FT	PC10	UART4_TX	USART3_TX_1
52	PC11	I/O	FT	PC11	UART4_RX	USART3_RX_1
53	PC12	I/O	FT	PC12		USART3_CK_1
54	PD2	I/O	FT	PD2	TIM3_ETR	TIM3_ETR_2 TIM3_ETR_3
55	PB3	I/O	FT	PB3		TIM2_CH2_1 TIM2_CH2_3 SPI1_SCK
56	PB4	I/O	FT	PB4		TIM3_CH1_2 SPI1_MISO
57	PB5	I/O	FT	PB5	2C1_SMBA	TIM3_CH2_2 SPI1_MOSI

pin number	pin name	pin type <sup>(1)</sup>	/I electricity flat	main function (Reset back)	Default Multiplexing Function Remapping Function	
LQFP64M						
58	PB6	I/O	FT	PB6	I2C1_SCL TIM4_CH1 USBFS_DM	USART1_TX_1
59	PB7	I/O	FT	PB7	I2C1_SDA TIM4_CH2 USBFS_DP	USART1_RX_1
60	BOOT0	-	-	BOOT0		
61	PB8	I/O/A	FT	PB8	TIM4_CH3	I2C1_SCL CAN1_RX
62	PB9	I/O/A	FT	PB9	TIM4_CH4	I2C1_SDA CAN1_TX
63	VSS_3	P	-	VSS_3		
64	VDD_IO_3	P	-	VDD_IO_3		

Note 1: Explanation of table abbreviations

**I** = TTL/CMOS level Schmitt input;

**O** = CMOS Level three-state output;

**A** = analog signal input or output;

**P** = power supply;

**FT** = 5V tolerant;

**ON** = RF signal input and output (antenna);

### 3.3 Pin Alternate Function

Note that the pin function descriptions in the following table are for all functions, not specific models. Peripheral resources vary between different models, please confirm whether this function is available according to the product model resource table before viewing.

Table 3-2 CH32V203xx pin multiplexing function

Reuse pin	ADC	TIM1	TIM 2/3/4/5	UART USE	USB	SYS	2C	SPI	ETH	OPA	CAN
PA0	ADC_IN0		TIM2_CH1 TIM2_CH1_ETR_2 TIM2_ETR TIM5_CH1	USART2_CTS		BUY					
PA1	ADC_IN1		TIM2_CH2 TIM2_CH2_2 TIM5_CH2	USART2_RTS							
PA2	ADC_IN2		TIM2_CH3 TIM2_CH3_1 TIM5_CH3	USART2_TX						OPA2_OUT0	
PA3	ADC_IN3		TIM2_CH4 TIM2_CH4_1 TIM5_CH4	USART2_RX						OPA1_OUT0	
PA4	ADC_IN4			USART2_CK				SPI1_NSS		OPA2_OUT1	
PA5	ADC_IN5			USART1_CTS_2 USART1_CK_3 USART4_TX_1				SPI1_SCK		OPA2_CH1N	
PA6	ADC_IN6	TIM1_BKIN_1	TIM3_CH1	USART1_TX_3 USART4_CK_1				SPI1_MISO		OPA1_CH1N	
PA7	ADC_IN7	TIM1_CH1N_1	TIM3_CH2	USART1_RX_3 USART4_CTS_1				SPI1_MOSI		OPA2_CH1P	
PA8		TIM1_CH1 TIM1_CH1_1		USART1_CK USART1_CK_1 USART1_RX_2		MCO					
PA9		TIM1_CH2 TIM1_CH2_1		USART1_TX USART1_RTS_2							
PA10		TIM1_CH3 TIM1_CH3_1		USART1_RX USART1_CK_2							
PA11		TIM1_CH4 TIM1_CH4_1		USART1_CTS USART1_CTS_1	USBDM						CAN1_RX
PA12		TIM1_ETR TIM1_ETR_1		USART1_RTS USART1_RTS_1	USBDP						CAN1_TX
PA13						SWDIO					
PA14						swclk					
PA15			TIM2_CH1_ETR_1 TIM2_CH1_ETR_3	USART4_RTS_1				SPI1_NSS			
PB0	ADC_IN8	TIM1_CH2N_1	TIM3_CH3 TIM3_CH3_2	UART4_TX_1 USART4_TX						OPA1_CH1P	
PB1	ADC_IN9	TIM1_CH3N_1	TIM3_CH4 TIM3_CH4_2	UART4_RX_1 USART4_RX						OPA1_OUT1	
PB2				USART4_CK		BOOT1					
PB3			TIM2_CH2_1 TIM2_CH2_3	USART4_CTS				SPI1_SCK			
PB4			TIM3_CH1_2	USART4_RTS				SPI1_MISO			
PB5			TIM3_CH2_2	USART4_RX_1			2C1_SMBA	SPI1_MOSI			
PB6			TIM4_CH1	USART1_TX_1	USBFS_DM		I2C1_SCL				
PB7			TIM4_CH2	USART1_RX_1	USBFS_DP		I2C1_SDA				
PB8			TIM4_CH3				I2C1_SCL				CAN1_RX
PB9			TIM4_CH4				I2C1_SDA				CAN1_TX
PB10			TIM2_CH3_2 TIM2_CH3_3	USART3_TX			I2C2_SCL			OPA2_CH0N	

Reuse pin	ADC	TIM1	TIM 2/3/4/5	UART USE	USB	SYS	2C	SPI	ETH	OPA	CAN
PB11			TIM2_CH4_2 TIM2_CH4_3	USART3_RX			I2C2_SDA			OPA1_CH0N	
PB12		TIM1_BLOCK		USART3_CK			I2C2_SMBA	SPI2_NSS			
PB13		TIM1_CHIN		USART3_CTS USART3_CTS_1				SPI2_SCK			
PB14		TIM1_CH2N		USART3_RTS USART3_RTS_1				SPI2_MISO		OPA2_CH0P	
PB15		TIM1_CH3N		USART1_TX_2				SPI2_MOSI		OPA1_CH0P	
PC0	ADC_IN10										
PC1	ADC_IN11										
PC2	ADC_IN12										
PC3	ADC_IN13										
PC4	ADC_IN14			USART1_CTS_3							
PC5	ADC_IN15			USART1_RTS_3							
PC6			TIM3_CH1_3						ETH_RXP		
PC7			TIM3_CH2_3						ETH_RXN		
PC8			TIM3_CH3_3						ETH_TXP		
PC9			TIM3_CH4_3						ETH_TXN		
PC10				UART4_TX USART3_TX_1							
PC11				UART4_RX USART3_RX_1							
PC12				USART3_CK_1							
PC13						TAMPER-RTC					
PC14						OSC32_IN					
PC15						OSC32_OUT					
PD0						OSC_IN					
PD1						OSC_OUT					
PD2			TIM3_ETR TIM3_ETR_2 TIM3_ETR_3								

## Chapter 4 Electrical Characteristics

## 4.1 Test conditions

Unless otherwise specified and marked, all voltages are referenced to VSS.

All minimum and maximum values are guaranteed under worst-case ambient temperature, supply voltage and clock frequency conditions. Typical values are based on

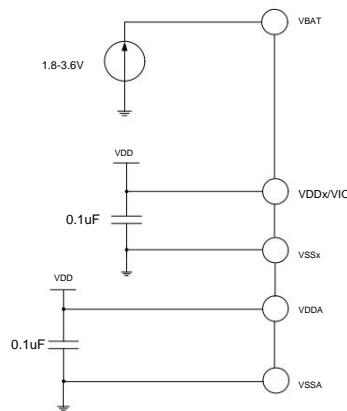
It is used for design guidance under normal temperature 25°C and VDD = 3.3V environment.

For data obtained through comprehensive evaluation, design simulation or process characterization, no testing will be performed on the production line. On the basis of comprehensive assessment

Basically, the minimum and maximum values are statistically obtained through sample testing. Unless otherwise specified as measured values, the characteristic parameters are comprehensively evaluated or Design Guaranteed.

Power supply scheme:

Figure 4-1 Typical circuit of conventional power supply



## 4.2 Absolute maximum

Critical or exceeding the absolute maximum value may cause the chip to malfunction or even be damaged.

Table 4-1 Absolute maximum parameter table

symbol	describe	min	max	unit	
Ambient temperature when TA is working		-40	85	°C	
Ambient temperature when TS is stored		-40	125	°C	
VDD-VSS external main supply voltage (including VDDA and VDD)		-0.3	4.0	IN	
VIO-VSS	IO Domain Terminal Supply Voltage	-0.3	4.0	IN	
COME	Input voltage on FT (5V tolerant) pin Input	VSS-0.3	5.5	IN	
	voltage on other pins  VDD_x	VSS-0.3	VDD+0.3		
Voltage difference between different main power supply pins  VIO_x	Voltage difference between different IO terminal		50	mV	
power supply pins  VSS_x	Voltage difference between different ground pins		50	mV	
VESD(HBM)	ESD Electrostatic Discharge Voltage (Human Body Model, Non-Contact)	4K		IN	
	USB pins (PA11, PA12)	3K		IN	
IVDD Total	current through VDD/VDDA/VIO power lines (supply current)		150		mA
IVss	total current through VSS ground (outgoing current)		150		
IIO	Sink current on any I/O and control pin Output		25		
	current on any I/O and control pin		-25		
IINJ(PIN)	NRST pin injection current		+/-5		
	OSC_IN pin of HSE and OSC_IN pin of LSE inject current		+/-5		

	Injection current of other pins		+/-5	
ÿIINJ(PIN)	Total injection current of all IO and control pins		+/-25	

## 4.3 Electrical parameters

## 4.3.1 Working conditions

Table 4-2 General working conditions

Symbol parameters	FHCLK internal	condition	min max	unit	
AHB clock	frequency FPCLK1 internal		144	MHz	
APB1 clock	frequency FPCLK2 internal		144	MHz	
APB2 clock	frequency		144	MHz	
VDD standard working voltage			2.4	3.6	IN
		use usb	3.0	3.6	
VIO most	IO pin output voltage	VIO cannot be higher than VDD	2.4	3.6	IN
VDDA	analog part operating voltage (ADC is not used) VDDA must be the same as VIO , VREF+	Cannot be higher than VDDA, VREF-equal to VSS	2.4	3.6	IN
VBAT <sup>(1)</sup>	The operating voltage of the backup unit cannot be greater than VDD		1.8	3.6	IN
T Ambient	temperature		-40	85	ÿ
TJ junction	temperature range		-40	85	ÿ

Note: 1. The connection between battery and VBAT should be as short as possible.

Table 4-3 Power-on and power-off conditions

symbol	parameter	condition	min max	unit	
tVDD	VDD rising rate		0	ÿ	us/V
	VDD drop rate		30	ÿ	

## 4.3.2 Embedded Reset and Power Control Module Features

Table 4-4 Reset and voltage monitoring (PDR selects high threshold gear)

symbol	Parameter condition	PLS[2:0] = 000 (rising edge)	Min	Typ	Max	Unit	
VPVD <sup>(1)</sup>	Programmable voltage detector for electrical flat selection	PLS[2:0] = 000 (falling edge)		2.39			IN
		PLS[2:0] = 001 (rising edge)		2.31			IN
		PLS[2:0] = 001 (falling edge)		2.56			IN
		PLS[2:0] = 001 (rising edge)		2.48			IN
		PLS[2:0] = 010 (rising edge)		2.65			IN
		PLS[2:0] = 010 (falling edge)		2.57			IN
		PLS[2:0] = 011 (rising edge)		2.78			IN
		PLS[2:0] = 011 (falling edge)		2.69			IN
		PLS[2:0] = 100 (rising edge)		2.89			IN
		PLS[2:0] = 100 (falling edge)		2.81			IN
		PLS[2:0] = 101 (rising edge)		3.05			IN
		PLS[2:0] = 101 (falling edge)		2.96			IN
		PLS[2:0] = 110 (rising edge)		3.17			IN
		PLS[2:0] = 110 (falling edge)		3.08			IN
		PLS[2:0] = 111 (rising edge)		3.31			IN

		PLS[2:0] = 111 (falling edge)		3.21		IN
VPVDhyst	VVD hysteresis			0.08		IN
VPOR/PDR	power-on/power-down reset threshold	rising edge	1.9	2.2	2.4	IN
		falling edge	1.9	2.2	2.4	IN
VPDRhyst	PDR hysteresis			20		mV
tRSTTEMPO	power-on		24	28	30	mS
	reset other resets		8	10	30	

Note: 1. Test value at room temperature.

#### 4.3.3 Built-in reference voltage

Table 4-5 Built-in reference voltage

Symbolic parameter	VREFINT built-	condition	minimum value		unit of maximum
in reference voltage		TA = -40~85°C	1.17	1.2	1.23 IN
TS_vrefint	When reading the internal reference voltage , ADC sampling time				17.1 us

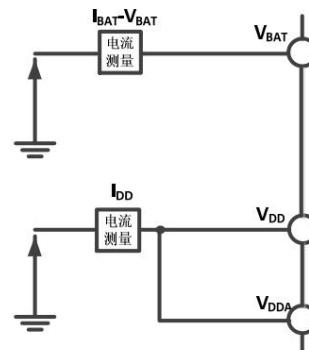
#### 4.3.4 Supply current characteristics

Current consumption is a composite of several parameters and factors, including operating voltage, ambient temperature, I/O pin

Load, product software configuration, operating frequency, I/O pin toggle rate, program location in memory, and executed code, etc.

The current consumption measurement method is as follows:

Figure 4-2 Current consumption measurement



The microcontroller is under the following conditions:

In the case of normal temperature VDD = 3.3V, when testing: all IO ports are configured with pull-up input, only one HSE or HSI is turned on, HSE=8M, HSI=8MHz

(Calibrated), FPLCK1=FHCLK/2, FPLCK2=FHCLK, when FHCLK>8MHz, PLL is turned on. Enables or disables the power consumption of all peripheral clocks.

Table 4-6-1 Typical current consumption in run mode, data processing code runs from internal flash memory (apply V203 chip)

symbol	parameter	condition	Typical value		unit
			Enable all peripherals	Disable all peripherals	
IDD <sup>(1)</sup>	in run mode supply current	external clock	FHCLK = 144MHz	12.08	mA
			FHCLK = 72MHz	6.43	
			FHCLK = 48MHz	4.51	
			FHCLK = 36MHz	4.12	
			FHCLK = 24MHz	2.72	
			FHCLK = 16MHz	2.18	

FHCLK = 8MHz	1.21	0.99
FHCLK = 4MHz	0.92	0.80
FHCLK = 500KHz	0.65	0.64
run at high speed inside RC oscillator (HSI), Use AHB prescaler to reduce the frequency	FHCLK = 144MHz	11.72
	FHCLK = 72MHz	6.02
	FHCLK = 48MHz	4.13
	FHCLK = 36MHz	3.31
	FHCLK = 24MHz	2.23
	FHCLK = 16MHz	1.68
	FHCLK = 8MHz	0.86
	FHCLK = 4MHz	0.56
	FHCLK = 500KHz	0.31
		0.29

Note: 1. The above are measured parameters. 2. During the test, when all peripheral clocks are turned off, serial port 1 and GPIOA clocks are not turned off.

Table 4-6-2 Typical current consumption in running mode, data processing code runs from internal flash memory (using V203RBT6 chip)

symbol	parameter	condition	typical value		unit
			Enable all peripherals	Disable all peripherals <sup>(2)</sup>	
IDD <sup>(1)</sup>	in run mode supply current	external clock	FHCLK = 144MHz	21.37	16.77
			FHCLK = 72MHz	10.91	8.73
			FHCLK = 48MHz	7.58	6.16
			FHCLK = 36MHz	6.49	5.29
			FHCLK = 24MHz	4.59	3.61
			FHCLK = 16MHz	3.13	2.59
			FHCLK = 8MHz	2.0	1.71
			FHCLK = 4MHz	1.42	1.28
		run at high speed inside RC oscillator (HSI), Use AHB prescaler to reduce the frequency	FHCLK = 500KHz	1.0	0.95
			FHCLK = 144MHz	20.75	16.27
		run at high speed inside RC oscillator (HSI), Use AHB prescaler to reduce the frequency	FHCLK = 72MHz	10.74	8.53
			FHCLK = 48MHz	7.42	5.98
			FHCLK = 36MHz	5.96	5.05
			FHCLK = 24MHz	4.62	3.41
			FHCLK = 16MHz	3.03	2.49
			FHCLK = 8MHz	1.66	1.42
			FHCLK = 4MHz	1.11	1.0
			FHCLK = 500KHz	0.63	0.62

Note: 1. The above are measured parameters. 2. During the test, when all peripheral clocks are turned off, serial port 1 and GPIOA clocks are not turned off.

Table 4-7-1 Typical current consumption in sleep mode, data processing code runs from internal flash memory or SRAM (application V203 chip)

symbol	parameter	condition	Typical value		unit
			Enable all peripherals	Disable all peripherals <sup>(2)</sup>	
IDD <sup>(1)</sup>	sleep mode supply current	external clock	FHCLK = 144MHz	7.37	3.05
			FHCLK = 72MHz	4.0	1.88

(At this time the peripheral power and clock protection hold)	FHCLK = 48MHz FHCLK = 36MHz FHCLK = 24MHz FHCLK = 16MHz FHCLK = 8MHz FHCLK = 4MHz FHCLK = 500KHz	FHCLK = 48MHz	2.9	1.7	
		FHCLK = 36MHz	2.9	1.48	
		FHCLK = 24MHz	1.93	1.2	
		FHCLK = 16MHz	1.64	1.0	
		FHCLK = 8MHz	0.94	0.72	
		FHCLK = 4MHz	0.78	0.66	
		FHCLK = 500KHz	0.63	0.62	
	run at high speed inside RC oscillator (HSI), Use AHB prescaler to reduce the frequency	FHCLK = 144MHz	7.1	2.72	
		FHCLK = 72MHz	3.65	1.56	
		FHCLK = 48MHz	2.56	1.15	
		FHCLK = 36MHz	2.17	1.06	
		FHCLK = 24MHz	1.46	0.76	
		FHCLK = 16MHz	1.2	0.68	
		FHCLK = 8MHz	0.6	0.4	
		FHCLK = 4MHz	0.44	0.34	
		FHCLK = 500KHz	0.3	0.28	

Note: 1. The above are measured parameters. 2. During the test, serial port 1, GPIOA clock, and power module clock are not turned off.

Table 4-7-2 Typical current consumption in sleep mode, data processing code runs from internal flash memory or SRAM (application V203RBT6 chip)

symbol	parameter	condition	typical value		unit
			Enable all peripherals	Disable all peripherals <sup>(2)</sup>	
IDD <sup>(1)</sup>	sleep mode supply current (At this time the peripheral power and clock protection hold)	external clock	FHCLK = 144MHz	8.17	3.69
			FHCLK = 72MHz	4.75	2.16
			FHCLK = 48MHz	3.35	1.69
			FHCLK = 36MHz	3.29	1.89
			FHCLK = 24MHz	2.18	1.26
			FHCLK = 16MHz	1.63	1.11
			FHCLK = 8MHz	1.23	0.98
			FHCLK = 4MHz	1.06	0.94
			FHCLK = 500KHz	0.97	0.91
	run at high speed inside RC oscillator (HSI), Use AHB prescaler to reduce the frequency		FHCLK = 144MHz	7.65	3.44
			FHCLK = 72MHz	4.61	2.02
			FHCLK = 48MHz	3.22	1.55
			FHCLK = 36MHz	2.73	1.44
			FHCLK = 24MHz	1.9	1.1
			FHCLK = 16MHz	1.48	0.95
			FHCLK = 8MHz	0.93	0.69
			FHCLK = 4MHz	0.75	0.63
			FHCLK = 500KHz	0.58	0.56

Note: 1. The above are measured parameters. 2. During the test, serial port 1, GPIOA clock, and power module clock are not turned off.

Table 4-8-1 Typical current consumption in stop and standby mode (using V203 chip)

symbol	parameter		typical unit	
IDD	Supply current in stop mode	condition the regulator is in run mode, the low-speed and high-speed internal state (no independent watchdog)	54	uA
		Both the RC oscillator and the external oscillator are turned off		
	Supply current in standby mode	regulator is in low-power mode, low-speed and high-speed internal Both the internal RC oscillator and the external oscillator are turned off status (no independent watchdog, PVD off), RAM enters low-power mode	9.4	
		The low-speed internal RC oscillator and independent watchdog are at On state, all RAMs are not charged	1.3	
	Supply current in standby mode	The low-speed internal RC oscillator is on, independent Standby watchdog is off, all RAM is not charged	1.3	
		LSI/LSE/RTC/IWDG off, 2K_RAM powered and in low power state	1.16	
		LSI/LSE/RTC/IWDG off, All RAM unpowered	0.5	
IDD_VBAT	Supply current in backup area (Remove VDD and VDDA, only make powered by VBAT)	Low speed external oscillator and RTC are on	1.3	

Note: The above are the measured parameters

Table 4-8-2 Typical current consumption in stop and standby mode (using V203RBT6 chip)

symbol	parameter		typical unit	
IDD	Supply current in stop mode	condition the regulator is in run mode, the low-speed and high-speed internal state (no independent watchdog)	253.4	uA
		Both the RC oscillator and the external oscillator are turned off		
	Supply current in standby mode	regulator is in low-power mode, low-speed and high-speed internal Both the internal RC oscillator and the external oscillator are turned off status (no independent watchdog, PVD off), RAM enters low-power mode	23.8	
		The low-speed internal RC oscillator and independent watchdog are at On state, all RAMs are not charged	1.3	
	Supply current in standby mode	The low-speed internal RC oscillator is on, independent Standby watchdog is off, all RAM is not charged	1.3	
		LSI/LSE/RTC/IWDG off, 32K_RAM powered and in low power state	2.18	
		LSI/LSE/RTC/IWDG off, 2K_RAM is powered and in low power state	0.86	
		LSI/LSE/RTC/IWDG off, All RAM is unpowered	0.7	
IDD_VBAT	Supply current in backup area (Remove VDD and VDDA, only make powered by VBAT)	Low speed external oscillator and RTC are on	1.23	

Note: The above are the measured parameters

#### 4.3.5 External Clock Source Characteristics

Table 4-9 From external high-speed clock

Symbolic parameters	condition	Min	Typ	Max	Unit		
FHSE_ext external clock frequency	Applicable to V203RBT6	3	8	25		MHz	
VHSEH <sup>(1)</sup> OSC_IN input pin high level voltage			0.8VIO	32			
VHSEL <sup>(1)</sup> OSC_IN input pin low level voltage			0		0.2VIO	IN	
Cin(HSE) OSC_IN input capacitance				5		pF	
DuCy(HSE) duty cycle				50		%	
THE OSC_IN input leakage current					±1	uA	

Note: 1. Failure to meet this condition may cause level recognition errors.

Figure 4-3 External high-frequency clock source circuit

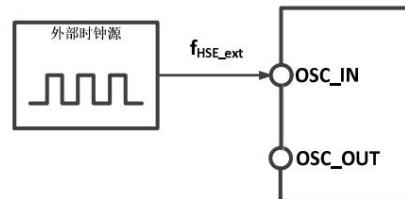


Table 4-10 From external low-speed clock

Symbolic parameters	condition	Min	Typ	Max	Unit		
FLSE_ext user external clock frequency			32.768	1000	KHz		
VLSEH OSC32_IN input pin high level voltage		0.8VDD			VDD	IN	
VLSEL OSC32_IN input pin low level voltage		0			0.2VDD	IN	
Eat (LSE) OSC32_IN input capacitance			5			pF	
DuCy(LSE) duty cycle			50			%	
THE OSC32_IN input leakage current				±1	uA		

Figure 4-4 External low-frequency clock source circuit

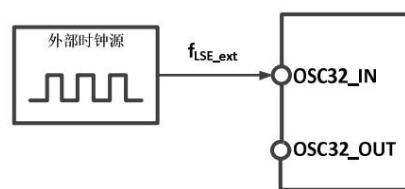


Table 4-11 High-Speed External Clock Generated Using a Crystal/Ceramic Resonator

symbol	parameter condition	Min	Typ	Max	Unit		
FOSC_IN resonator frequency	Applicable to V203RBT6	3	8	25		MHz	
				32(2)			
Recommended Load			250			kΩ	
C	Capacitance for RF Feedback Resistor and Corresponding Crystal RS=60 <sup>(1)</sup> Series impedance RS			30		pF	

I <sub>2</sub>	HSE drive current	VDD = 3.3V, 20p load start VDD		0.53		mA
gm oscillator transconductance		stable,		17.5		mA/V
tSU(HSE) start-up time	8M crystal			2.5		ms

1: 25MHz 2: No external load capacitor required.

#### Circuit reference design and requirements:

The load capacitance of the crystal is subject to the crystal manufacturer's recommendations, usually CL1=CL2.

The CH32V203RB chip is externally connected with a 32M crystal, the chip has a built-in load capacitor, and the external circuit can be saved.

Figure 4-5 Typical circuit of external 8M crystal

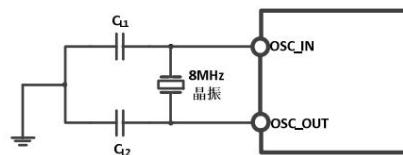


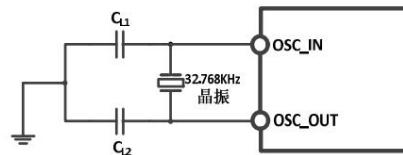
Table 4-12 Low-speed external clock generated using a crystal/ceramic resonator (fLSE=32.768KHz)

symbol	parameter	condition	Min	Typ	Max	Unit		
Recommended Load					5		MΩ	
C	Capacitance for RF Feedback Resistor and Corresponding Crystal String Row impedance RS	RS<70kΩ			15		pF	
I <sub>2</sub>	LSE drive current	VDD = 3.3V		0.35			uA	
gm oscillator transconductance		start up		25.3			uA/V	
tSU(LSE) start-up time		VDD is stable		800			ms	

#### Circuit reference design and requirements:

The load capacitance of the crystal is subject to the crystal manufacturer's recommendation, usually CL1=CL2, and about 12pF is optional.

Figure 4-6 Typical circuit of external 32.768K crystal



Note: The load capacitance CL is calculated by the following formula:  $\bar{C}_L = \frac{CL_1}{CL_1 + CL_2} + C_{stray}$ , where Cstray is the capacitance of the pin and the plate or PCB 2pF, its typical value is between.

#### 4.3.6 Internal Clock Source Characteristics

Table 4-13 Internal High Speed (HSI) RC Oscillator Characteristics

symbol	parameter	condition	Min	Typ	Max	Unit		
FHSI frequency (after calibration)				8			MHz	
DuCyHSI duty cycle			45	50	55		%	
ACCHSI	Accuracy of the HSI oscillator (after calibration)	TA = 0.070° - 1.0 TA = -40.85°	-2.2			1.6	%	
						2.2	%	
tSU(HSI)	HSI oscillator start-up stabilization time			10			us	
IDD(HSI)	HSI Oscillator Power Consumption		120	180	270		uA	

Table 4-14 Internal Low Speed (LSI) RC Oscillator Characteristics

symbol	parameter	condition	Min	Typ	Max	Unit		
FLSI frequency			25		39		60	KHz
		Applicable to V203RBT6	25		32		45	
DuCylSI duty cycle			45		50		55	%
tSU (LSI)	LSI oscillator start-up stabilization time				100			us
IDD(LSI)	LSI oscillator power consumption				0.6			uA

#### 4.3.7 PLL characteristics

Table 4-15 PLL characteristics

symbol	parameter	condition	Min	Typ	Max	Unit		
FPLL_IN	PLL input clock		3		8		25	MHz
		Applicable to V203RBT6	4		8		25	
	PLL input clock duty cycle		40				60	%
FPLL_OUT	PLL multiplied output clock		18				144(1)	MHz
		Applicable to V203RBT6	40				240(1)	
tLOCK	PLL lock time						200	us

Note 1: An appropriate multiplier must be selected to meet the output frequency range.

#### 4.3.8 Wake-up time from low-power mode

Table 4-16-1 Time to wake up from low power consumption mode (1) (using V203x chip)

Symbol	parameter	condition	typical unit	
twosleep	wakes up from sleep mode	Wakeup from stop mode with HSI	1.44	us
twostop	RC clock Wakeup from stop mode (regulator in run mode)	from regulator with HSI RC	22.87	us
	Wake up from stop mode (voltage regulator is in low power mode)	clock Wakeup time from low power mode + HSI RC clock wake-up	75.53	us
tWUSTDBY	wake up from standby mode	LDO stabilization time + HSI RC clock wakeup + code loading time (2)	4.82	ms

Note: 1. The above are measured parameters. 2. The code loading time is based on the current chip configuration. For running area capacity and loading configuration clock size calculations are

Table 4-16-2 Time to wake up from low power consumption mode (1) (using V203RBT6 chip)

Symbol	parameter	Wakeup	typical unit	
twosleep	wakes up from sleep mode	from stop mode (regulator in run mode)	2.6	us
twostop	Wakeup with HSI RC clock Wakeup with HSI RC clock		23.1	us
	Wake up from stop mode (voltage regulator is in low power mode)	Regulator wake-up time from low-power mode+ HSI RC clock wake-up	299	us
tWUSTDBY	wake up from standby mode	LDO stabilization time + HSI RC clock wake-up + code loading time (2) (Example 128K)	5.0	ms

Note: 1. The above are measured parameters. 2. The code loading time is based on the current chip configuration. For running area capacity and loading configuration clock size calculations are

## 4.3.9 Memory Characteristics

Table 4-17 Flash memory features

Symbolic parameters	condition	Min	Typ	Max	Unit		
Fprog operating frequency <sup>(1)</sup>	TA = -40~85 $\mu$ s tprog_page				60	MHz	
page (256 bytes) programming time TA = -40~85 $\mu$ s terase_page page (256 bytes)			2			ms	
erasing time TA = -40~85 $\mu$ s terase_sec sector (4K bytes)	Erase time TA = -40~85 $\mu$ s			16		ms	
				16		ms	
Vprog programming voltage		2.4			3.6	IN	

Note: 1. The operating frequency of flash includes reading, programming, and erasing, and the clock comes from HCLK.

Table 4-18 Flash memory lifespan and data retention period

Symbolic parameters	condition	Min	Typ	Max	Unit		
NEND erase times tRET	TA = 25 $\mu$ s	10K	80K(1)			Second-time	
data retention period		20				Year	

Note: The number of erasing and writing operations measured is not a guarantee.

## 4.3.10 I/O port characteristics

Table 4-19 General I/O static characteristics

symbol	parameter	Condition Min	Typ	Max	Unit		
HIV	Standard I/O pin, input high level voltage		0.41*(VDD 1.8)+1.3			VDD+0.3	IN
	FT IO pin, input high level voltage		0.42*(VDD 1.8)+1			5.5	IN
WILL	Standard I/O pin, input low level voltage		-0.3			0.28*(VDD 1.8)+0.6	IN
	FT IO pin, input low level voltage		-0.3			0.32*(VDD 1.8)+0.55	IN
Vhys	Schmitt trigger voltage hysteresis on standard I/O pins		150				mV
	FT IO Pin Schmitt Trigger Voltage Hysteresis		90				
Ilkg	input leakage current	Standard IO port				1	uA
		FT IO port				3	
RPU	weak pull-up equivalent resistance		30	40		50	k $\Omega$
RPD	weak pull-down equivalent resistance		30	40		50	k $\Omega$
CIO	I/O pin capacitance			5			pF

## Output Drive Current Characteristics

GPIOs (general purpose input/output ports) can sink or source up to  $\pm 8$ mA and sink or source  $\pm 20$ mA (not strictly up to VOL/VOH). In user applications, the total current driven by all IO pins must not exceed the absolute maximum ratings given in Section 4.2:

Table 4-20 Output voltage characteristics

Symbolic parameters	condition	min	max	unit		
VOL outputs low level, 8 pins sink current	TTL port, IIO = +8mA 2.7V < VDD <3.6V		0.4		IN	
VOH outputs high level, 8 pins output current		VDD-0.4				

VOL outputs low level, 8 pins sink current	CMOS port, IIO = +8mA 2.7V < VDD < 3.6V	2.3	0.4	IN	
VOH outputs high level, 8 pins output current					
VOL outputs low level, 8 pins sink current	IIO = +20mA 2.7V < VDD < 3.6V	VDD-1.3	1.3		
VOH outputs high level, 8 pins output current					
VOL outputs low level, 8 pins sink current	IIO = +6mA 2.4V < VDD < 2.7V	VDD-1.3	0.4		
VOH outputs high level, 8 pins output current					

Note: If more than one of the above conditions are met, the pins are driven at the same time, and the total current cannot exceed 4.2 section gives the absolute maximum ratings. in addition to the table. When multiple pins are driven at the same time, the current of the power ground points very large, which will cause a voltage drop and the internal voltage cannot reach the power supply voltage in the table.

Table 4-21 Input and output AC characteristics

MODEx[1:0] configuration	symbol	parameter	condition	min	max	unit
10 ÿ2MHzÿ	Fmax(Io)out	maximum	CL=50pF,VDD=2.7-3.6V		2	MHz
	frequency tf(Io)out	output high to low fall time	CL=50pF,VDD=2.7-3.6V		125	ns
	tr(Io)out	output low to high rise time			125	ns
01 ÿ10MHzÿ	Fmax(Io)out	maximum	CL=50pF,VDD=2.7-3.6V		10	MHz
	frequency tf(Io)out	output high to low fall time	CL=50pF,VDD=2.7-3.6V		25	ns
	tr(Io)out	output low to high rise time			25	ns
11 ÿ50MHzÿ	Fmax(Io)out	maximum frequency	CL=30pF,VDD=2.7-3.6V		50	MHz
	tf(Io)out	output high to low fall time	CL=50pF,VDD=2.7-3.6V		30	MHz
	tr(Io)out	output low to high rise time	CL=30pF,VDD=2.7-3.6V		20	ns
			CL=50pF,VDD=2.7-3.6V		5	ns
			CL=30pF,VDD=2.7-3.6V		8	ns
			CL=50pF,VDD=2.7-3.6V		12	ns
	tEXTI pw	EXTI controller detected external signal pulse width of		10		ns

#### 4.3.11 NRST pin characteristics

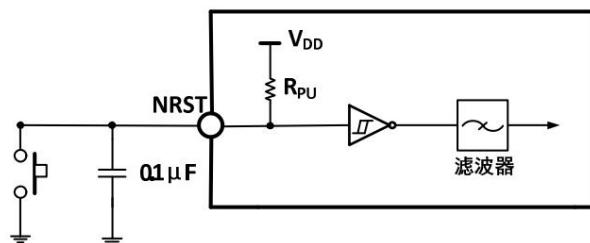
Table 4-22 External reset pin characteristics

symbol	parameter	condition	minimum value	Typical Value	Maximum Unit	
VIL(NRST)	NRST input low level voltage		-0.3	0.28*(VDD-1.8)+0.6V		
VIH(NRST)	NRST input high level voltage		0.41*(VDD-1.8)+1.3	VDD+0.3		IN
V <sub>hys</sub> (NRST)	NRST Schmitt trigger voltage		150			mV
( <sup>1</sup> RPUs)	Weak pull-up equivalent resistance		30	40	50	kÿ
VF(NRST)	NRST input can be filtered pulse width				100	ns
VNF(NRST)	NRST input cannot filter pulse width		300			ns

Note: 1. The pull-up resistor is a real resistor in series with a switchable implementation. The resistance of this PMOS/NMOS switch is very small (approximately accounted for 10%).

Circuit reference design and requirements:

Figure 4-7 Typical circuit of external reset pin



#### 4.3.12 TIM Timer Features

Table 4-23 TIMx features

symbol	parameter	condition	min	max	unit
tres(TIM) timer reference clock			1		tTIMxCLK
	fTIMxCLK = 72MHz		13.9		ns
FEXT	Timer external clock frequency of CH1 to CH4		0	tTIMxCLK/2	MHz
		fTIMxCLK = 72MHz	0	36	MHz
ResTIM timer	resolution			16 bit	
tCOUNTER	16-bit count when internal clock is selected clock cycle		1	65536	tTIMxCLK
		fTIMxCLK = 72MHz	0.0139	910	us
tMAX_COUNT	maximum possible count			65535	tTIMxCLK
		fTIMxCLK = 72MHz		59.6	s

#### 4.3.13 I2C Interface Features

Figure 4-8 I2C bus timing diagram

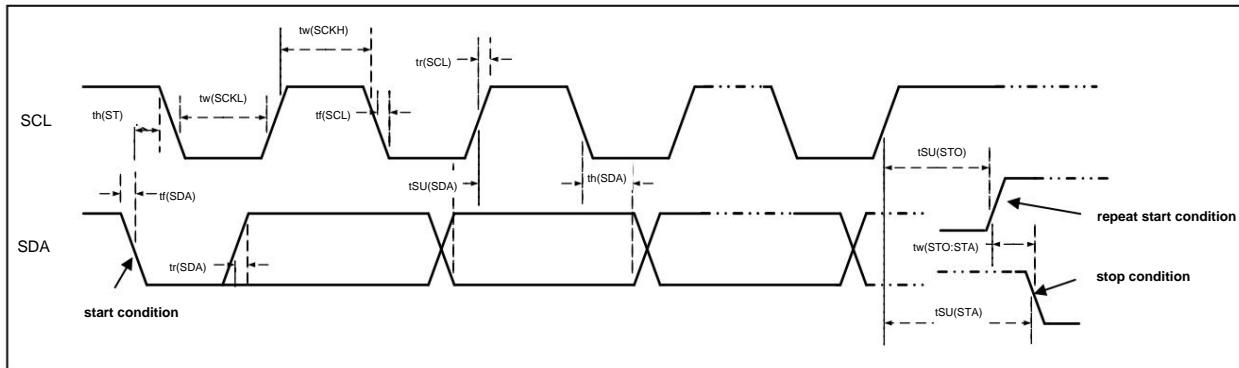


Table 4-24 I2C interface features

symbol	parameter	Standard I2C		Fast I2C		unit
		minimum value	maximum value	minimum value	maximum value	
tw(SCKL)	SCL clock low time	4.7		1.2		us
tw(SCKH)	SCL clock high time	4.0		0.6		us
tSU(SDA)	SDA data setup time	250		100		ns
th(SDA)	SDA data hold time	0		0	900	ns
tr(SDA)/tw(SCL)	SDA and SCL rise time tf(SDA)/		1000	20		ns
tf(SCL)	SDA and SCL fall time th(STA) start		300			ns
condition hold time tSU(STA)	repeat start	4.0		0.6		us
condition setup time		4.7		0.6		us

tSU(STO) stop condition setup time	4.0		0.6		us
tw(STO:STA) Stop condition to start condition time (bus free) 4.7			1.2		us
C <sub>b</sub> capacitive load per bus		400		400	pF

#### 4.3.14 SPI Interface Features

Figure 4-9 Timing Diagram of SPI Master Mode

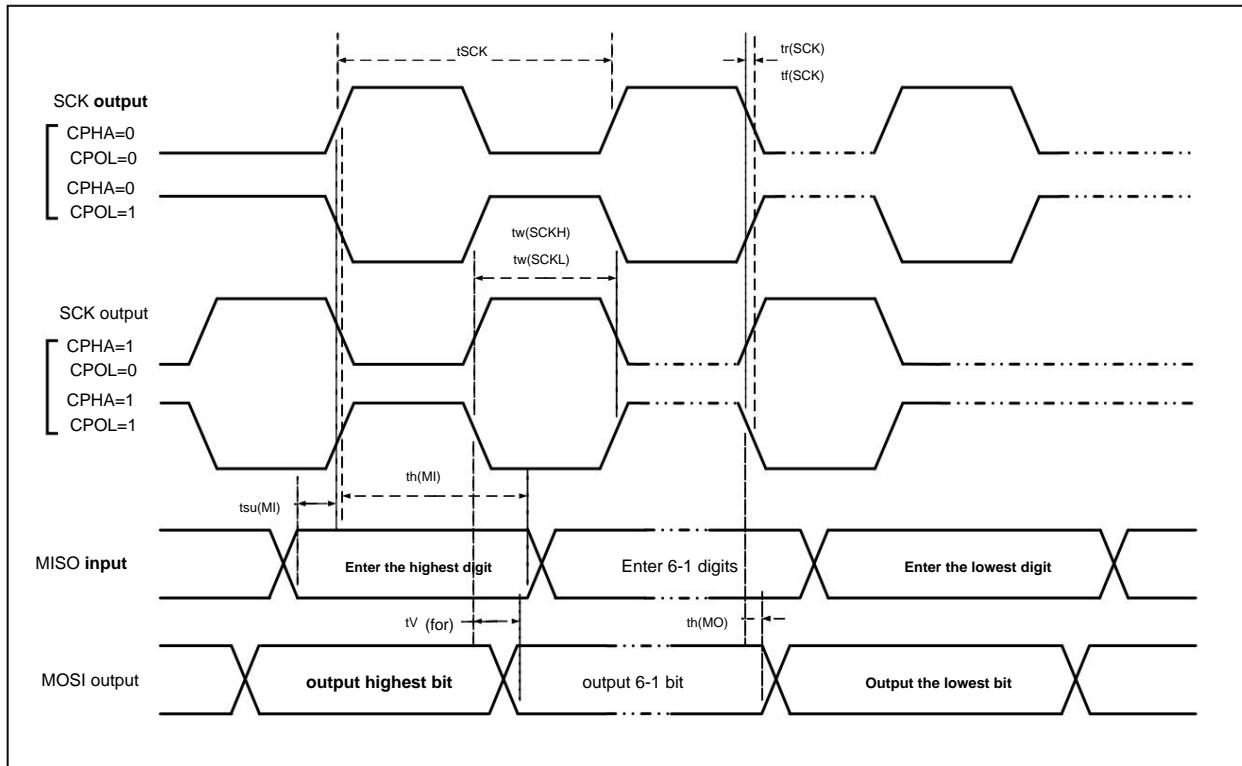


Figure 4-10 SPI slave mode timing diagram (CPHA=0)

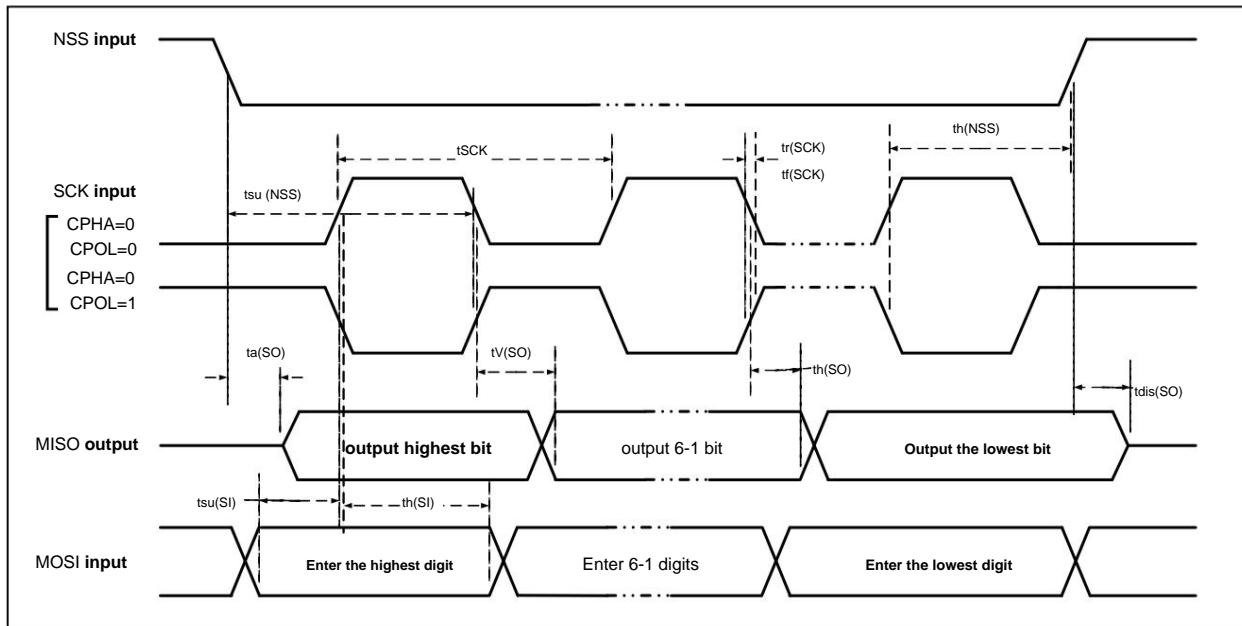


Figure 4-11 SPI slave mode timing diagram (CPHA=1)

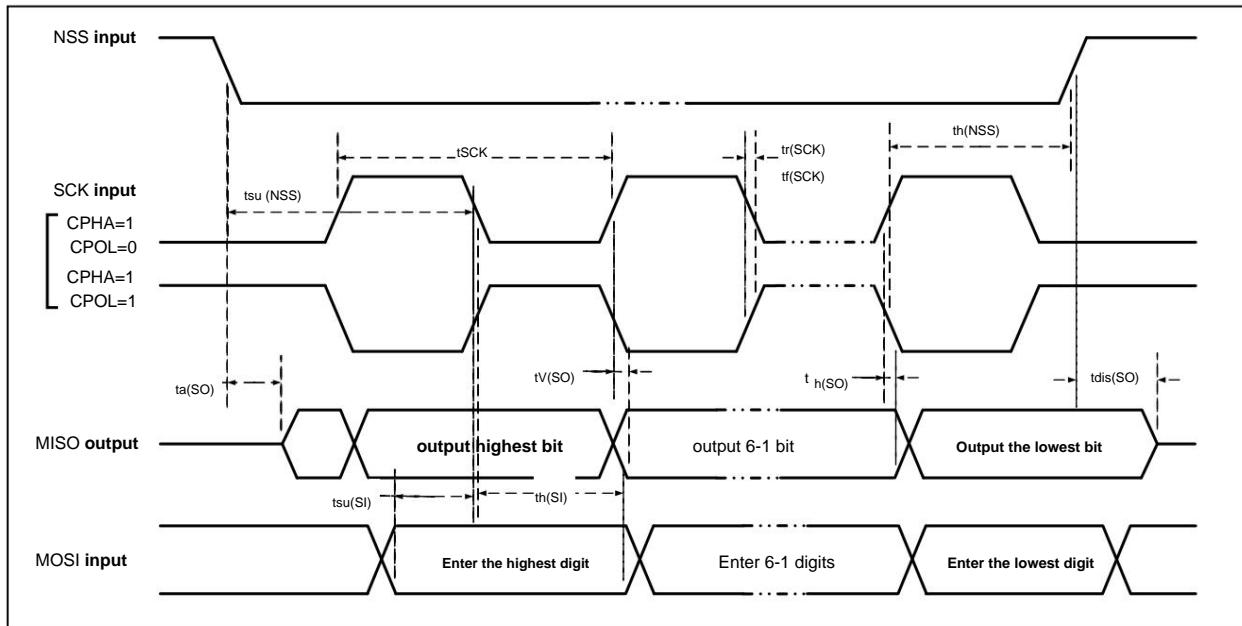


Table 4-25 SPI interface features

symbol	parameter	condition	min	max	unit
fSCK/tSCK	SPI clock frequency	Master		36	MHz
		Mode		36	MHz
Slave Mode tr(SCK)/tf(SCK)	SPI Clock Rise and Fall Time Load Capacitance: C = 30pF			20	ns
tsu(NSS)	NSS establishment time	Slave	2tPCLK		ns
th(NSS)	NSS hold time	mode	2tPCLK		ns
tw(SCKH)/tw(SCKL)	SCK high and low time	Slave mode Master mode, fPCLK = 36MHz, prescaler Coefficient	40	60	ns
tsu(MI)	Data input setup time	= 4 Master	5		ns
		Mode	5		ns
th(MI)	Data input hold time	Slave	5		ns
		Mode	4		ns
ta(SO)	data output access time tdis(SO) data	Master Mode Slave Mode, fPCLK	0	1tPCLK	ns
output disable time		= 20MHz	0	10	ns
tV(SO)	Data output effective time	Slave Mode Slave Mode (after Enable Edge)		25	ns
		Master Mode (after Enable Edge)		5	ns
th(SO)	Data output hold time	Slave Mode (after Enable Edge)	15		ns
		Master Mode (after Enable Edge )	0		ns

#### 4.3.15 USB Interface Features

Table 4-26 USB module features

symbol	parameter	condition	min	max	unit
vdd	USB operating voltage		3.0	3.6	IN
VSE	Single-Ended Receiver Threshold	VDD = 3.3V	1.2	1.9	IN
VOL	static output low level			0.3	IN
VOH	static output high level		2.8	3.6	IN

VHSSQ High Speed Suppression Information Detection Threshold		100	150	mV
VHSDSC High Speed Disconnect Detection Threshold		500	625	mV
VHSOI High Speed Idle Level		-10	10	mV
VHSOH high speed data high level		360	440	mV
VHSOL High Speed Data Low		-10	10	mV

#### 4.3.16 12-bit ADC characteristics

Table 4-27 ADC characteristics

symbol	parameter	condition	Min	Typ	Max	Unit		
VDDA supply voltage			2.4			3.6	IN	
VREF+ positive reference voltage		VREF+ cannot be higher than VDDA	2.4			VDDA	IN	
IVREF reference current					160	220	uA	
IDDA supply current					480	530	uA	
fADC	ADC clock frequency					14	MHz	
tS sampling rate fTRIG			0.05				MHz	
external trigger frequency						16	1/fADC	
VAIN conversion voltage range			0			VREF+	IN	
RAIN external input impedance						50	k $\ddot{\text{v}}$	
RADC sampling switch resistance					0.6		k $\ddot{\text{v}}$	
CADC internal sampling and holding capacitor					8		pF	
tCAL calibration time tlat					100		1/fADC	
injection trigger conversion delay tlatr						2	1/fADC	
regular trigger conversion delay ts sampling						2	1/fADC	
time tSTAB power-on time			1.5			239.5	1/fADC	
tCONV total conversion time							us	
(including sampling time)			14			252	1/fADC	

Note: The above are guaranteed by design parameters.

Formula: Max RAIN

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln 2^{N+1}} - R_{ADC}$$

The above formula is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N=12 (indicating 12-bit resolution).

Table 4-28 Maximum RAIN at fADC = 14MHz

TS (period)	tS (us)	Maximum RAIN(k $\ddot{\text{v}}$ )
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	invalid
239.5	17.1	invalid

Table 4-29 ADC error

symbol	parameter	condition	Min	Typ	Max	Unit		
EO offset error	fPCLK2 = 56 MHz,fADC = 14 MHz,RAIN < 10 k $\Omega$ ,VDDA = 3.3V				$\pm 2$			
ED Differential Nonlinear Error					$\pm 0.5$	$\pm 3$ LSB		
EL integral nonlinearity error					$\pm 1$	$\pm 4$		

C<sub>p</sub> represents the parasitic capacitance (about 5pF) on the PCB and the pad, which may be related to the quality of the pad and PCB layout. Larger C<sub>p</sub> values will

To reduce the conversion accuracy, the solution is to reduce the fADC value.

Figure 4-12 ADC typical connection diagram

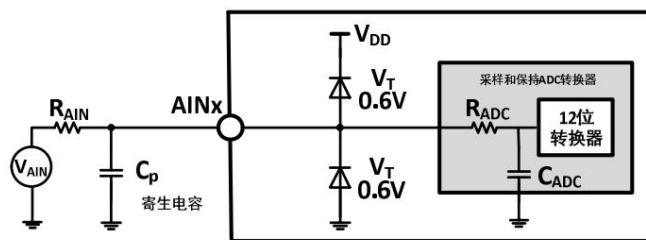
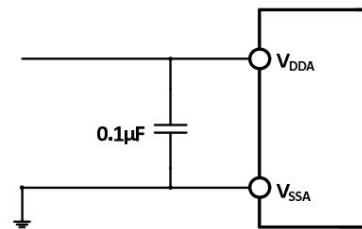


Figure 4-13 Analog power supply and decoupling circuit reference



#### 4.3.17 Temperature sensor characteristics

Table 4-30 Temperature sensor characteristics

Symbolic parameters		condition	Min	Typ	Max	Unit		
RTS temperature sensor measuring range			-40			85	$^{\circ}\text{C}$	
Measurement error of ATSC temperature sensor					$\pm 12$			$^{\circ}\text{C}$
Avg_Slope Average slope (negative temperature coefficient)			3.8	4.3		4.8 mV/ $^{\circ}\text{C}$		
Voltage of V25 at 25°C			1.34	1.40		1.46		IN
TS_temp When reading temperature, ADC sampling time fADC = 14MHz						17.1		us

#### 4.3.18 OPA features

Table 4-31 OPA features

symbol	parameter	condition	Min	Typ	Max	Unit		
VDDA supply voltage			2.4	3.3	3.6			IN
CMIR common mode input voltage			0			VDDA-0.9		IN
VIOFFSET input offset voltage				2.5		8		mV
ILOAD drive current					600			uA
IDDOPAMP Current Consumption	(1) Common Mode	no load, static mode		195				uA
PSRR Rejection Ratio Power		@ 1KHz		96				dB
OF Supply Rejection Ratio Open Loop Gain	(1) Open Loop Gain	CLOAD=5pF		86				dB
				136				dB

<sup>(1)</sup> GBW	Unity Gain Bandwidth	CLOAD=5pF		19		MHz
<sup>(1)</sup> PM	Phase Margin	CLOAD=5pF		93		
<sup>(1)</sup> SR	Slew Rate	CLOAD=5pF P		8		V/us
tWAKU <sup>(1)</sup> shutdown	to wake-up setup time, 0.1% input VDDA/2, CLOAD=5pF, RLOAD=4k $\Omega$	RLOAD resistive load			368	ns
			4			k $\mu$
CLOAD capacitive load					50	pF
<sup>(2)</sup> VOHSAT	High saturation output voltage	RLOAD=4k $\Omega$ , input VDDA	VDDA-45			mV
		RLOAD=20k $\Omega$ , input VDDA VDDA-10				
<sup>(2)</sup> WANTED	Low saturation output voltage	RLOAD=4k $\Omega$ , input 0			0.5	mV
		RLOAD=20k $\Omega$ , input 0			0.5	
EN(1) equivalent input voltage noise		RLOAD=4k $\Omega$ , @1KHz		83		$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
		RLOAD=4k $\Omega$ , @10KHz		42		

Note: 1. The source simulation is not measured. 2. The load current will limit the saturated output voltage.

## Chapter 5 Packaging and Ordering Information

## Chip

Package Order Model	Package Type	Plastic Body Width	Lead Pitch	Package Description	Shipping tray
CH32V203F6P6 TSSOP20	4.4*6.5mm 0.65mm thin	and small 20-pin	patch plastic tube		
CH32V203F8P6 TSSOP20	4.4*6.5mm 0.65mm thin	and small 20-pin	patch plastic tube		
CH32V203F8U6 QFN20X3	3*3mm	0.4mm square	leadless 20-pin pallet		
CH32V203G6U6 QFN28X4	4*4mm	0.4mm	Square Leadless 28 Foot Tray		
CH32V203G8R6 QSOP28	3.9*9.9mm 0.635mm			28-pin SMD plastic tube	
CH32V203K6T6 LQFP32	7*7mm	0.8mm		LQFP32 (7*7) patch tray	
CH32V203K8T6 LQFP32	7*7mm	0.8mm		LQFP32 (7*7) patch tray	
CH32V203C6T6 LQFP48	7*7mm	0.5mm		LQFP48 (7*7) patch tray	
CH32V203C8T6 LQFP48	7*7mm	0.5mm		LQFP48 (7*7) patch tray	
CH32V203C8U6 QFN48X7	7*7mm	0.5mm square	leadless 48-pin pallet		
CH32V203RBT6 LQFP64M	10*10mm	0.5mm	LQFP64M (10*10)	patch tray	

Note: 1. QFP/QFN generally defaults to trays, and the specific model can be confirmed with the packaging factory.

2. Pallet size: The size of the pallet is generally a uniform size, 322.6\*135.9\*7.62, and the size of the limit hole is different for different packaging types.

There are differences between different packaging factories, please confirm with the manufacturer for details.

Explanation: The unit of dimension is mm (millimeter), the distance between the centers of the pins is always the nominal value, there is no error, other than that, the dimensional error is not Greater than  $\pm 0.2\text{mm}$  or  $\pm 10\%$ , whichever is greater.

Figure 5-1 TSSOP20 package

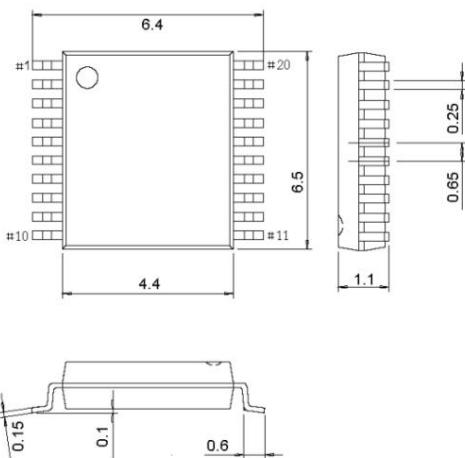


Figure 5-2 QFN20X3 package

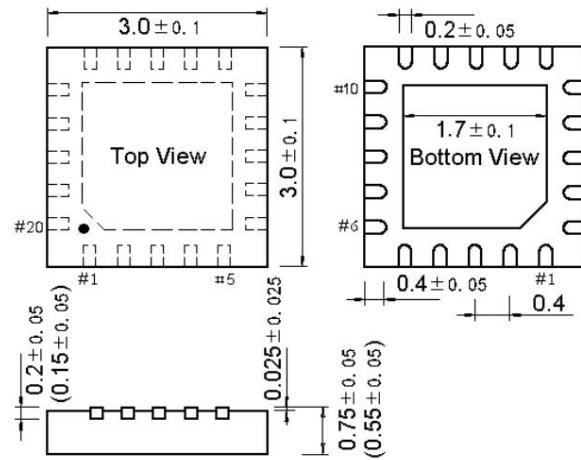


Figure 5-3 QFN28X4 package

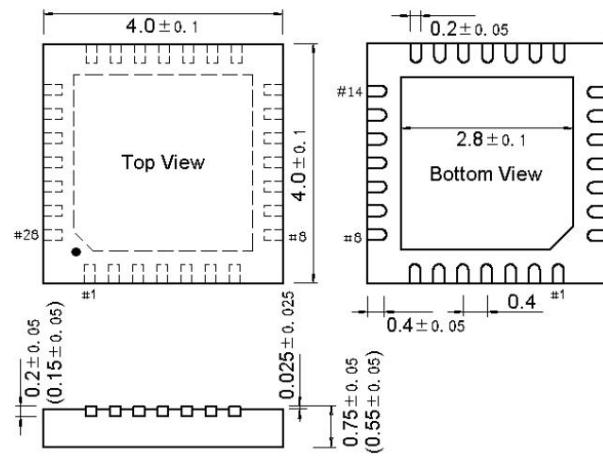


Figure 5-4 QFN48X7 package

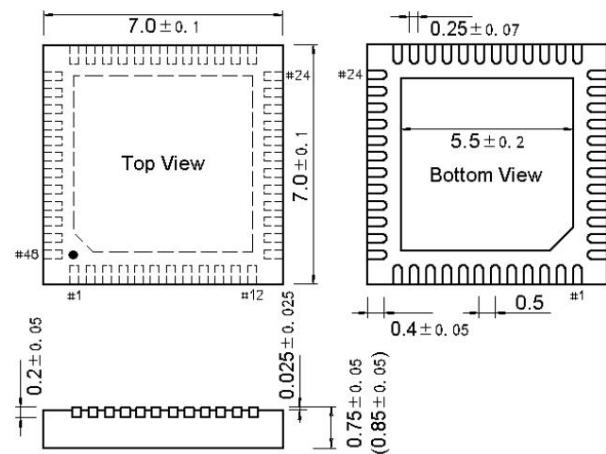


Figure 5-5 LQFP32 package

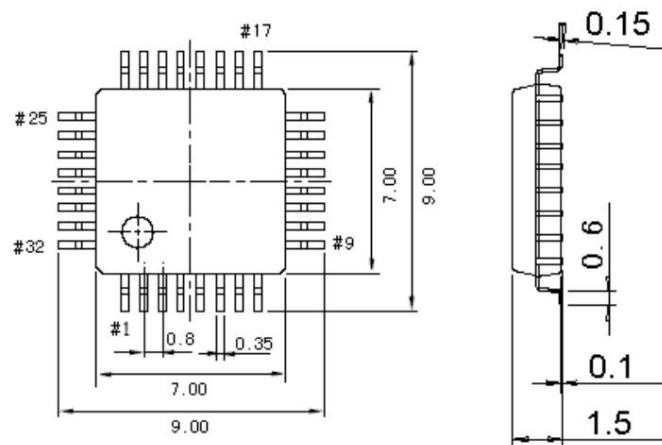


Figure 5-6 LQFP48 package

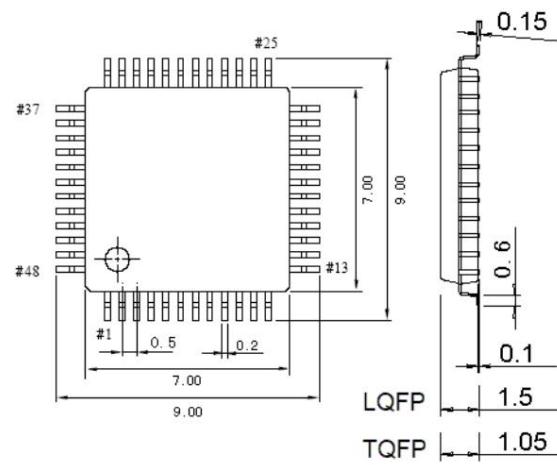


Figure 5-7 LQFP64M package

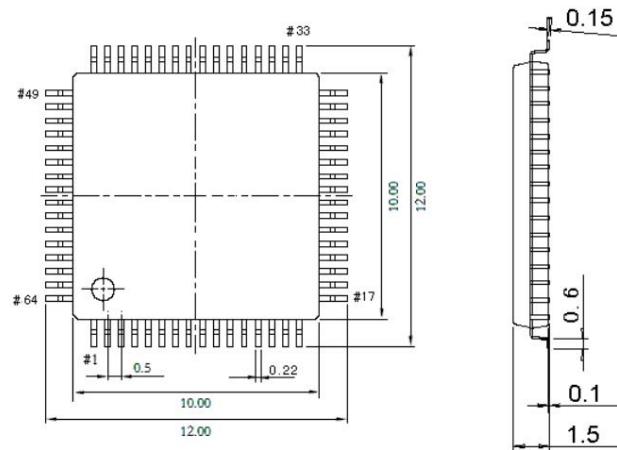
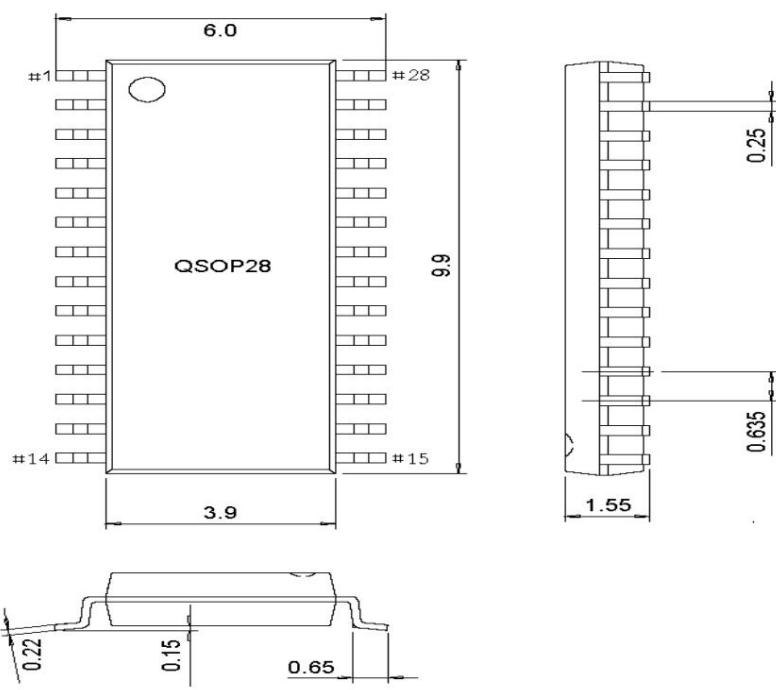


Figure 5-8 QSOP28 package



### Series Product Naming Rules

