Andrew Friedman
Lab 1 Report
ECE 2031 CS
26 May 2023
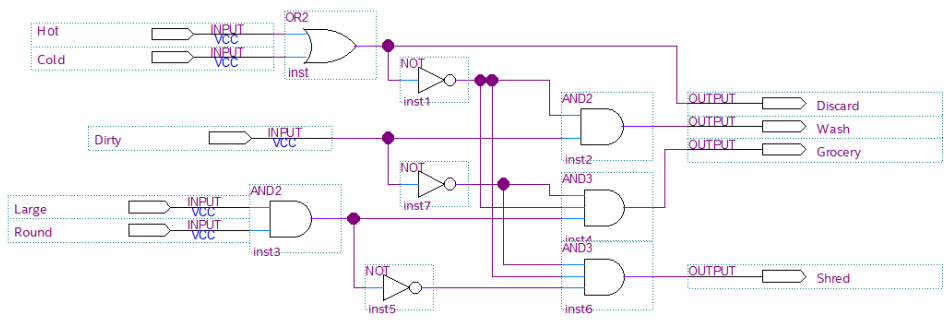
	TITLE	Cabbage Sorting			
	COMPANY	Georgia Tech			
	DESIGNER	Andrew Friedman			
	NUMBER	1.00		REV	A
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Figure 1. Schematic design for a cabbage sorting system implemented on a DE10-Standard board, using slide switches for inputs and LEDs as outputs.
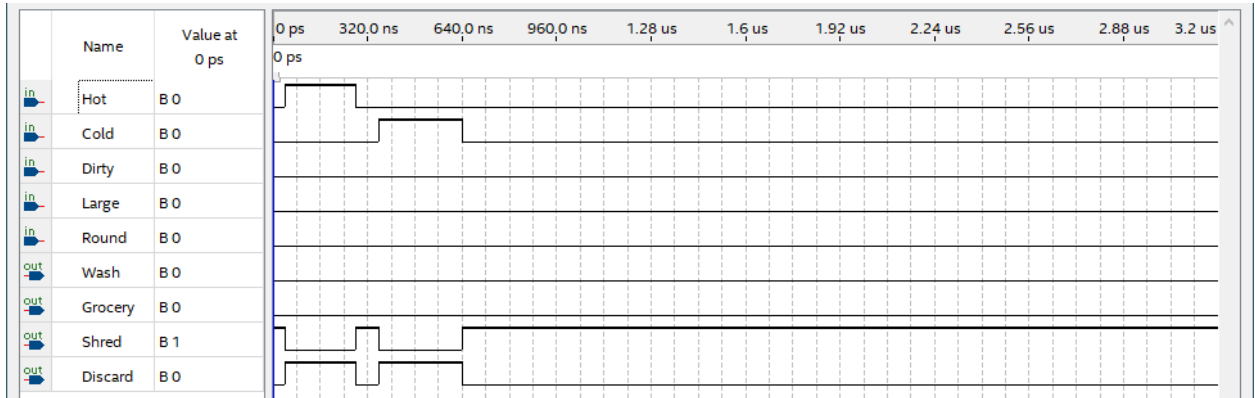

Figure 2. The waveform editor result captures the functional simulation outcomes, with unique test cases of high signals on "Hot" and "Cold" implemented independently, thereby elucidating the behavior of "Discard" output for these instances and the "Shred" baseline when all inputs are "zero."
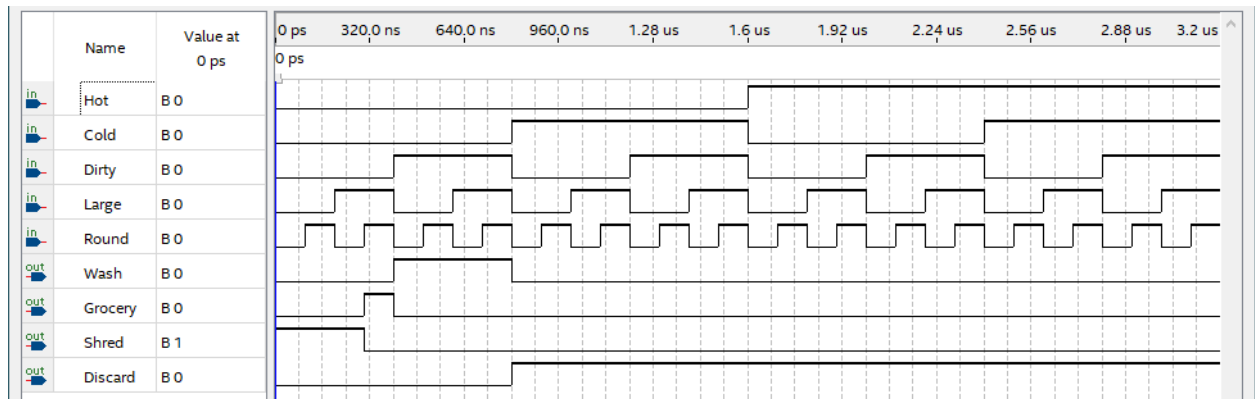
Figure 3. The comprehensive input variation simulation presents a snapshot of the simulation running all potential test cases, employing systematically diminishing signal periods within a 3.2 µs timeframe to validate output assertions based on diverse input combinations.

Figure 4. The schematic with assigned FPGA pins illustrates the application of the FPGA pin assignments following the design's functional requirements.