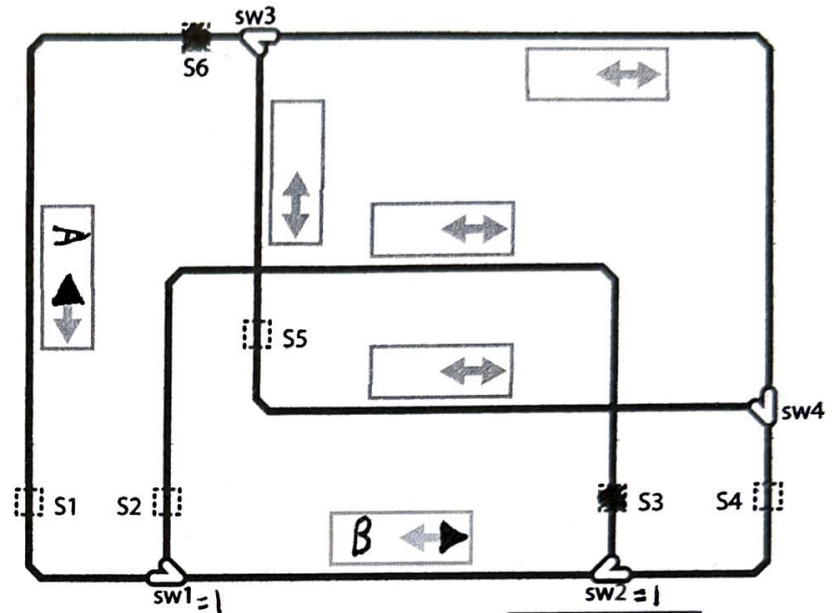


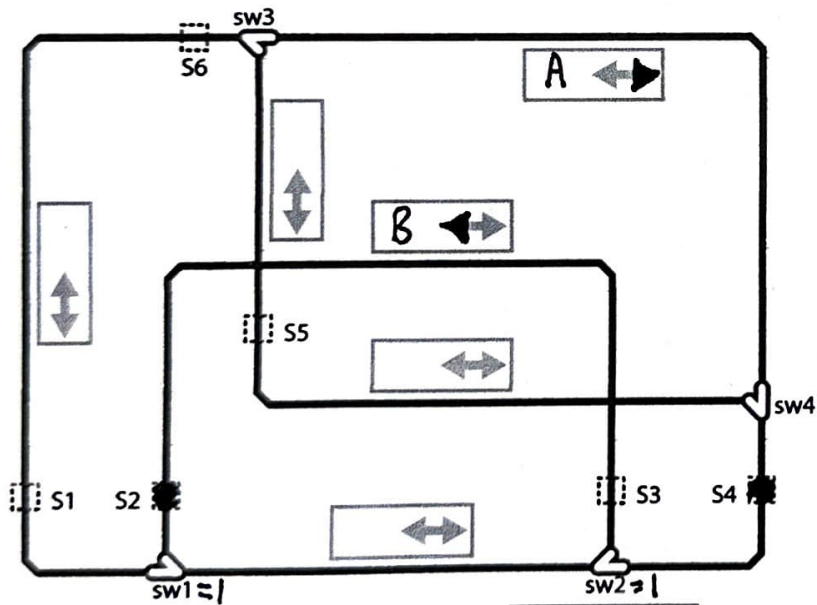
State: *init*

Input	Next State
S2	Ainit Bdown
S6	Astop Binit
S2.S6	Astop Bdown



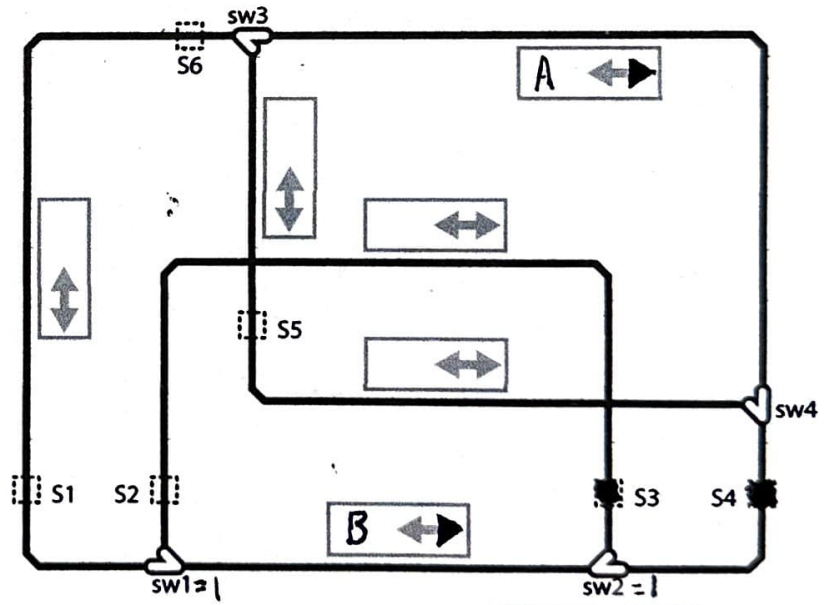
State: *Ainit Bdown*

Input	Next State
S3	init
S6	Astop Bdown
S3.S6	Astop Binit



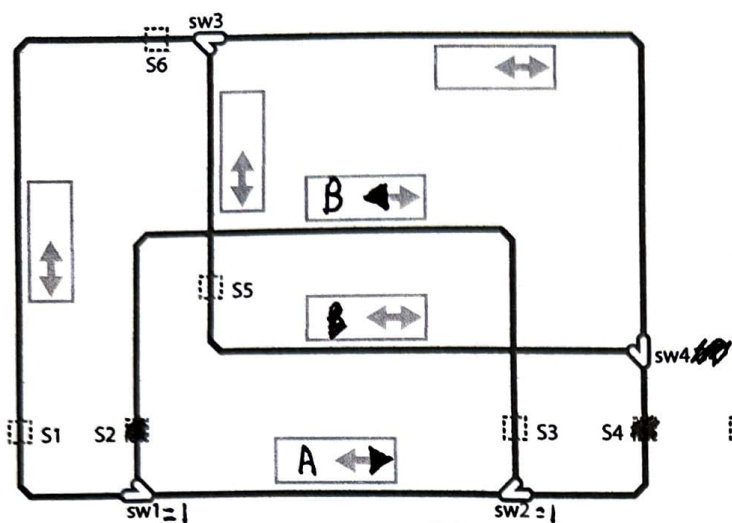
State: *Astop Binit*

Input	Next State
S2	Astop Bdown
S4	Astop Binit
S2.S4	A.B



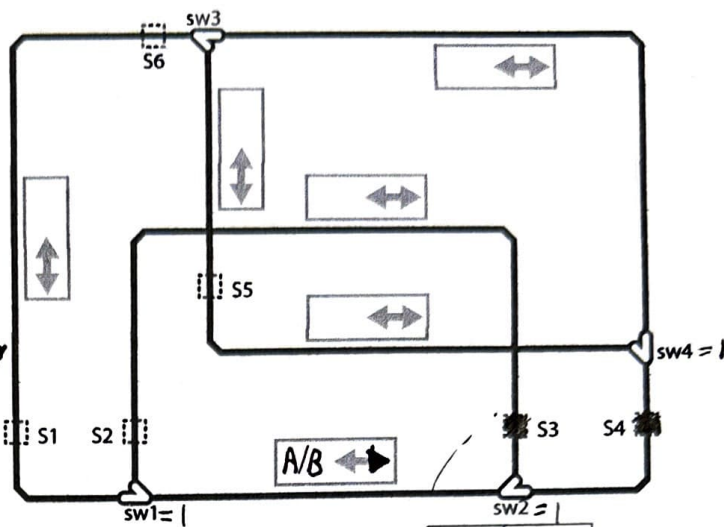
State: *Astop Bdown*

Input	Next State
S3	init
S4	A.B
S3.S4	Astop Binit



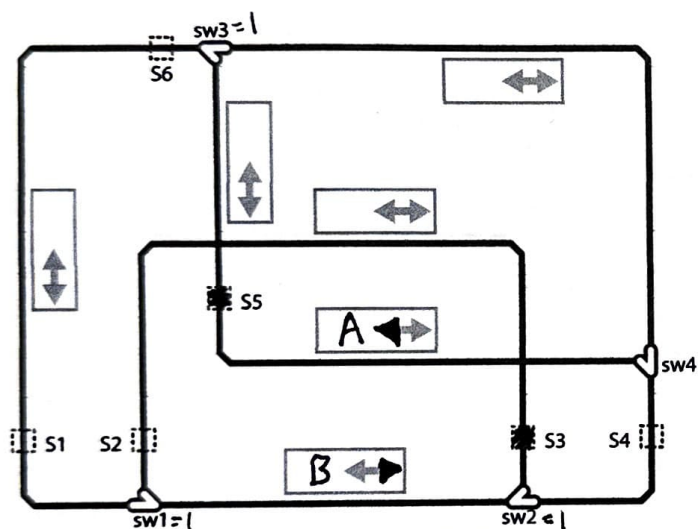
State: A bot B init

Input	Next State
S2	A.B
S3.S4	A left B init
S2.S3	A left B down



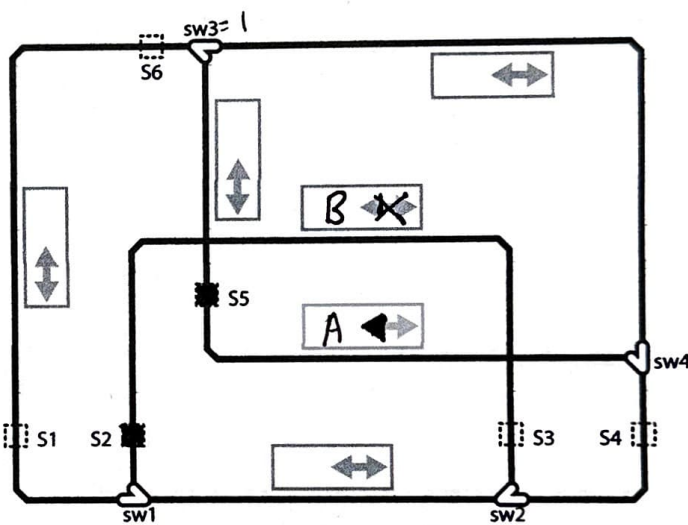
State: A.B

Input	Next State
S3	A bot B init
S4	A left B down
S3.S4	A left B init



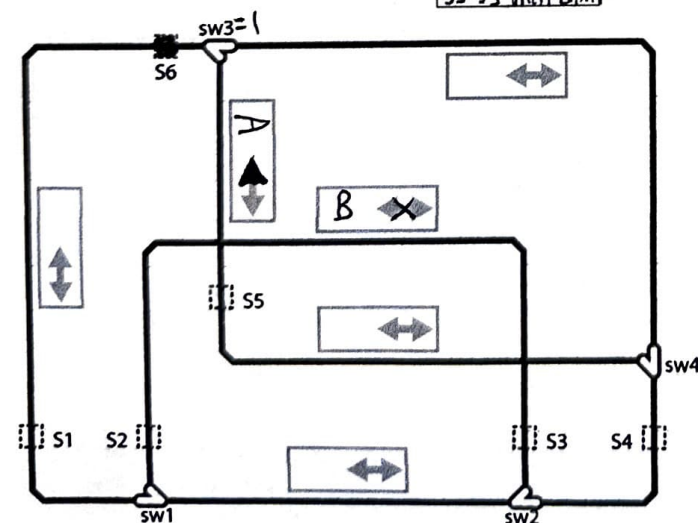
State: A mid B down

Input	Next State
S3	A left B init
S5	A left B down
S3.S5	A left B init



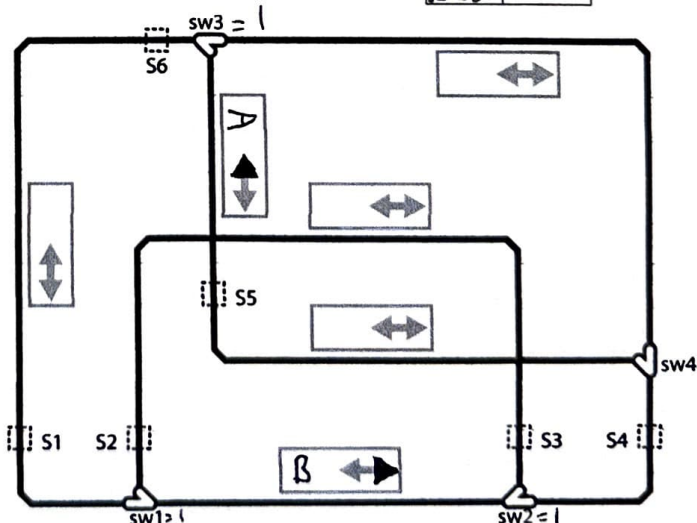
State: A mid B init

Input	Next State
S2	—
S5	A left B init
S2.S5	—



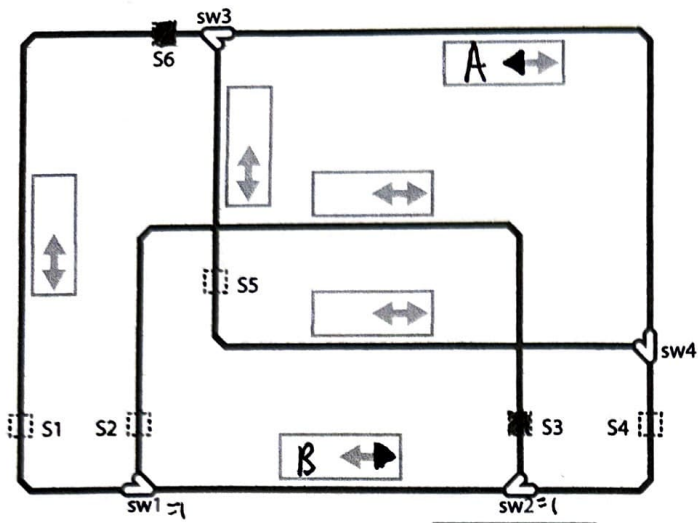
State: A left B init

Input	Next State
S2	—
S6	init
S2.S6	—



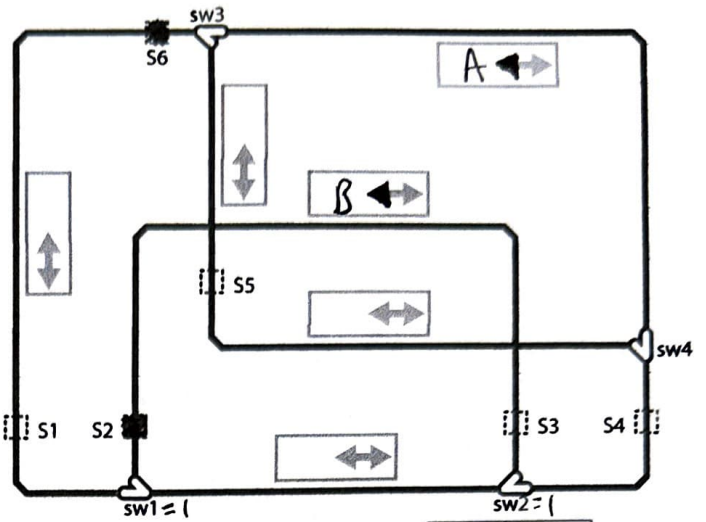
State: A left B down

Input	Next State
S3	A left B init
S6	A left B down
S3.S6	init



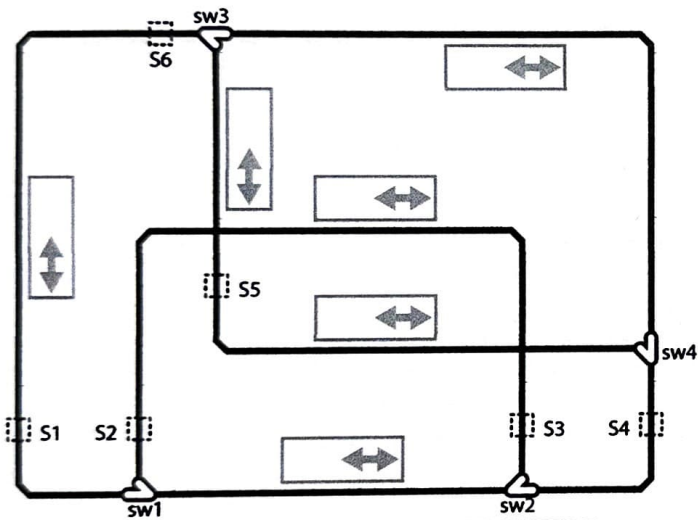
State: A top 2 B down

Input	Next State
S3	A top 2 B init
S6	A init B down
S3:S6	init



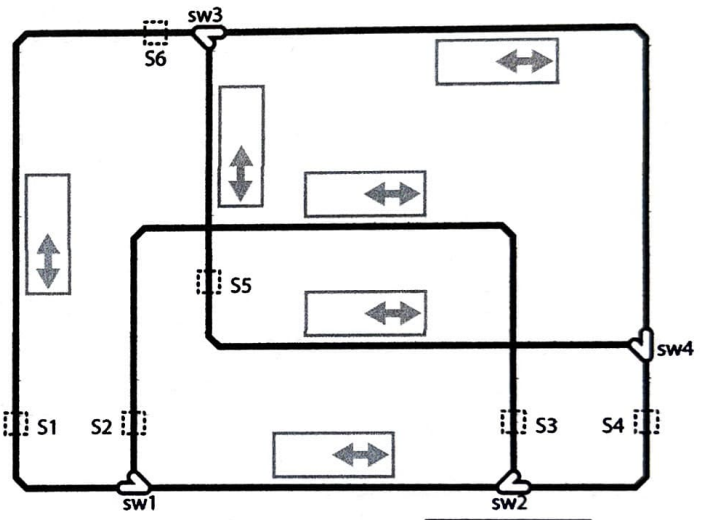
State: A top 2 B init

Input	Next State
S2	A top 2 B down
S6	init
S2:S6	A init B down



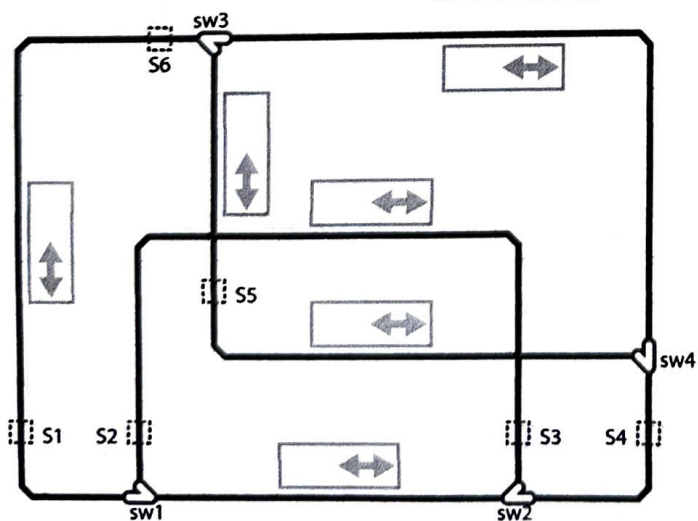
State:

Input	Next State



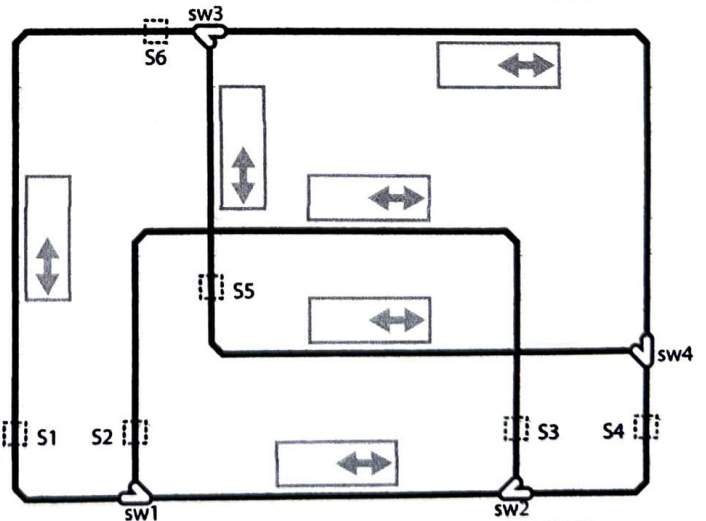
State:

Input	Next State



State:

Input	Next State



State:

Input	Next State

Outputs	States							
	init	A _{left} B _{down}	A _{top} B _{down}	A _{top} B _{init}	A _{bot} B _{init}	A·B	A _{mid} B _{down}	A _{mid} B _{init}
Sw1	1	1	1	1	1	1	1	0
Sw2	1	1	1	1	1	1	1	0
Sw3	0	0	0	0	0	0	1	1
Sw4	0	0	0	0	0	1	0	0
DA[1..0]	01	01	01	01	10	10	10	10
DB[1..0]	01	01	01	01	01	01	01	00

Outputs	States							
	A _{left} B _{init}	A _{left} B _{down}	A _{top} B _{down}	A _{top} B _{init}				
Sw1	0	1	1	1				
Sw2	0	1	1	1				
Sw3	1	1	0	0				
Sw4	0	0	0	0				
DA[1..0]	10	10	10	10				
DB[1..0]	00	01	01	01				

Outputs	States							
Sw1								
Sw2								
Sw3								
Sw4								
DA[1..0]								
DB[1..0]								