Solving Abrupt Silicon PN Junction Question

1. Calculate V_{bi}.
2. Look up D_p on the diffusion coefficient chart. 3
3. Calculate the diffusion length: $L_p = \sqrt{D_p\tau_p}$ (for p^+n) - or - $L_n = \sqrt{D_n\tau_n}$ (for pn^+)
4. If: $L_p > x_p$ (for p^+n) - or - $L_n > x_n$ (for pn^+), the diode is short-base.

Bipolar Junction Transistor

$\beta_F = \frac{\alpha_F}{1-\alpha_F}$; $\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}}$ Gain

$\alpha_F = \gamma_F\alpha_T$; $\alpha_{dc} = \gamma\alpha_T$ Base Transport Factor (BTF)

$\alpha_R = \gamma_R\alpha_T$

$\alpha_{T(npn)} = \frac{I_{Cn}}{I_{En}}$; $\alpha_{T(pnp)} = \frac{I_{Cp}}{I_{EP}}$ BTF (≈ 0.999)

$\alpha_T = 1 - \frac{x_B^2}{2D_n\tau_n} = 1 - \frac{x_B^2}{2Ln^2}$ BTF (D_n. Fig 3,5)

$I_{pE} = \frac{-qA_E n_i^2 D_p}{N_{dE}x_E}\exp\left(\frac{qV_{BE}}{k_BT} - 1\right)$ Short Emitter $L_{pE} = \sqrt{D_{pE}\tau_n} > x_E$

$I_{pE} = \frac{-qA_E n_i^2 D_p}{N_{dE}L_p}\exp\left(\frac{qV_{BE}}{k_BT} - 1\right)$ Long Emitter $L_{pE} = \sqrt{D_{pE}\tau_n} < x_E$

$\gamma_F = \left[1 + \frac{x_B N_{aB} D_{pE}}{x_E N_{dE} D_{nB}}\right]^{-1}$ Short Emitter Forward and Reverse Emitter Injection (REI) Efficiency (γ_R swap roles, E & C)

$\gamma_R = \left[1 + \frac{x_B N_{aB} D_{pC}}{x_E N_{dC} D_{nB}}\right]^{-1}$

$\gamma_F = \left[1 + \frac{x_B N_{aB} D_{pE}}{L_{PE} N_{dE} D_{nB}}\right]^{-1}$ Long Emitter Forward and (REI) Efficiency (for γ_R swap roles of E & C)

$\gamma_R = \left[1 + \frac{x_B N_{aB} D_{pC}}{L_{PC} N_{dC} D_{nB}}\right]^{-1}$

$\gamma_{(npn)} = \frac{I_{En}}{I_E} = \frac{|I_{En}|}{|I_{En}| + |I_{Ep}|}$ Emitter injection Efficiency

$\gamma_{(pnp)} = \frac{I_{Ep}}{I_E} = \frac{|I_{Ep}|}{|I_{En}| + |I_{Ep}|}$

$I_E = I_{Ep} + I_{En}$ $I_C = I_{Cp} + I_{Cn}$ $I_B = \frac{I_C - I_{CE0}}{\beta_{dc}}$

$I_C = \alpha_{dc}I_E + I_{CB0}$ $I_C = \beta I_B + I_{CE0}$ $I_{Cn} \approx I_{BC0}$

$I_{Cn} \approx I_{BC0}$ Collector Reverse Saturation Current

$I_{Cn} \approx I_{BC0}$ Emitter-Collector Saturation Current

Electron Current Density (ECD) - constant base doping

$J_n = \frac{qD_n n_i^2}{x_B N_{aB}}\left[\exp\left(\frac{qV_{BC}}{k_BT}\right) - \exp\left(\frac{qV_{BE}}{k_BT}\right)\right]$ (A/cm^2)

ECD - non-constant base doping (A/cm^2)

$J_n = J_0\left[\exp\left(\frac{qV_{BC}}{k_BT}\right) - \exp\left(\frac{qV_{BE}}{k_BT}\right)\right]$

$J_0 = \frac{q^2 n_i^2 \tilde{D}_n}{Q_B}$, $\tilde{D}_n = \text{avg}(D_n)$

Collector Current Density (under active bias)

$J_C \approx J_0\exp\left(\frac{qV_{BE}}{k_BT}\right)$

Recombination of excess minority carriers in the base

$I_{rB} = \frac{qA_g n_i^2 x_B}{2N_{aB}\tau_n}\left[\exp\left(\frac{qV_{BE}}{k_BT}\right) - 1\right]$

Collector-Emitter Breakdown Voltage in terms of the Collector-Base Breakdown. Note that $m \approx 4$

$BV_{CE0} = \frac{BV_{CB0}}{\beta^{1/m}}$

Finding β Of a BJT

1. Look-up D_{pE} amd D_{pC} on chart
2. Find $L_{pE} = \sqrt{D_{pE}\tau_{pE}}$ and $L_{pC} = \sqrt{D_{pC}\tau_{pC}}$
3. Check if emitter is long or short $L_{pE} > x_B \rightarrow$ long emitter or $L_{pE} < x_B \rightarrow$ short emitter.
4. Find γ_F, (Short Emitter Forward Efficiency)
5. Find α_T (Base Transport Factor)
6. Find α_F (Base Transport Factor)
7. Find β_F (Current Gain)

Designing an Prototype NPN Structure for an Amplifier

1. Assume these doping levels: $N_{dC} = 10^{16}\text{cm}^{-3}$ and $N_{aB} = 5\times10^{16}\text{cm}^{-3}$
2. Calculate $V_{bi} = \frac{k_BT}{q}\ln\left[\frac{N_d N_a}{n_i^2}\right]$
3. Use V_a, desired punch through voltage. $x_B = \left(\frac{N_{aB}}{N_{dC}}\right)^{-1}\left[\frac{2\epsilon_s}{q}\left(\frac{1}{N_{aB}} + \frac{1}{N_{dC}}\right)(V_A - V_{bi})\right]^{1/2}$
4. Calculate (shown as a design parameter) $x_{p0} = \left(\frac{N_{aB}}{N_{dC}}\right)^{-1}\left[\frac{2\epsilon_s}{q}\left(\frac{1}{N_{aB}} + \frac{1}{N_{dC}}\right)(V_{bi})\right]^{1/2}$
5. Calculate $\alpha_T = 1 - \frac{x_B^2}{2D_n\tau_n}$ use hole curve ($D_n = 23\text{cm}^2s^{-1}$) for doping levels above.
6. With these doping levels $\alpha_t \cong 1$. Since $\alpha_T \cong 1$, assume $\alpha_F = \gamma_F$.
7. Find the ratio $= \frac{N_{dE}}{D_{pE}} = \underbrace{\left(\frac{x_B N_{aB}}{x_E D_{nB}}\right)\left(\frac{1}{\gamma_F} - 1\right)}_{ratio}$
8. Using $D_{pE} = \frac{N_{dE}}{ratio}$, find a good value for N_{dE} that allows you to look up D_{pE} on the diffusion chart. Use the curve for holes.

Ebers-Moll Equations

$I_E = I_F - \alpha_R I_R$ Emitter Current

$I_C = \alpha_F I_F - I_R$ Collector Current

$I_B = I_E - I_C$

$I_B = (1-\alpha_F)I_F + (1-\alpha_R)I_R$ Base Current

$I_{F0} = qA\left[\frac{D_E n_{E0}}{L_e} + \frac{D_B p_{B0}}{W}\right]$ Forward Coefficient

$I_F = I_{F0}\left[e^{(eV_{eB}/k_BT)} - 1\right]$ For Curr Component

$I_{R0} = qA\left[\frac{D_E N_{c0}}{L_C} + \frac{D_B p_{B0}}{W}\right]$ Reverse Coefficient

$I_R = I_{R0}\left[e^{(qV_{cB}/k_BT)} - 1\right]$ Rev Cur Component

$\alpha_F I_{F0} = \alpha_R I_{R0} = I_S$

$\frac{I_{F0}}{I_{R0}} = \frac{\alpha_R}{\alpha_F}$ reciprocity Relation.

$\beta_f = \frac{\alpha_F}{1-\alpha_F}$ Normal Forward β

$\alpha_R I_R = \frac{qAD_B p_{B0}}{W}\left[e^{(qV_{cB}/k_BT)-1}\right]$ Ebers-Moll Eqns

$\alpha_R I_R = \frac{qAD_B p_{B0}}{W}\left[e^{(qV_{cB}/k_BT)-1}\right]$ Vol III - 47.

Transit Time and Frequency Response

$\tau_1 = r_e C_{jE}$ Emitter-Base Capacitance Charging Time

$\tau_2 = r_C C_{jC}$ Collector Capacitance Charging Time

$\tau_B = \frac{x_B^2}{2D_{nB}}$ Base Transit Time

$\tau_C = \frac{x_{dc}}{v_{sat}}$ Collector Depletion Region Transit Time (x_{dc}:Depletion region width of collector) (v_{sat}: Saturation velocity, $\approx 10^7$ m/s)

$\tau_{EC} = \tau_1 + \tau_2 + \tau_B + \tau_C$ $\tau_{EC} = \tau_C + \tau_B + \tau_E$

Emitter to Collector Transit Time. $f_T = \frac{1}{2\pi\tau_{EC}}$ Cut-off Frequency.

Amplification: For amplifying BJTs, the thickness and resistivity of the collector are both large. Th is results in an increased breakdown voltage and reduces the early effect.

Switching: For switching BJT's, saturation (On-State) resistance must be minimized, which requires a very thin collector layer with a resistivity of a few tenths of an Ω-cm.

The Early Effect results in an increase in I_C due to base-width modulation when V_{CB} is increased.

Finding V_T: Using substrate resistivity $\rho \rightarrow N_A\&N_D$ (Vol I - pg 71) 2. Calculate ϕ_p 3. Calculate Q_f from given data Q_f/q 4. Calculate C_{ox} 5. Find ϕ_{MS} (depends on gate material, use Vol I - pg 96. 6. Calculate V_{FB} 7. Calculate V_T.

MOSFET's

$K_s = 11.8$ Dielectric Constant of Si (at 300 K)

$K_o = 3.9$ Dielectric Constant of SiO_2 (at 300K)

$\epsilon_s = K_s\epsilon_0 = 1.1045\times10^{-12}\frac{F}{cm}$ Permittivity of Si (at 300K)

$\epsilon_{ox} = K_0\epsilon_0 = 345.15\times10^{-15}\frac{F}{cm}$ Permittivity SiO_2 (300K)

P-type Si MOS Structure $\rightarrow$ N-channel Device

N-type Si MOS Structure $\rightarrow$ P-channel Device

Ref Voltage rel to the semicond doping concent. $\phi_{F(p-type)} = \phi_p = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)$

$\phi_{F(n-type)} = \phi_p = -\frac{kT}{q}\ln\left(\frac{N_D}{n_i}\right)$ Semicond Surf Pot at Depletion-Inversion Transition Point $\phi_S = 2\phi_F$

Flat-band voltage (voltage that produces flat energy bands in the oxide and silicon)

$V_{FB} = \phi_{MS} - \frac{Q_f}{C_{ox}}$ With a charge on the oxide layer.

$V_{FB} = \phi_M - \phi_S = \phi_{MS}$ oxide layer free of charge.

$W_T = \left[\frac{2K_s\epsilon_0}{qN_A}(2\phi_p)\right]^{1/2}$ Depletion Width Iv p 43

$\phi(x) = \frac{1}{q}[E_f - E_i(x)]$ Potential in Silicon

$\phi_S = \phi(0) = \frac{1}{q}(E_f - E_i(0))$ Surface Potential

$C_{ox} = \frac{\epsilon_{ox}}{x_{ox}}$ $\dot{A} = 10^{-10}m$ Oxide Layer Capacitance

$Q_{d(max)} = \sqrt{4k_s\epsilon_0 qN_A|\phi_P|}$ Space Charge Density (max)

$V_T = V_{FB}+2|\phi_p|+\frac{|Q_{d(max)}|}{C_{ox}}$, Threshold Voltage(T.V.)

$V_T = 2\phi_F - \frac{K_s x_{ox}}{K_{ox}}\left[\frac{4qN_A}{K_S\epsilon_0}\phi_F\right]$

$\Delta V_G = V_T' - V_T$ (Threshold Adjustment) $\Delta V_G = \frac{-Q_l}{C_{ox}}$

$Q_l = \pm qN_l \rightarrow N_l = \pm\frac{Q_l}{q}$ V_T' Un-adjusted T.V. V_T: Adjusted T.V. N_l: # of implanted ions Q_l: Implant-related charge/cm^2 Donor{+} or Acceptor {-}

$I_D = \frac{Z\bar{\mu}_n C_{ox}}{L}\left[(V_G - V_T)V_D - \frac{V_D^2}{2}\right]$ Square-law theory

Z: Width of MOSFET $\bar{\mu}_n$ Effe hole mobil Vol IV. Pg 73

Long Channel MOSFET Equation Bulk Charge Factor (α) $I_D = \mu C_{ox}\frac{W}{L}\left[\left(V_G - V_T - \frac{1}{2}V_D\right)V_D\right]$

$I_D = \mu C_{ox}\frac{W}{2\alpha L}\left[\left(V_G - V_T - \frac{1}{2}V_D\right)V_D\right]$

Channel Carrier Velocity (Using Long-Channel Theory) $V = \dfrac{\mu_n C_{ox}\left[\left(V_G - V_T - \frac{1}{2}V_D\right)V_D\right]}{Q_N L}$

Note: The saturation velocity of carriers in Silicon is: $v_{sat} \approx 10^7$ cm/s. If this equation yields a velocity $v > v_{sat}$, long channel theory does not apply in this situation. $Q_{n(source)} = C_{ox}(V_G - V_T)$, $Q_{n(drain)} = C_{ox}(V_G - V_D - V_T)$.

Drain Saturation Voltage $V_{D(sat)} = V_G - V_T$

$V_{D(sat)} = \frac{V_G - V_T}{\alpha}$.

g_d, g_m Small Signal Parameters and Conductance

$f_{max} = \frac{g_m}{2\pi C_{ox}} = \frac{\bar{\mu}_n V_D}{2\pi L^2}$ Cutoff f $V_D \leq V_{D(sat)}$

Using $I_{D(sat)} = \mu_n C_{ox}\frac{W}{2L}(V_G - V_T)^2$

Channel Dimensions $\frac{W}{L} = \frac{2I_{D(sat)}}{\mu_n C_{ox}(V_G - V_T)^2}$

MOSFET Integrated Circuit Applications

$V_T = V_{FB} + 2|\phi_p| + \frac{Q_{d(max)}}{\epsilon_{ox}}(d_1 + d_2) + \frac{Q_{fg}}{\epsilon_{ox}}d_1$ Charge stored on a floating gate memory cell

$|Q_{fg}| = \frac{\epsilon_{ox}}{d_1}\left[V_T - V_{FB} - 2\phi_P - \frac{Q_{d(max)}}{\epsilon_{ox}}(d_1 + d_2)\right]$,

Q_{fg} = Floating Gate Charge Density $V_{FB} = \phi_{MS}$

Step 1: Find V_{bi} (n-well to source/drain junction) using N_d from, the n-well and N_a from the p-channel source/drain.

Step 2: Find x_d using the doping levels and V_{bi}.

Step 3: Find V_{bi} (n-well to p-substrate junction) using N_d from the n-well and N_a from the p-substrate.

Step 4: Find x_n using V_{bi} and $V_a = V_{DD}$, and the same doping level as step 3.

Step 5: The minimum required n-well depth to prevent punchthrough at this voltage is:

$d_{n-well} = d_{p-channelsrc/drn} + x_{d(step2)} + x_{n(step4)}$

$V_{bi} = \frac{k_B T}{q}\ln\left(\frac{N_d N_a}{n_i^2}\right)$

$x_d = x_n + x_p = \left[\frac{2\epsilon_s}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)(V_a - V_{bi})\right]^{1/2}$,

$x_n = \left\{\frac{2K_s\epsilon_0}{q}(V_{bi} + V_a)\left[\frac{N_a}{N_d(N_a + N_d)}\right]\right\}^{1/2}$ Note: The p-channel source/drain depth $d_{p-channelsrc/drn}$ should be given in the question.

CMOS Well-Depth Design: Finding minimum well depth to prevent vertical punch through.

CMOS Structures P-Well: The substrate is N-Type. The N-Channel device is built into a P-Type well within the parent N-Type substrate. The P-channel device is built directly on the substrate.

N-Well: The substrate is P-Type. The N-channel device is built directly on the substrate, while the P-channel device is built into a N-type well within the parent P-Type substrate.

$g_d = \frac{Z\bar{\mu}_n C_o}{L}(V_G - V_T)$ $(V_D = 0)$

Practise Test 2 1) Which of the following can reduce the base transit time? c) Short base width.

2) Design the doping levels and dimensions of a silicon npn bipolar transistor such that the dc current gain is 320 and the Gummel Number is 10^{12}cm^{-2}. Assume that $\tau_n = 10^{-7}s$ in the base, $\tau_p = 10^{-8}s$ in the collector.

$GN = Q_B = \int_0^{x_B} N_{aB}(x)dx$.

Table 3.1 MOSFET Small Signal Parameters.*

	Below pinch-off ($V_D \le V_{Dsat}$)	Post pinch-off ($V_D > V_{Dsat}$)
Square law	$g_d = \frac{Z\bar{\mu}_n C_o}{L}(V_G - V_T - V_D)$	$g_d = 0$
Bulk charge	$g_d = \frac{Z\bar{\mu}_n C_o}{L}[V_G - V_T - V_D - V_W(\sqrt{1 + V_D/2\phi_F} - 1)]$	$g_d = 0$
Square law	$g_m = \frac{Z\bar{\mu}_n C_o}{L}V_D$	$g_m = \frac{Z\bar{\mu}_n C_o}{L}(V_G - V_T)$
Bulk charge	$g_m = \frac{Z\bar{\mu}_n C_o}{L}V_D$	$g_m = \frac{Z\bar{\mu}_n C_o}{L}V_{Dsat}$ with V_{Dsat} per Eq. (3.27)

*Entries in the table were obtained by direct differentiation of Eqs. (3.15), (3.20), and (3.26). The variation of $\bar{\mu}_n$ with V_G was neglected in establishing the g_m expressions.

Figure 1: Vol IV Mosfet table

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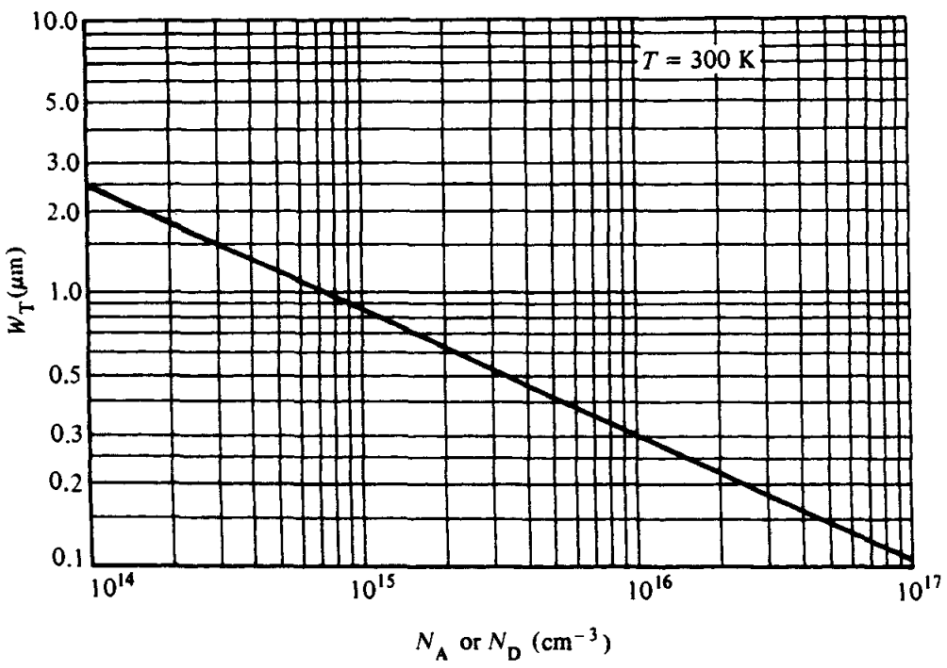

Figure 2: Doping dependence of the maximum equilibrium depletion width inside silicon devices maintained at 300 K.

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Table 12.1 | Notation used in the analysis of the bipolar transistor

Notation	Definition
For both the npn and pnp transistors	
N_E, N_B, N_C	Doping concentrations in the emitter, base, and collector
x_E, x_B, x_C	Widths of neutral emitter, base, and collector regions
D_E, D_B, D_C	*Minority carrier* diffusion coefficients in emitter, base, and collector regions
L_E, L_B, L_C	*Minority carrier* diffusion lengths in emitter, base, and collector regions
τ_{E0}, τ_{B0}, τ_{C0}	*Minority carrier* lifetimes in emitter, base, and collector regions
For the npn	
p_{E0}, n_{B0}, p_{C0}	Thermal-equilibrium *minority carrier* hole, electron, and hole concentrations in the emitter, base, and collector
$p_E(x')$, $n_B(x)$, $p_C(x'')$	Total *minority carrier* hole, electron, and hole concentrations in the emitter, base, and collector
$\delta p_E(x')$, $\delta n_B(x)$, $\delta p_C(x'')$	Excess *minority carrier* hole, electron, and hole concentrations in the emitter, base, and collector
For the pnp	
n_{E0}, p_{B0}, n_{C0}	Thermal-equilibrium *minority carrier* electron, hole, and electron concentrations in the emitter, base, and collector
$n_E(x')$, $p_B(x)$, $n_C(x'')$	Total *minority carrier* electron, hole, and electron concentrations in the emitter, base, and collector
$\delta n_E(x')$, $\delta p_B(x)$, $\delta n_C(x'')$	Excess *minority carrier* electron, hole, and electron concentrations in the emitter, base, and collector

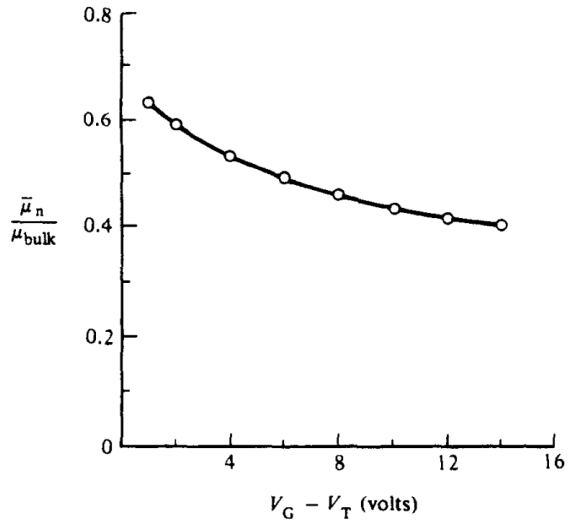

Figure 3: Vol IV Mosfet Gate voltages

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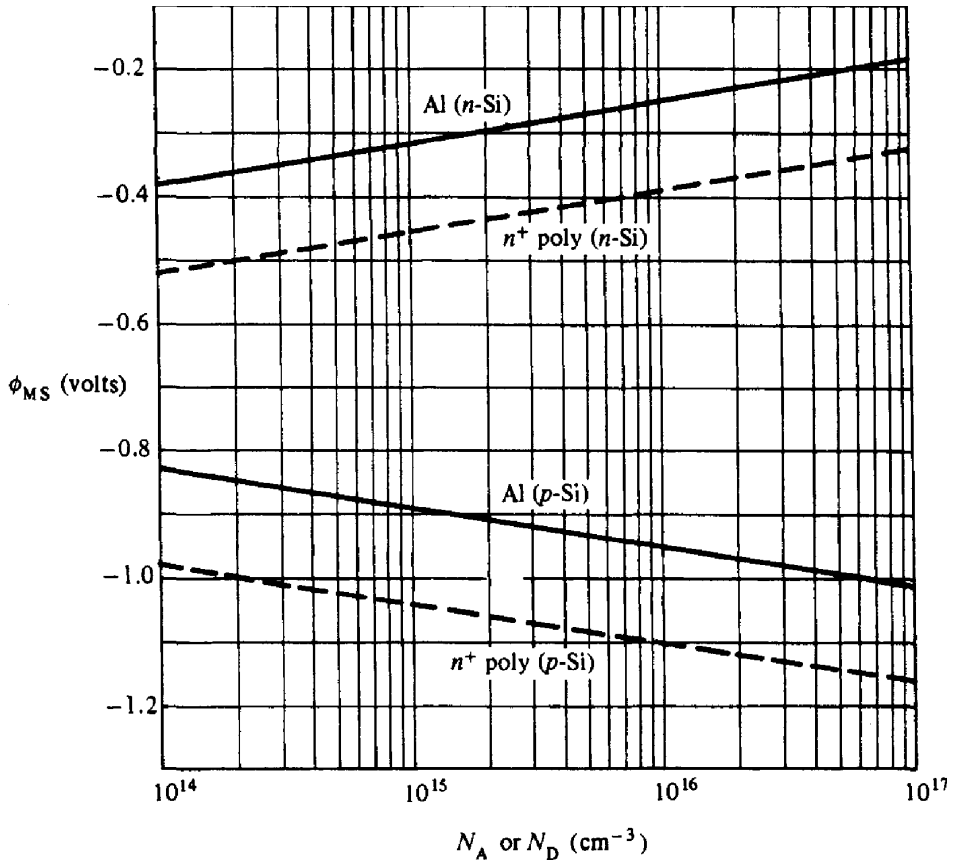

Figure 4: Workfunction difference as a function of a n- and p-type dopant conecntration in n^+ poly-Si-gate and Al-gate $SiO_2 - Si$ structures. ($T = 300K$. $\phi'_M - \chi' = -0.18\ eV$ for the n' poly-Si-gate structure; $\phi'_M - \chi' = 0.03eV$ for the Al-gate structure.)

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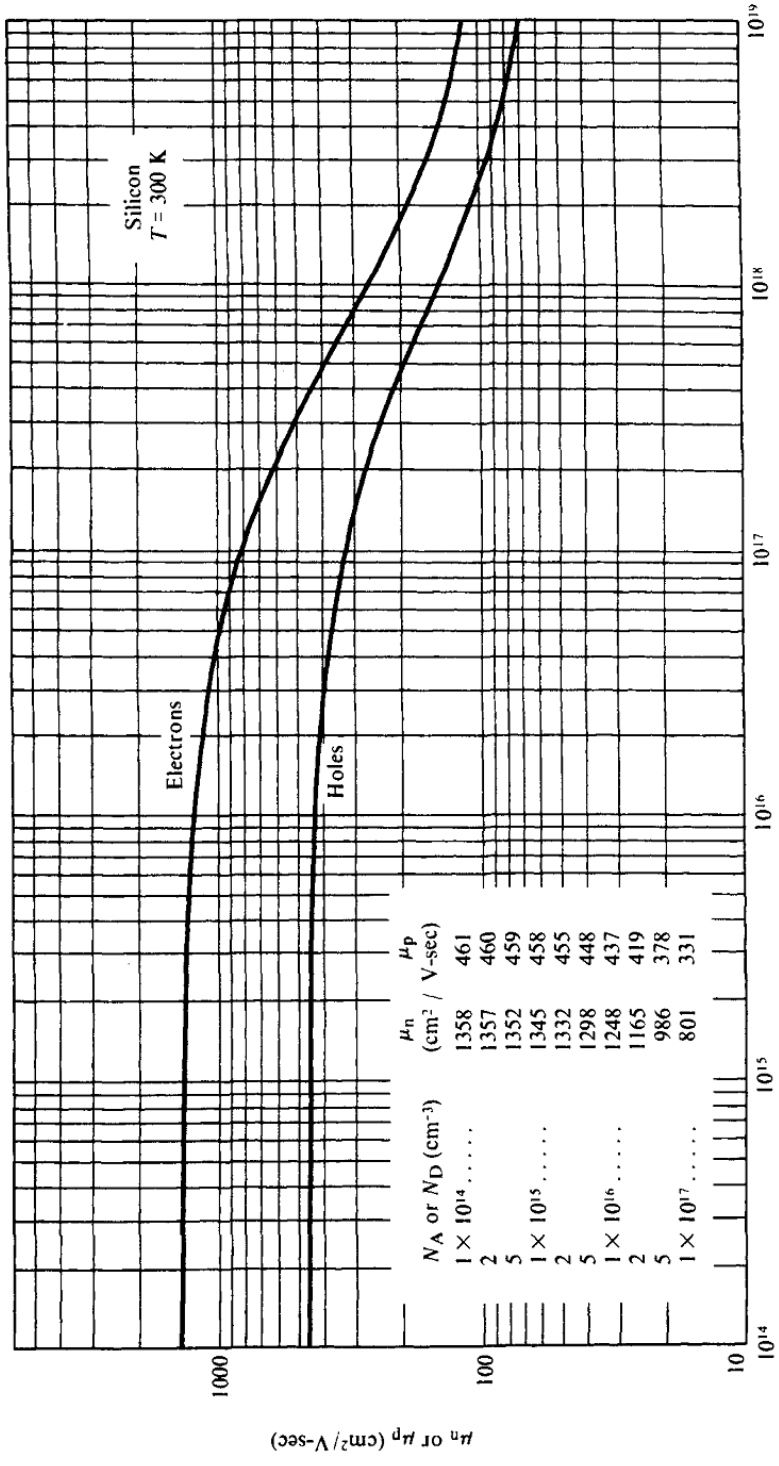


Fig. 3.5 Room-temperature carrier mobilities in silicon as a function of the dopant concentration. μ_n is the electron mobility; μ_p is the hole mobility.

Figure 5: Diffussion Constant

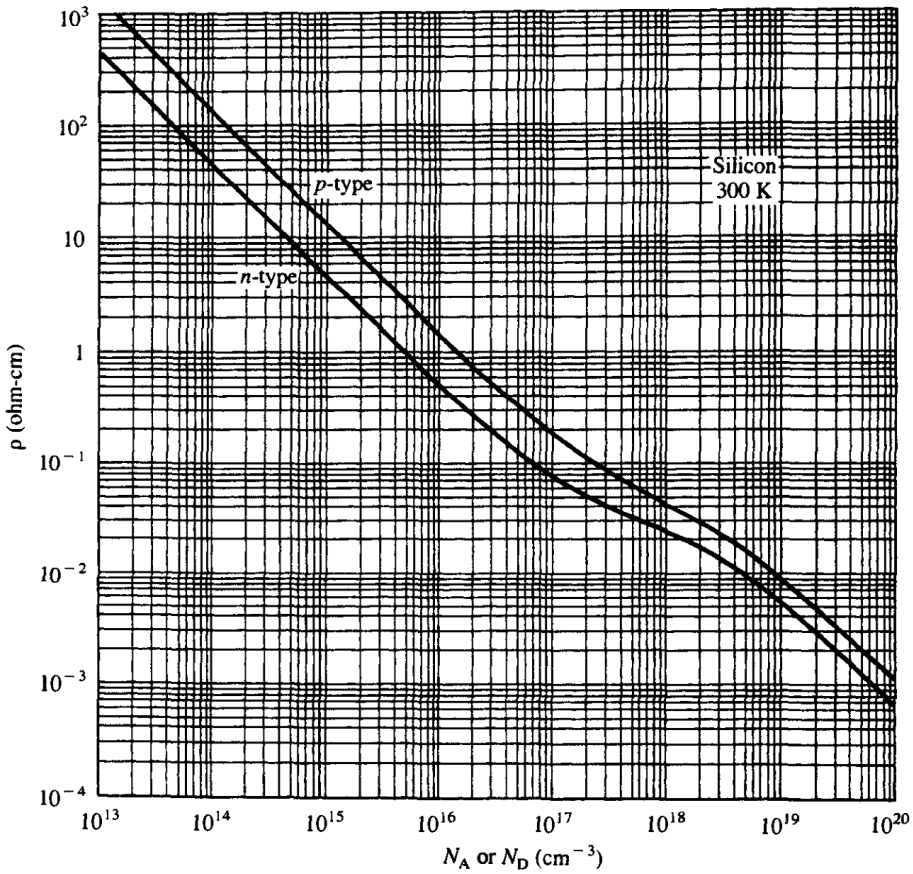
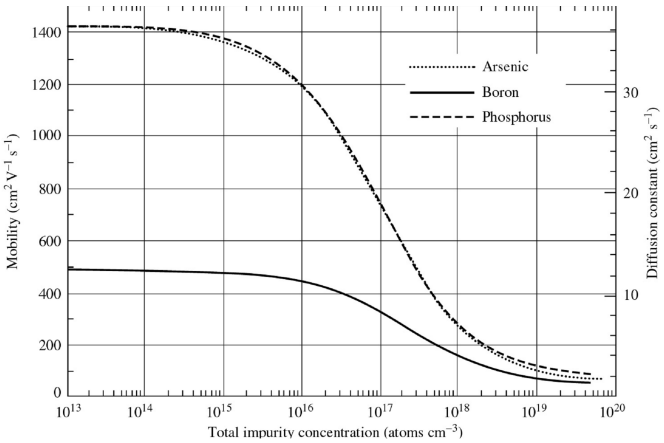


Fig. 3.7 Si resistivity versus impurity concentration at 300 K.



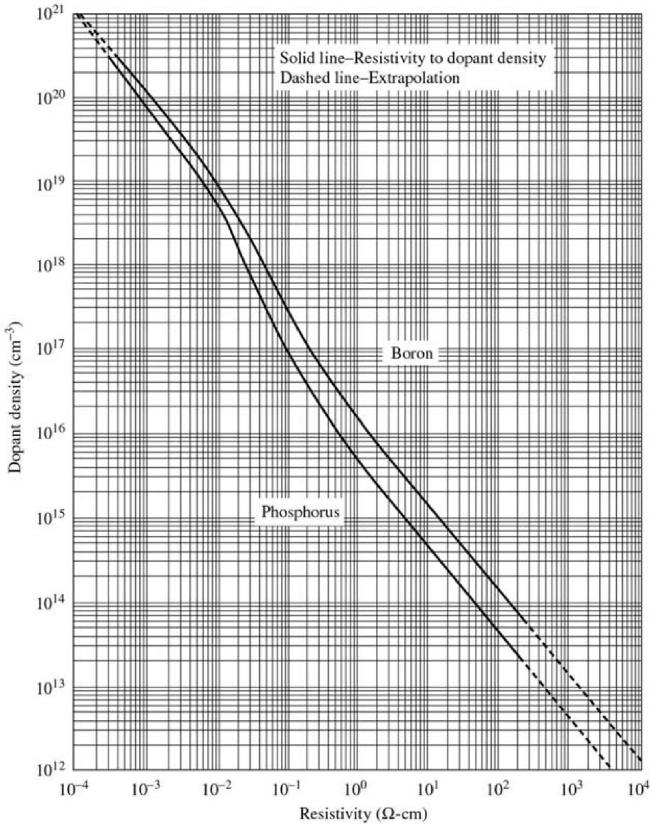


Figure 6: Boron Chart

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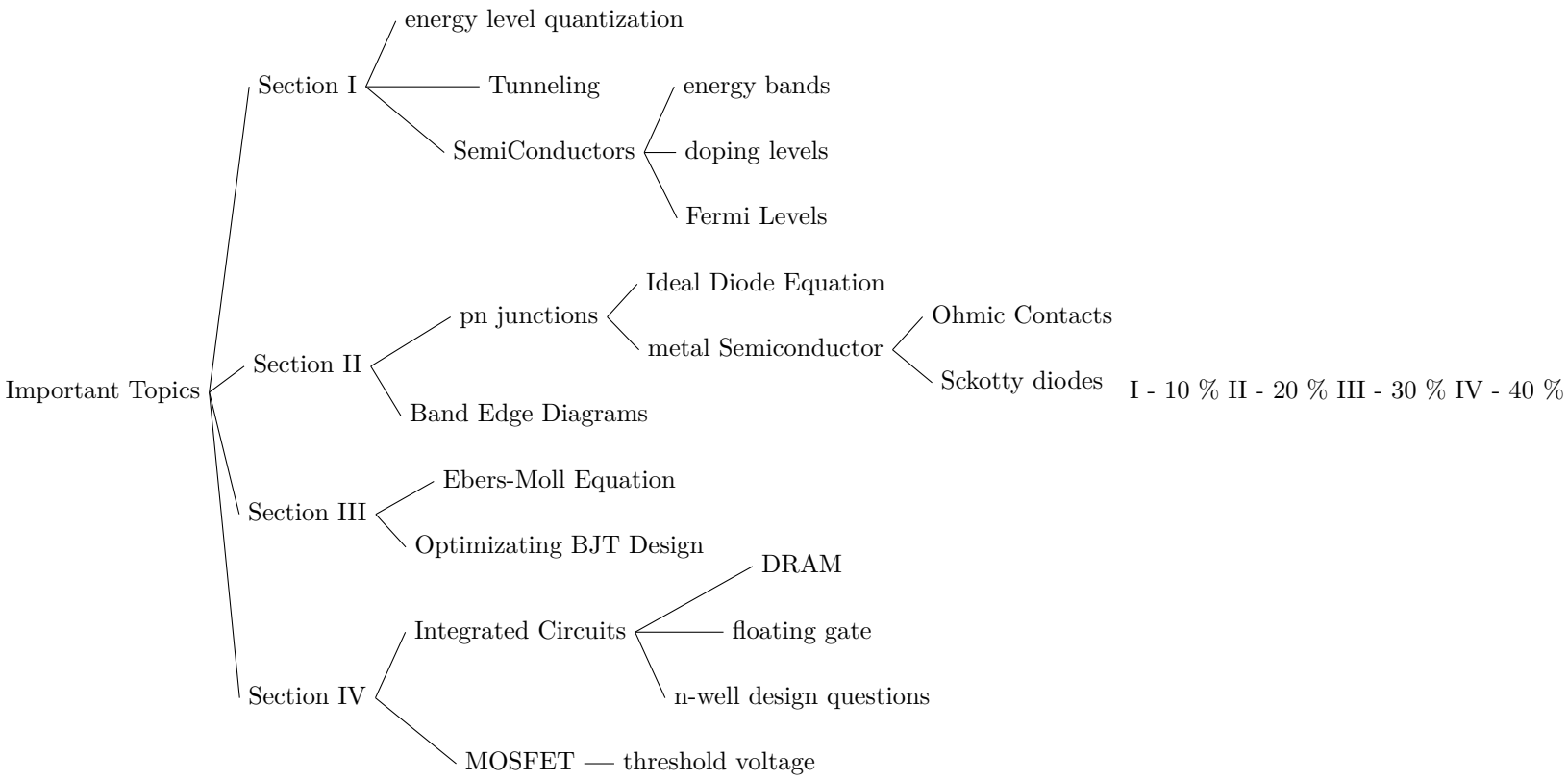
Important Topics
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MOSFET — threshold voltage
I - 10 % II - 20 % III - 30 % IV - 40 %