

COMPUTER ARCHITECTURES

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LAB 04 – WINMIPS

Considering a MIPS architecture with the following characteristics:

- Integer ALU: 1 clock cycle
- Data memory: 1 clock cycle
- FP arithmetic unit: pipelined, 2 clock cycles
- FP multiplier unit: pipelined, 4 clock cycles
- FP divider unit: not pipelined, 10 clock cycles

Assume also:

- branch delay slot not enabled
- data forwarding enabled
- EXE stage could be completed also in out-of-order fashion

Given the codes provided, estimate the number of clock cycles needed for completion.

Also, fill up the tables with the pipeline stages at each clock cycle (this is needed only for one iteration of the loop).

EX. 01

```
; ***** C *****  
; for (i = 0; i < 10; i++) {  
;     v4[i] = v1[i]/v2[i] + v3[i]*k;  
; }  
; ***** MIPS64 *****
```

```
.data  
V1: .double "10 values"  
V2: .double "10 values"  
V3: .double "10 values"  
V4: .double "10 values"
```

```
.text  
main: daddui r1,r0,0  
      daddui r2,r0,10  
cycle: l.d f1, v1(r2)  
       l.d f2, v2(r2)  
       l.d f3, v3(r2)  
       mul.d f5,f3,f4  
       div.d f6, f1, f2  
       add.d f7, f6, f5  
       s.d f7,v4(r1)  
       daddui r1,r1,8  
       daddi r2,r2,-1  
       bnez r2, cycle  
       halt
```

Total:

comments	Clock cycles
r1 ← pointer	
r2 ← 10	
f1 ← v1[i]	
f2 ← v2[i]	
f3 ← v3[i]	
f5 ← v3[i]*k	
f6 ← v1[i]/v2[i]	
f7 ← v3[i]*k + v1[i]/v2[i]	
v4[i] ← f7	
r1 ← r1+8	
r2 ← r2-1	

[illegible]

```
; ***** C *****
;  for (i = 0; i < 10; i++) {
;      v5[i] = v1[i]*v2[i] - v3[i]/v4[i];
;  }
; ***** MIPS64 *****
```

	comments	Clock cycles
.data		
V1: .double "10 values"		
V2: .double "10 values"		
V3: .double "10 values"		
...		
V5: .double "10 zeros"		
.text		
main: daddui r1,r0,0	$r1 \leftarrow \text{pointer}$	
daddui r2,r0,10	$r2 \leftarrow 10$	
loop: l.d f1,v1(r1)	$f1 \leftarrow v1[i]$	
l.d f2,v2(r1)	$f2 \leftarrow v2[i]$	
mul.d f5,f1,f2	$f5 \leftarrow v1[i] * v2[i]$	
l.d f3,v3(r1)	$f3 \leftarrow v3[i]$	
l.d f4,v4(r1)	$f4 \leftarrow v4[i]$	
div.d f6, f3, f4	$f6 \leftarrow v3[i] / v4[i]$	
sub.d f5,f5,f6	$f5 \leftarrow v1[i] * v2[i] - v3[i] / v4[i]$	
s.d f5,v5(r1)	$v5[i] \leftarrow f5$	
daddui r1,r1,8	$r1 \leftarrow r1 + 8$	
daddi r2,r2,-1	$r2 \leftarrow r2 - 1$	
bnez r2,loop		
halt		
Total:		

[illegible]