Cubik innovation
Electronic Design
Prototype
Production

Bristol & Bath Science Park
Dirac Crescent, Emersons Green
Bristol BS16 7FR

Tel: 0117 244 3000 Fax: 0117 244 3001
Web: www.cubik-innovation.co.uk

Project Name	Dongle
Project Number	TRI003
Project File Name	TRI003 Dongle V2.0.PrjPcb
Project Full Path	G:\Active\Projects\TRI003\Working Phase 1\Hardware\TRI003 Dongle
Variant Name	None

Schematic	
Schematic drawn by	Giles Sanders
Schematic/BOM Version	Issue 2.0

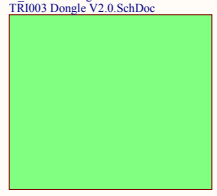
PCB	
PCB drawn by	Giles Sanders
PCB Name	TRI003 Dongle
PCB Version	Issue 2.0

Report Date & Time	3/31/2014 3:59:55 PM
Print Date:	31-Mar-14
Print Time:	3:59:59 PM

PCB CHECKLIST

Test rig fixing holes	NA
BOARD MARKER	NA
TRACE LABEL	NA
FIDUCIALS	NA
PCB THICKNESS [x] mm	1.6mm
PCB DIMENSIONS [x] mm X [x] mm	16mm x 25mm
SCOPE GROUND POINT [NET]	NA
ENCLOSURE	27JAN_con1_2_ASSY.pdf
Mounting holes	2 x 1.6mm
PCB Clearances	NA
PCB outline ref doc	27JAN_con1_2_ASSY.pdf
Logo on silkscreen	NA

U_TRI003 Dongle V0
TRI003 Dongle V2.0.SchDoc



NOTES
N.B. LED Cathodes are identified, assembler to refer to part datasheet for correct orientation

Project Number: TRI003			
Project Name: Dongle			
Title:		Version: Issue 2.0	
Size: A3	Number:1	Drawn by: Giles Sanders	
Date: 3/31/2014	Time: 4:00:02 PM	Sheet 1 of 2	
File: TRI003 Dongle Cover Sheet V2.0.SchDoc			

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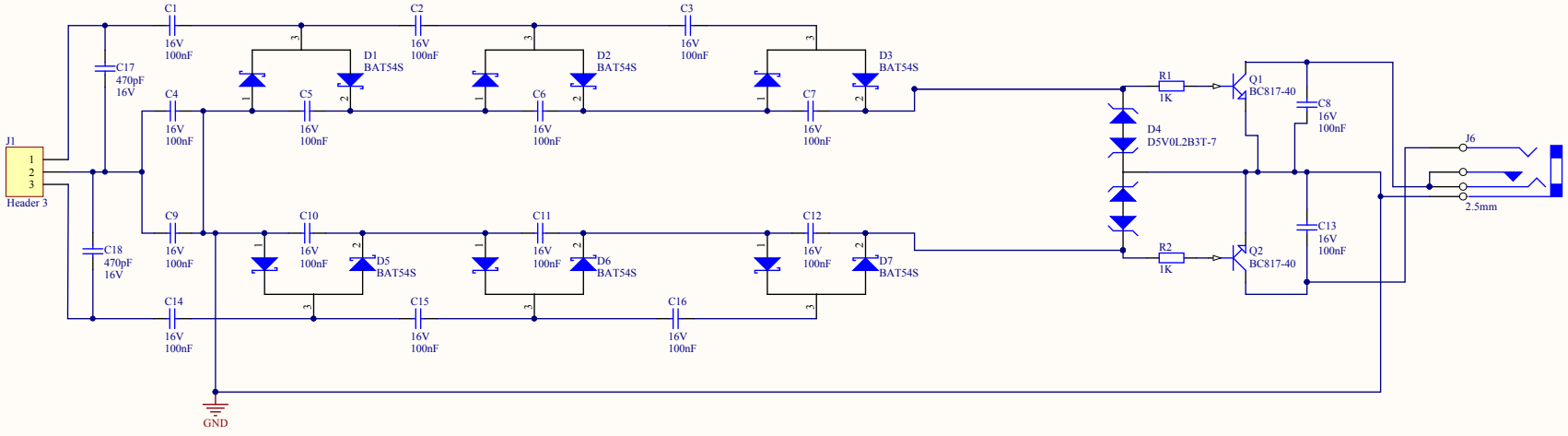

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Project Number:	***TRI003***		
Project Name:	***Dongle***		
Title:		Version:	***Issue 2.0***
Size: A3	Number:2	Drawn by:	***Giles Sanders***
Date: 3/31/2014	Time: 4:00:02 PM	Sheet 2 of 2	
File: TRI003 Dongle V2.0.SchDoc			

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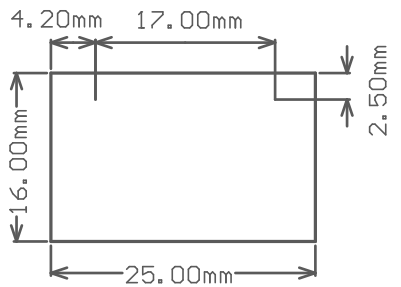

PLACE FMARKS ON PANEL

Manufacturing Notes

Finished Board Thickness 1.6mm
Board to be FR4 Material
Board is 2 layer
Double sided resist in GREEN
1 Ident bottom
Copper weight to be 1 oz finished
All Holes PTH
Please ignore all items outside MECH 1
Finish HASL Lead Free
PLACE FMARKS ON PANEL

Build notes

LED Cathodes are identified, assembler to refer to part datasheet for correct orientation.

Layout by:
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Bristol BS16 7FR

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Email: paul.mullen@cubik-innovation.co.uk

Layer

Mechanical 1
Mechanical 2
Top Overlay

Drawn by	Giles Sanders
Date	30/01/2014
Issue	Issue 2.0
Document Name	TRI003 Dongle V2.0.PcbDoc

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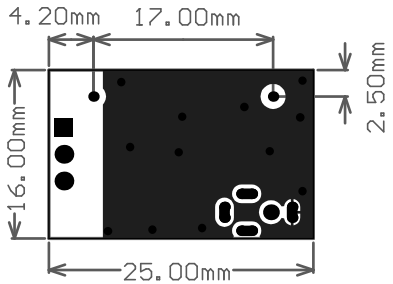
Layer

Mechanical 1
Mechanical 2

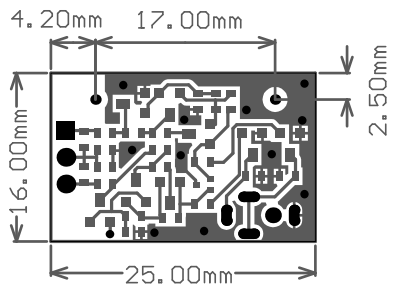
Multi-Layer

Top Layer



PLACE FMARKS ON PANEL

Drawn by	Giles Sanders
Date	30/01/2014
Issue	Issue 2.0
Document Name	TRI003 Dongle V2.0.PcbDoc



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Build notes

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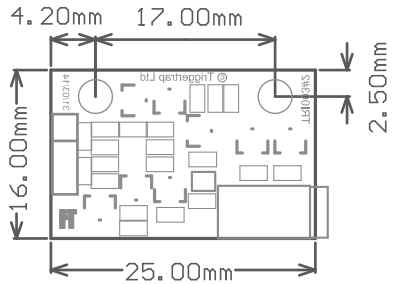
Layer

Mechanical 1
Mechanical 2

Keep-Out Layer

Bottom Layer

Drawn by	Giles Sanders
Date	30/01/2014
Issue	Issue 2.0
Document Name	TRI003 Dongle V2.0.PcbDoc



PLACE FMARKS ON PANEL

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Layer

Mechanical 1
Mechanical 2

Bottom Overlay

Drawn by	Giles Sanders
Date	30/01/2014
Issue	Issue 2.0
Document Name	TRI003 Dongle V2.0.PcbDoc

Design Rules Verification Report

Filename : G:\Active\Projects\TRI003\Working Phase 1\Hardware\TRI003 Dongle V2.0\TRI003 Dongle V2.0.PcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Silk primitive without silk layer	0
Assembly Testpoint Style (Under Component=Yes) (Disabled)(All)	0
Assembly Testpoint Usage (Valid =One Required, Allow multiple per net=No) (Disabled)(All)	0
Clearance Constraint (Gap=15mil) (InPolygon),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Silk to Silk (Clearance=2mil) (All),(All)	0
Silk To Solder Mask (Clearance=10mil) (Disabled)(IsPad),(All)	0
Minimum Solder Mask Sliver (Gap=10mil) (Disabled)(All),(All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=10mil) (Max=10mil) (Preferred=10mil) and Width	0
Hole Size Constraint (Min=1mil) (Max=100mil) (Disabled)(All)	0
Pads and Vias to follow the Drill pairs settings	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (Disabled)(All)	0
Component Clearance Constraint (Horizontal Gap = 10mil, Vertical Gap = 10mil) (Disabled)(All),(All)	0
Fabrication Testpoint Style (Under Component=Yes) (Disabled)(All)	0
Fabrication Testpoint Usage (Valid =One Required, Allow multiple per net=No) (Disabled)(All)	0
Routing Via (MinHoleWidth=15.748mil) (MaxHoleWidth=28mil) (PreferredHoleWidth=15.748mil) (MinWidth=31.496mil)	0
Routing Layers(All)	0
Width Constraint (Min=9mil) (Max=500mil) (Preferred=12mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Clearance Constraint (Gap=6mil) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Total	0