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SAMPLING FREQUENCIES RATIO ESTIMATION AND SYMBOL TIMING RECOVERY FOR BASEBAND BINARY PULSE AMPLITUDE MODULATION

by

Ana A. Paniagua Rodriguez

A report submitted in partial fulfillment
of the requirements for the degree

of

MASTER OF SCIENCE

in

Electrical Engineering

Approved:

Dr. Jacob H. Gunther Major Professor	Dr. Todd K. Moon Committee Member

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UTAH STATE UNIVERSITY
Logan, Utah

2008

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Abstract

Sampling Frequencies Ratio Estimation and Symbol Timing Recovery for Baseband Binary Pulse Amplitude Modulation

by

Ana A. Paniagua Rodriguez, Master of Science

Utah State University, 2008

Major Professor: Dr. Jacob H. Gunther
Department: Electrical and Computer Engineering

The original intent of this project was to perform real time digital communications between a personal computer (PC) as the transmitter and a digital signal processor (DSP) as the receiver using the audio band analog channel. Although transmitter and receiver were both designed with baseband binary Pulse Amplitude Modulation (PAM), a low data rate and a sampling rate of 8 kilohertz, it was not possible to achieve communication between the two with traditional synchronization algorithms because of large differences in sampling clock frequencies.

This thesis explores the theory and results of implementing digital communications between systems with different sampling frequencies. The receiver structure has no a priori knowledge of the transmitter's sampling rate, although it is assumed to be approximately equal to that of the receiver. Therefore, a receiver structure that can correct this clock frequency offset is developed.

Similar sampling frequencies at the transmitter and receiver are assumed in most derivations in the literature. A search of the literature found no cases of a large difference in the sampling frequencies. In general, if the receiver knows the transmitter's sampling rate, a resampling filter at the receiver converts the signal to one compatible with the transmitters

sampling rate. However, here it is assumed that the receiver does not know the transmitter's exact sampling frequency and must be estimated.

The mathematical expressions for the signals in the system are derived. The sampling frequency offset introduces errors in the correct detection of the signal when it is done through traditional synchronization algorithms. Therefore, a receiver structure that corrects the sampling frequency offset based on the interpolation concept is proposed. This structure will be shown to work when the correct sampling frequency ratio is known. Later, an approach to estimate the sampling frequency ratio is explored. A feedback estimator structure is derived from the Maximum Likelihood optimum criteria. A feed forward estimator that assumes the clock frequency of the transmitter and uses a synchronization sequence is explored as well.

(48 pages)

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Last, and most important, I would like to thank my parents, Etna and Cesar, for their love and teachings during all my life. To them I dedicate this thesis.

Ana Andreina Paniagua Rodriguez

Contents

List of Tables

List of Figures

Acronyms

A/D	Analog-to-Digital
AWGN	Additive White Gaussian Noise
D/A	Digital-to-Analog
DFT	Discrete Fourier Transform
DSP	Digital Signal Processor
FB	Feedback
FF	Feed Forward
FFT	Fast Fourier Transform
ISI	Intersymbol Interference
LUT	Look-Up Table
ML	Maximum Likelihood
NCO	Numerically Controlled Oscillator
PAM	Pulse Amplitude Modulation
PDF	Probability Density Function
PLL	Phase Locked Loop
SNR	Signal-to-Noise Ratio
SRRC	Square Root Raised Cosine
STR	Symbol Timing Recovery
TED	Timing Error Detector

Chapter 1

Introduction

The original intent of this project was to perform real time digital communications between a personal computer (PC) as the transmitter and a digital signal processor (DSP) as the receiver using the audio band analog channel. Although transmitter and receiver were both designed with baseband binary Pulse Amplitude Modulation (PAM), a low data rate and a sampling rate of 8 kilohertz, it was not possible to achieve communication between the two with traditional synchronization algorithms because of large differences in sampling clock frequencies. Therefore, this thesis presents the theory and results of implementing digital communications between systems that are working at different sampling frequencies.

The components of the transmitter and receiver are simulated by software (Fig. 1.1), so after the A/D conversion at the receiver all the signal processing is performed in discrete time. The exact sampling frequency of the transmitter, F_{s1}, is unknown to the receiver, although it is supposed to be close to 8 kilohertz.

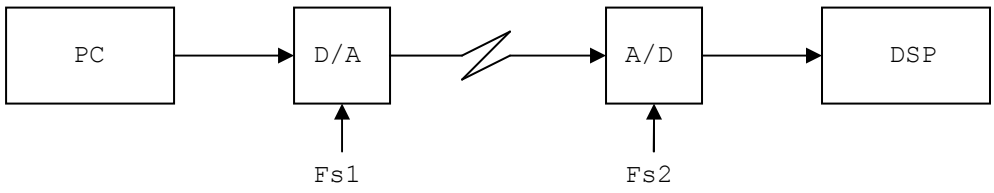

Fig. 1.1: Digital communication system.

1.1 Signals in the System

At the transmitter, the signal was generated using Matlab according to Fig. 1.2. At the output of the look-up table (LUT) the signal is given by

$$s(n) = \sum_n a(n)\,\delta(k-n), \tag{1.1}$$

where $a(n)$ is the n^{th} symbol of the sequence and $\delta(k-n)$ is the Kronecker delta function. In this case, $a(n) \in \{-1, +1\}$ because M = 2 in the M-ary PAM baseband signal. This signal is upsampled by a factor of N_1 in order to have N_1 samples per symbol. The output of the upsampler is the weighted impulse train

$$s(n) = \sum_n a(n)\,\delta(k-nN_1). \tag{1.2}$$

The sequence of data symbols modulate the amplitude of the baseband trasmitter pulse, which explains the name pulse amplitude modulation. The signal at the output of the transmitter pulse shaping filter is

$$\begin{aligned} s(n) &= \sum_n a(n)\,p([k-nN_1]\,T_1) && (1.3)\\ &= \sum_n a(n)\,p(kT_1 - nN_1T_1) && (1.4)\\ &= \sum_n a(n)\,p(kT_1 - nT_{s1}), && (1.5) \end{aligned}$$

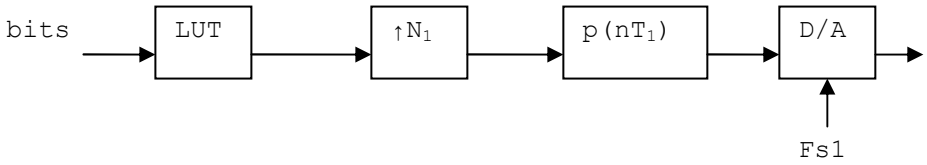

Fig. 1.2: Digital transmitter.

where $T_1 = \frac{1}{F_{s1}}$ is the sample period in the transmitter and $T_{s1} = \frac{N_1}{F_{s1}}$ is the symbol period in the transmitter. Both carry units of seconds.

After the discrete-time PAM signal is generated, it is transmitted through the sound card of the PC to the DSP with sample frequency $F_{s1} \approx 8$ kHz. At the output of the digital to analog converter the signal is of the form

$$s(t) = \sum_n a(n)\, p(t - nT_{s1}). \tag{1.6}$$

The receiver's analog-to-digital converter operates at a frequency F_{s2}. The symbol period is $T_{s2} = \frac{N_2}{F_{s2}}$, where $N_2 = N_1$ is assummed. Note that $F_{s1} = F_{s2}$ is assumed in most derivations in the literature [1–3]. No references have been found for the case $F_{s1} \neq F_{s2}$.

Here, consider the signal after being sampled at the receiver and ignore the noise added by the channel and its associated distortions. The sampled received signal is

$$\begin{aligned} s\left(\frac{k}{F_{s2}}\right) &= \sum_n a(n)\, p\left(\frac{k}{F_{s2}} - nT_{s1}\right) && (1.7) \\ &= \sum_n a(n)\, p\left(\frac{1}{F_{s2}}\left(k - nN_1\frac{F_{s2}}{F_{s1}}\right)\right). && (1.8) \end{aligned}$$

If $F_{s1} = F_{s2}$ the received signal can be demodulated and detected. Synchronization algorithms must be employed to estimate the value of unknown parameters (e.g., symbol timing, carrier phase or frequency) that interfere with accurate detection. On the other hand, if $F_{s1} \neq F_{s2}$, $\frac{F_{s2}}{F_{s1}}$ becomes a new unknown parameter in (1.8). Define $\eta = F_{s2}/F_{s1}$. The received signal can be demodulated and correctly detected if $F_{s1} \approx F_{s2}$. However, in the case of a considerable sampling frequency offset, η must be identified first and a sample rate conversion performed to demodulate the signal at the receiver. The effect of $\eta \neq 1$ can be observed comparing received and transmitted signals. The received sampled signal appears as an increasingly delayed version of the transmitted one as shown in Fig. 1.3.

For this project the TMS320C6713 DSP was used as the receiver with sample rate configured to be 8 kHz. The sound port of a PC with sample rate configured to be 8 kHz was used as the output of the transmitter. However, the DSP was actually working at a

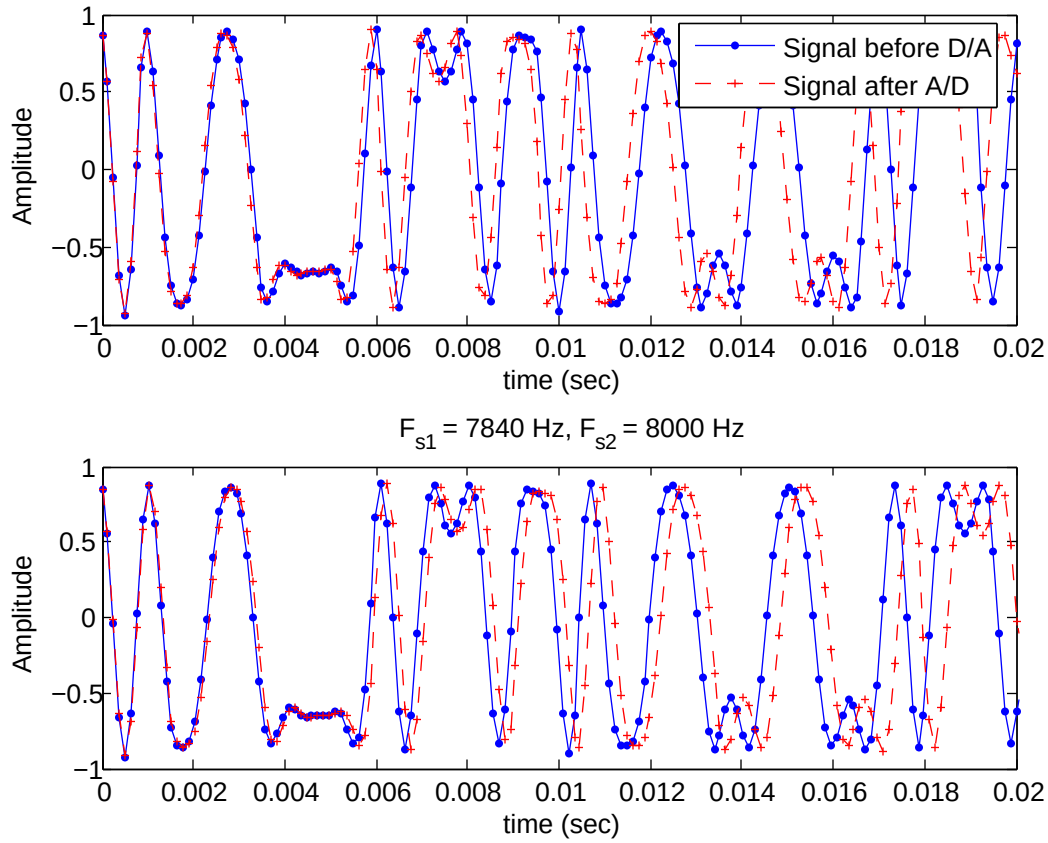

Fig. 1.3: When $\eta \neq 1$ the received signal is an increasingly delayed version of the transmitted signal. If $F_{s1} > F_{s2}$ the received sampled signal is a shrinked version of the transmitted one (top), and if $F_{s1} < F_{s2}$ the received sampled signal is a stretched version of the transmitted one (bottom).

different sampling rate. This difference in the transmitter and receiver sampling frequency was significant enough that made it impossible to synchronize using traditional techniques. Specifically, F_{s1} was unknown to the receiver. Generally if F_{s1} is known, a resampling filter can be used at the receiver to convert the signal to a transmitter's compatible sampling rate.

To analyze the effect of the clock frequency offset expand (1.8) and assume no channel distortion or noise:

$$s\left(\frac{k}{F_{s2}}\right) = a_0 p\left(\frac{k}{F_{s2}}\right) + a_1 p\left(\frac{k}{F_{s2}} - \frac{N_1}{F_{s1}}\right) + a_2 p\left(\frac{k}{F_{s2}} - 2\frac{N_1}{F_{s1}}\right) + ... + a_{N-1} p\left(\frac{k}{F_{s2}} - (N-1)\frac{N_1}{F_{s1}}\right). \tag{1.9}$$

The transmitted signal is generated as the result of multiplying each symbol of the sequence with a time translated version of the original transmitter pulse. In the continuous time domain (1.9) can be rewritten as:

$$s(t) = a_0 p(t) + a_1 p\left(t - \frac{N_1}{F_{s1}}\right) + a_2 p\left(t - 2\frac{N_1}{F_{s1}}\right) + ... \tag{1.10}$$

where the following equivalences are used:

$$0 \leq t \leq N\frac{N_1}{F_{s1}}, \tag{1.11}$$

$$0 \leq \frac{k}{F_{s2}} \leq N\frac{N_1}{F_{s1}}. \tag{1.12}$$

The discrete time domain of the receiver's pulse is affected by the factor η,

$$0 \leq k \leq NN_1\frac{F_{s2}}{F_{s1}}, \tag{1.13}$$

but the receive filter does not take into account this new time scale. To demodulate the received signal, η must be considered.

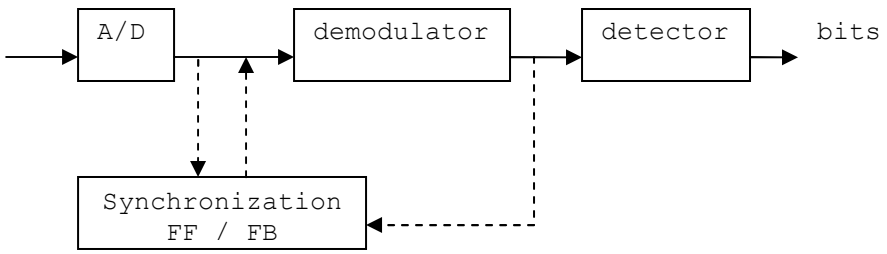

Fig. 1.4: Digital receiver.

1.2 Receiver Architecture

The channel between transmitter and receiver is assumed to be a linear filter that introduces linear distortions to the signal. At the input of the receiver the signal is a modified version of the transmitted signal plus white Gaussian noise (AWGN). In this section it will be assumed there is no difference between the sampling frequencies (i.e., $F_{s1} = F_{s2}$). Typical derivations of receivers (e.g., [2] and [3]) are developed for systems with no clock frequency offset.

The receiver can be viewed as a two part system: (1) demodulation and (2) signal detection (Fig. 1.4). At the demodulation stage the noise component should be reduced and the signal reshaped by the receiver filter. One architecture that has been widely proven as an optimum[1] receiver is the matched filter. Proakis [2] shows that a filter with an impulse response matched to the signal maximizes the output SNR of an AWGN corrupted signal.

At the detection stage and with no timing delay the output of the matched filter is the sampled signal, (1.8), convolved with the receive filter,

$$s\left(\frac{k}{F_{s2}}\right) = \sum_{n=0}^{N-1} a\left(n\right) r_p\left(\frac{k}{F_{s2}} - n\frac{1}{F_{s1}}\right), \tag{1.14}$$

where r_p is the convolution of the transmitted pulse $p\left(nT\right)$ with a filter that matches $p\left(nT\right)$ impulse response: $r_p\left(nT\right) = p\left(nT\right) * p\left(-nT\right)$.

[1] The criteria for optimum in this case is to minimize the probability of error.

When trying to detect the k^{th} symbol, the signal at the k^{th} instant can be expressed as

$$s\left(\frac{k}{F_{s2}}\right) = a\left(k\right) + \sum_{n\neq k}^{N-1} a\left(n\right) r_p\left(\frac{k}{F_{s2}} - n\frac{1}{F_{s1}}\right). \tag{1.15}$$

The first term of the right hand side is the desired symbol, while the second term is interference from the other symbols (i.e., ISI). An extremely important characteristic of the receive filter is the ability to reduce the ISI. This condition is known as the *Nyquist condition for zero ISI*[2] and the pulses that satisfy this condition are known as *Nyquist pulses*. A Nyquist pulse, the Square Root Raised Ccosine, and a matched filter demodulator are used in this project.

To this point the receiver was analyzed assuming that no distortions were introduced by the channel to the signal (see (1.8) - (1.14)). Several parameters, sometimes called "reference parameters," need to be synchronized prior to the detection of the signal. In real world applications, the channel's distortions and the shift between transmitter and receiver clocks should be incorporated into (1.8):

$$r\left(\frac{k}{F_{s2}}\right) = \sum_{n=0}^{N-1} a\left(n\right) p\left(\frac{1}{F_{s2}}\left(k - nN_1\frac{F_{s2}}{F_{s1}}\right) - \tau\right) + n\left(\frac{k}{F_{s2}}\right), \tag{1.16}$$

where $r\left(\frac{k}{F_{s2}}\right)$ is the received signal, the parameter τ is the time delay between the transmitter and the receiver and $n\left(\frac{k}{F_{s2}}\right)$ is the sampled version of the AWGN $n\left(t\right)$.

The receiver's decisions are done from this noisy signal. Therefore, to reduce the probability of error, these decisions should be derived at the optimum sampling instants. It has been widely shown in the literature that the optimum instant to sample the filtered incoming signal is when the eye diagram[3] is at its maximum opening. The channel distortions affect the optimum sampling instants of the signal, and therefore must be mitigated.

Reference parameters are generally estimated through synchronization. The structures

[2] **Nyquist Theorem**. A necessary and sufficient condition for $s\left(t\right)$ to satisfy $s\left(nT\right) = 1$ when $n = 0$ and $s\left(nT\right) = 0$ when $n \neq 0$ is that $\sum_{m=-\infty}^{\infty} S\left(f + \frac{m}{T_s}\right) = T_s$ when $S\left(f\right)$ is the Fourier Transform of $s\left(t\right)$.

[3] An eye diagram is an oscilloscope display of the signal at the matched filter output where information such as SNR and timing errors can be observed. In this case the display is done modulo the symbol period.

used to estimate the timing error are *timing recovery circuits* or *symbol timing synchronizers*. When different type of modulation is used or the demodulation is performed in a coherent[4] way additional reference parameters must be estimated. In those cases *carrier synchronization* and *frequency synchronization* are performed at the receiver to estimate the correct carrier phase or frequency, respectively.

Synchronization is an important yet difficult task in signal processing. The receiver and transmitter are each built with specifications that must be met at both ends for successful communication. Although a range of accuracy is specified by the transmitter and receiver equipment, the signal becomes distorted in its path to the receiver. Therefore, a number of parameters must be synchronized prior to the detection stage.

These parameters include the carrier frequency, carrier phase, symbol timing and frame synchronization. Generally, frame synchronization is performed after the first three parameters are correctly recovered. Carrier phase or carrier frequency are not necesarry for this project because the implementation is done at baseband, therefore only symbol timing synchronization is taken into account. Much attention is given to synchronization in the literature because the majority of signal processing at the receiver is intended to recover the reference parameters. Hence, several methods have been developed to achieve rapid and accurate synchronization.

Synchronizers can be classified into two groups according to the way they extract information from the signal: *feed forward* and *feedback*. Feed forward synchronizers estimate the parameters from the incoming signal and use this estimate in the synchronization circuit. This type of synchronizer does not suffer from hang-ups, and therefore allows rapid parameter acquisition [4]. Conversely, feedback synchronizers derive an estimate of the error of the parameters and minimizes the error through a signal to the synchronization circuit. Feedback synchronizers have an advantage over feed forward because they are able to automatically track parameters that vary slowly [1].

The reference parameters can be estimated directly from the unknown received symbols

[4]Coherent demodulation makes use of the phase relation between the reference carrier and the received signal.

or from a sequence of known symbols. These two approaches are classified as *data-aided* and *non-data-aided* algorithms, respectively. Non-data-aided synchronizers have the advantage that no bandwith nor power at the transmitter is employed in transmiting the known sequence. If a non-data-aided synchronizer uses the detected symbols in its algorithm then it is classified as a *decision-directed*.

1.3 A Limited Solution to Sampling Frequency Offset

This section reviews the implementation of symbol timing recovery for binary PAM. At the receiver, signal processing is done in discrete time, the incoming signal is sampled at F_{s2} by a free running oscillator and the timing recovery circuit uses the signal's samples to extract the timing error. This implementation is called asynchronous because the sampling rate F_{s2} is asynchronous to the transmitter's symbol rate T_{s1}.

The symbol timing recovery system works at the symbol rate with a structure similar to a phase locked-loop (PLL). In contrast to PLL, the estimated parameter is not the phase but rather the timing of the signal and other components are therefore used. To obtain the structure of the timing error detector the ML estimate of the timing parameter is analyzed. A derivation of the ML estimation for timing error for M-ary PAM is explained in detail in M. Rice [3]. Using the results from that derivation and from (1.16), the log-likelihood function for binary PAM is:

$$\Lambda\left(\underline{\mathbf{a}},\tau\right)=-\frac{L_0N}{2}ln\left(2\pi\sigma^2\right)-\frac{1}{2\sigma^2}\sum_{n=0}^{NL_0-1}\left\{\left|r\left(nT\right)\right|^2-2r\left(nT\right)s\left(nT;\tau\right)+\left|s\left(nT;\tau\right)\right|^2\right\}, \tag{1.17}$$

where $r\left(nT\right)=s\left(nT\right)+n\left(nT\right)$ is the received signal, and the representation $s\left(nT;\tau\right)$ has been used to denote that $s\left(nT\right)$ has a dependence on τ. Next, a derivation of the log-likelihood function with respect to the timing error τ finds the value of τ that will maximize this function. The value of τ that drives the derivative log-likelihood function to zero is the ML estimate of the timing error.

Note that neither the noise nor the first term in the log-likelihood function for binary PAM depend on the timing error. Inside the summation only the middle term has a strong

dependence on τ and thus the derivative log-likelihood function can be expressed as:

$$\frac{\partial}{\partial\tau}\Lambda\left(\underline{\mathbf{a}},\tau\right)=\frac{1}{\sigma^2}\frac{\partial}{\partial\tau}\sum_{k=0}^{L_0-1}a\left(k\right)\sum_{n=0}^{NL_0-1}r\left(nT_2\right)p\left(\frac{n}{F_{s2}}-k\frac{N_1}{F_{s2}}-\tau\right), \tag{1.18}$$

where $s\left(nT\right)$ was replaced with (1.14). The second summation

$$\sum_{n=0}^{NL_0-1}r\left(nT_2\right)p\left(\frac{n}{F_{s2}}-k\frac{N_1}{F_{s2}}-\tau\right) \tag{1.19}$$

is recognized as the matched filter output $x\left(\frac{k}{F_{s2}}+\tau\right)$, further reducing (1.18) to:

$$\frac{\partial}{\partial\tau}\Lambda\left(\underline{\mathbf{a}},\tau\right)=\frac{1}{\sigma^2}\frac{\partial}{\partial\tau}\sum_{k=0}^{L_0-1}a\left(k\right)x\left(k\frac{N_1}{F_{s2}}+\tau\right), \tag{1.20}$$

$$\sum_{k=0}^{L_0-1}a\left(k\right)\dot{x}\left(\frac{k}{F_{s2}}+\tau\right)=0. \tag{1.21}$$

This equation sets the structure of the timing error detector (see Fig. 1.5). In the structure first, an interpolator is used to derive the samples at the correct time. Next, the error estimate is extracted using the samples at the output of a derivative matched filter $\dot{x}\left(\frac{k}{F_{s2}}+\tau\right)$ and the summation in (1.21) is interpreted as a low pass filter which output drives an interpolation control that determine the new sampling times of the signal.

The above derivation was done using the known symbols $a\left(k\right)$, but a non-data-aided estimator can be obtained similarly by using the decision of the symbol $\hat{a}\left(k\right)$ instead of the known symbol $a\left(k\right)$. For a detailed derivation of the ML estimation for timing error refer to M. Rice [3].

Only the ML TED is analyzed here and the timing recovery circuit was derived based on this structure. Rice [3] and Proakis [2] cover several TEDs as the Muller and Mueller [5] decision-directed TED, the zero crossing TED or the early-late gate non-decision directed TED. Among them the optimal criteria of ML was used for this project because the others have been proven to be ad-hoc estimations of the ML function.

Note that the sample clock at the receiver is independent of the symbol clock at the

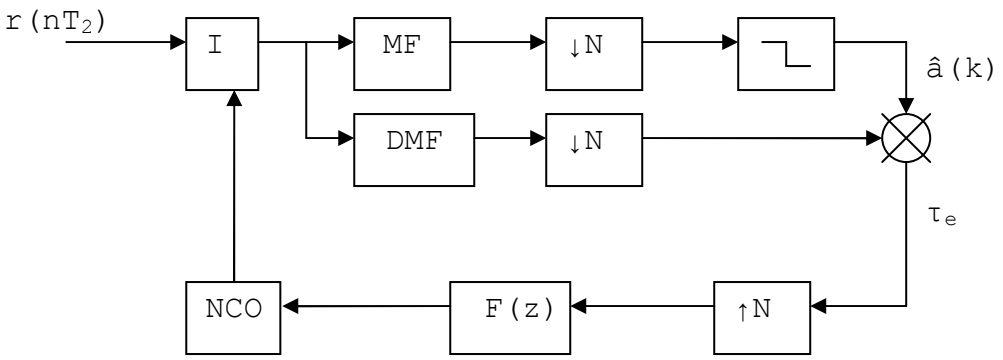

Fig. 1.5: Symbol timing recovery circuit with ML TED.

transmitter. That is, T and T_s are incommensurate. Accordingly, at the receiver only the sample clock $1/T_{s2}$ is known and is independent from the symbol clock $1/T_1$. The different relationships between T and T_s dictate the behavior of the interpolation parameters in the symbol timing synchronization circuit.

Symbol timing synchronization can work in cases where the sampling frequencies are approximately equal: $F_{s1} \approx F_{s2}$ [1]. If the STR is based on a structure similar to a PLL then based on the behavior of PLLs, there is a frequency offset Δf within which the loop can lock [3]. This frequency offset (also called pull-in range) is related to the noise bandwith B_n of the signal and the damping factor ζ of the loop:

$$\Delta f_{pull-in} \approx \left(2\pi\sqrt{2}\zeta\right) B_n. \tag{1.22}$$

However if the frequency difference is too large, the loop may never lock. This thesis explores those cases where the frequency offset was such that the PLL could not lock.

The objective of this chapter is to introduce the problem of sampling frequency offset between the transmitter and receiver of a communication system. In the cases of small offsets communication can still be achieved with STR. Meyr, Moeneclaey and Fetchel [1], in the performance analysis of synchronizers, point the behavior of feedback and feed forward synchronizers in the case of small sampling frequency offset. The allowable frequency offset

in that case was defined to be a very small fraction of the symbol rate. Nevertheless, the literature fails to mathematically analyze the case of clock frequency offset.

From the structures of digital PLLs, the permissible sampling frequency offset for a PLL based receiver is obtained. Lindsey et al. [6] have profoundly studied the structure of digital PLLs and their frequency stability. Rice [3] states the case of frequency offset when covering the PLLs behavior and structure; he also gives a good explanation of STR circuit and the function of its PLL similar components. However, there is not too much information in the literature about the relationship between digital PLLs and STR algorithms.

Only the used of ML TED was covered here, its performance characteristics are detailed in Proakis [2]. Other TED are easily available in the literature because the performance of them does not affect directly the problem stated in this thesis they are just mentioned. For a mathematical insight in synchronization algorithms, Meyr et al. [1] explains different cases like data-aided or non-data-aided systems, operating at the symbol rate or higher rates.

Chapter 2

Architecture and Estimation Algorithm for Sampling Rate Estimation and Correction

This chapter presents a receiver structure designed to correct an offset between the sampling frequencies detailed in Chapter 1. Here the use of interpolation in timing adjustment will be reviewed because the structure uses interpolation of the received signal to resample at the transmitter's sampling rate. The receiver's structure is first shown to work when the correct η is provided. Next, an algorithm is derived to estimate the correct η from the incoming signal with the ML optimum criteria. Finally, an architecture is suggested from the estimate of η.

2.1 Interpolation for Timing Adjustment

The sampling clock at the receiver is fixed and asynchronous to the transmitter's symbol clock. In STR, the non synchronized samples are interpolated to obtain new samples synchronized to the transmitter's symbol rate. Digital interpolation for timing recovery is detailed in F. M. Gardner [7].

The STR structure used in this case is as follows: (1) interpolation is performed on every incoming sample, (2) the interpolated samples are demodulated and (3) the symbol decision is performed on the desired interpolated sample (Fig. 1.5). The interpolation parameters are updated at the symbol rate, because the TED outputs an error value every symbol period. An alternative approach that will not be covered here is to upsample the signal and then downsample with an offset that will produce the desired interpolant [8].

Here the terms and concepts for interpolation and interpolation control when performing symbol timing recovery are reviewed. At the A/D, samples are taken at T uniform intervals: ..., $x\left(\left(n-1\right)T\right)$, $x\left(nT\right)$, $x\left(\left(n+1\right)T\right)$, ... On the other hand, symbols are uni-

formly spaced at T_s. Because the samples are not synchronized with the symbol rate, let the desired sample fall somewhere between $x(nT)$ and $x((n+1)T)$ (see Fig. 2.1a).

The interpolation function can be derived assuming that the digital signal $x(nT)$ is converted to continuous time $x(t)$ and filtered by an interpolating filter with impulse response $h_I(n)$:

$$x_i(t) = \sum_n x(nT)\, h_I(t - nT). \tag{2.1}$$

The sample at the desired sample time kT_I is obtained by evaluating $x_i(t)$ at $t = kT_I$:

$$x_i(kT_I) = \sum_n x(nT)\, h_I(kT_I - nT). \tag{2.2}$$

Equation (2.2) can be expressed in terms of an index i. Define the change of variable [7] $i = m_k - n$, where n is the index of the signal samples, $m_k = floor\left(\frac{kT_I}{T}\right)$ is a basepoint index and $\mu_k = \frac{kT_I}{T} - m_k$ is a fractional interval. The following equation is the foundation for digital interpolation and is obtained using the previous definitions in (2.2):

$$x_i(kT_I) = \sum_{i=I_1}^{I_2} x[(m_k - i)T]\, h_I[(\mu_k + i)T], \tag{2.3}$$

where the number of taps of the filter is defined by $I_2 - I_1 + 1$. The sample index is called the *basepoint index* and represented by m_k. The desired sample is located at a fraction of the sample time (Fig. 2.1b), between nT and $(n+1)T$. This fraction is called *fractional interval*, μ_k, and it satisfies $0 \leq \mu(k) < 1$.

Note in (2.3) that samples of the input sequence, the impulse response of the interpolating filter, the basepoint index and the fractional interval must be known to obtain the desired interpolant.

The interpolation control structure provides the parameters m_k and μ_k to the interpolation function. Signal samples are available every T seconds so the interpolation control also provides a trigger signal that is synchronized with the transmitter's symbol rate.

The interpolation control is performed by a numerically controlled oscillator (NCO). In this case, the NCO is a decrementing modulo-1 register that triggers every N samples

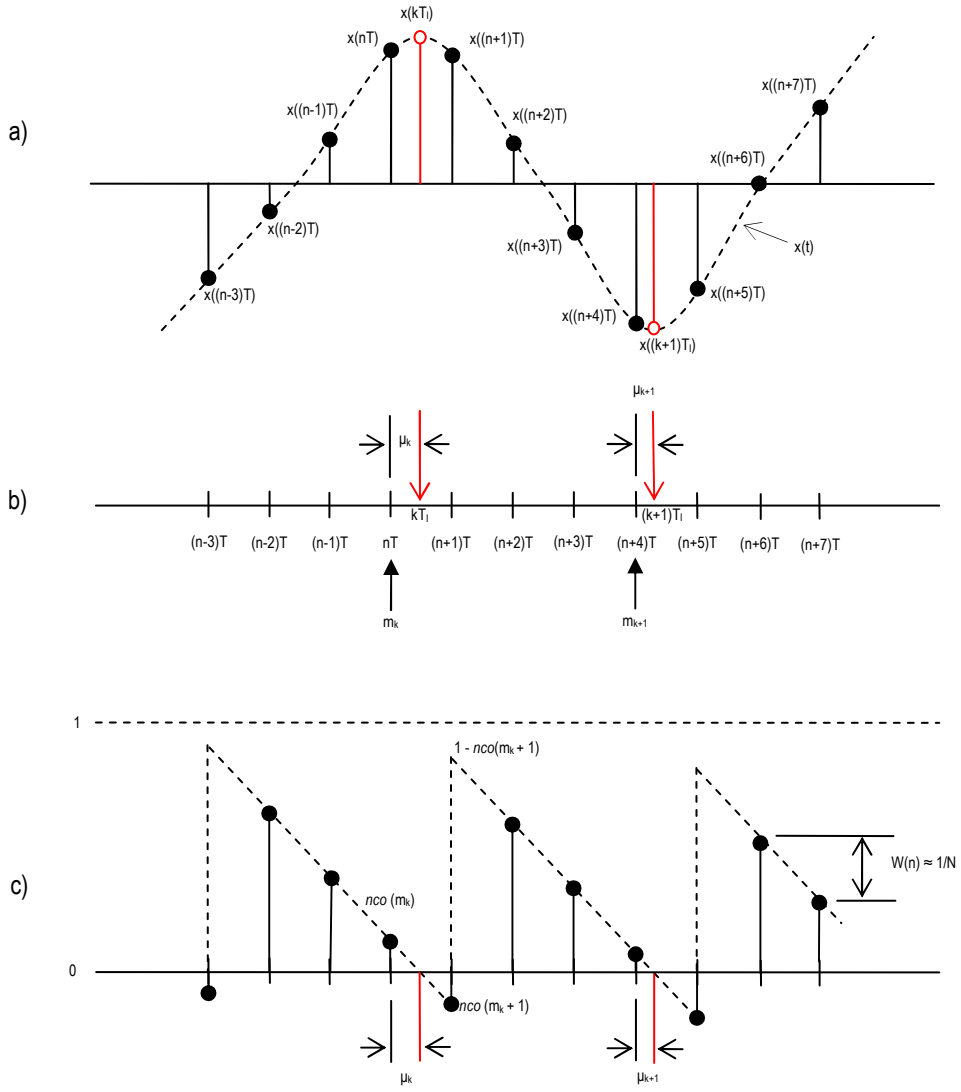

Fig. 2.1: From M. Rice [3]: a)Relationship between the available samples and the desired one. b)Relationship between the interpolation interval T_I, the sample time T, the basepoint index m_k and the fractional interval μ_k. c)Relationship between the NCO register, basepoint index m_k and fractional interval μ_k. The fractional interval μ_k is calculated from the NCO register content and the control word $W(n)$ using similar triangles.

(Fig. 2.1c). The fractional interval and the trigger signal are calculated from the NCO register as follows. Let $nco\,(m)$ be the content of the NCO register:

$$nco\,(m) = [nco\,(m-1) - W\,(m-1)]\,mod\,(1)\,. \tag{2.4}$$

The control word $W\,(m-1)$ satistifies $W\,(m-1) = \frac{1}{N} + v\,(m-1)$ in the case of timing error synchronization, where $v\,(m)$ is the loop filter output. In general, the contents of the NCO register will decrement by the amount $W\,(m)$ every T seconds on average, so the NCO register will underflow every T_s seconds. Therefore, the NCO period is $T_i = \frac{T}{W(m)}$ and the control word can be rewritten as:

$$W\,(m) = \frac{T}{T_i}. \tag{2.5}$$

$W\,(m)$ can be interpreted as the estimate of the ratio of the sampling period to the interpolation period.

The value of the fractional interval is obtained from the NCO register values using similar triangles (Fig. 2.1c) according to

$$\frac{\mu_k T}{nco\,(m_k)} = \frac{(1-\mu_k)\,T}{1 - nco\,(m_k+1)}, \tag{2.6}$$

$$\mu_k = \frac{nco\,(m_k)}{W\,(m_k)}. \tag{2.7}$$

2.2 Architecture for Sampling Rate Correction

The objective of this thesis is to resample the received signal to a rate that is equal to the transmitter. Based on the concepts detailed in Sec. 2.1, a receiver structure was designed that correctly recovers information when the sampling frequency ratio, η, is known. Here this structure is further explained.

At the A/D the samples are taken at T_2 uniform intervals, however the desired samples are spaced at T_1 uniform intervals (Fig. 2.2). To counteract this problem the A/D samples at T_2 are used to extract the desired samples at intervals T_1. If $F_{s1} > F_{s2}$ the period between desired samples is smaller than the period between A/D samples (i.e., $T_1 < T_2$) which

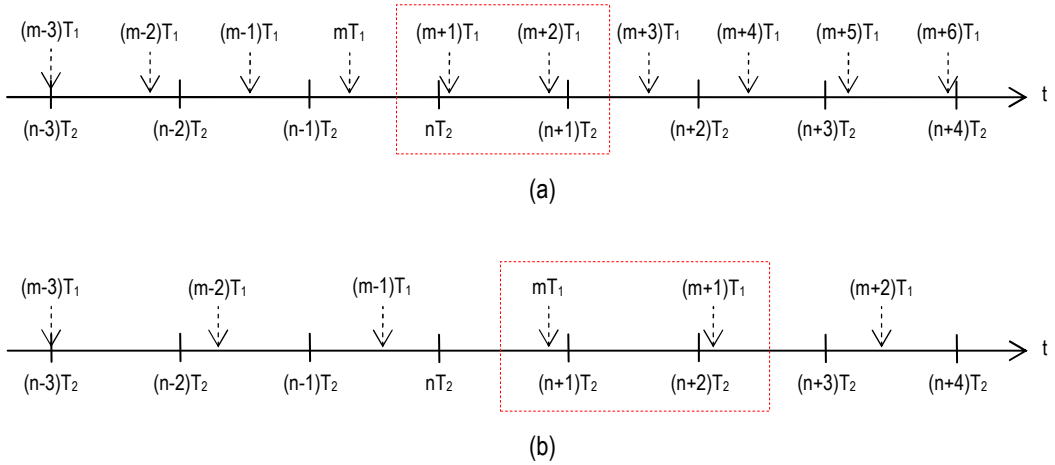

Fig. 2.2: Relationship between A/D samples and desired samples: (a) $F_{s1} > F_{s2}$ and (b) $F_{s1} < F_{s2}$.

creates instances where more than one new sample must be extracted from an available A/D sample (see box in Fig. 2.2a). Conversely, if $F_{s1} < F_{s2}$ then $T_1 > T_2$ and new samples are not required from each available A/D sample (see box in Fig. 2.2b).

In Sec. 2.1 when the interpolation was analyzed for symbol timing recovery, the NCO was used because one sample per symbol period was needed. In this case, when the interpolation is used to resample at the transmitter sampling rate, a new sample per transmitter's period, T_1, is required. For timing recovery it was derived that the control word used at the NCO is an estimate of the ratio of the sampling frequency to the interpolation frequency (2.5). Similarly, in the interpolation for sampling frequency recovery, the control word is an estimate of the receiver's sampling frequency to transmitter's sampling frequency: $\frac{F_{s2}}{F_{s1}}$, previously defined as η.

Since an interpolant needs to be output every T_1 seconds, and the incoming samples are every T_2 seconds, the NCO notifies the interpolator about the relationship between the time axis t_1 and t_2. The NCO tracks when zero or more than one (i.e., $\neq 1$) interpolated samples occur within T_2 seconds, as shown in the boxes in Fig. 2.2. In the receiver structure developed here the NCO is a modulo-1 counter that will underflow every time an interpolated sample is needed.

Note that when $F_{s1} > F_{s2}$, the fractional interval will be continuously decrementing

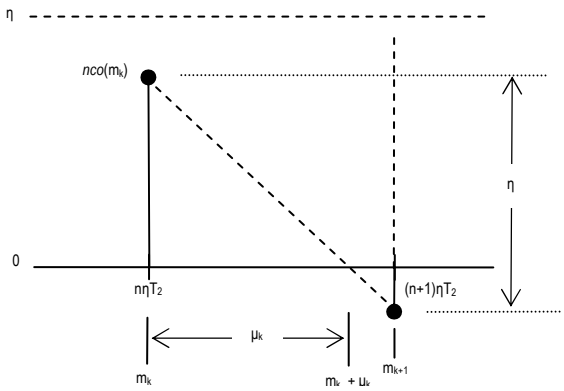

Fig. 2.3: Relationship between NCO register, fractional interval μ_k and basepoint index m_k.

(or continuosly incrementing if $F_{s1} < F_{s2}$) in the interval $0 \leq \mu_k < 1$ and will reset with a period related to η. Here, the STR approach is used to calculate μ at the k^{th} instant (see Fig. 2.3):

$$\frac{\mu_k \eta T_2}{\eta T_2} = \frac{nco\,(m_k)}{\eta}, \tag{2.8}$$

$$\mu_k = \frac{nco\,(m_k)}{\eta}. \tag{2.9}$$

The flow of this new receiver architecture (Fig. 2.4) is summarized in Table 2.1. Note in Fig. 2.4 that at the output of the A/D, the frequency is F_{s2} and at the output of the interpolator the transmitter's sampling frequency, F_{s1}, has been recovered.

The demodulation and detection of the newly sampled signal is performed with a traditional receiver structure. The timing error, obtained with the TED defined in Chapter

Table 2.1: Sampling frequency offset receiver pseudocode.

1. The A/D output a new sample.
2. Fill the interpolation buffer with new sample.
3. Evaluate trigger signal at the NCO.
4. If there is a trigger signal at the NCO:
   - perform interpolation
   - perform demodulation and detection
   - calculate timing error
   - go to 3.

   else
   - go to 1.

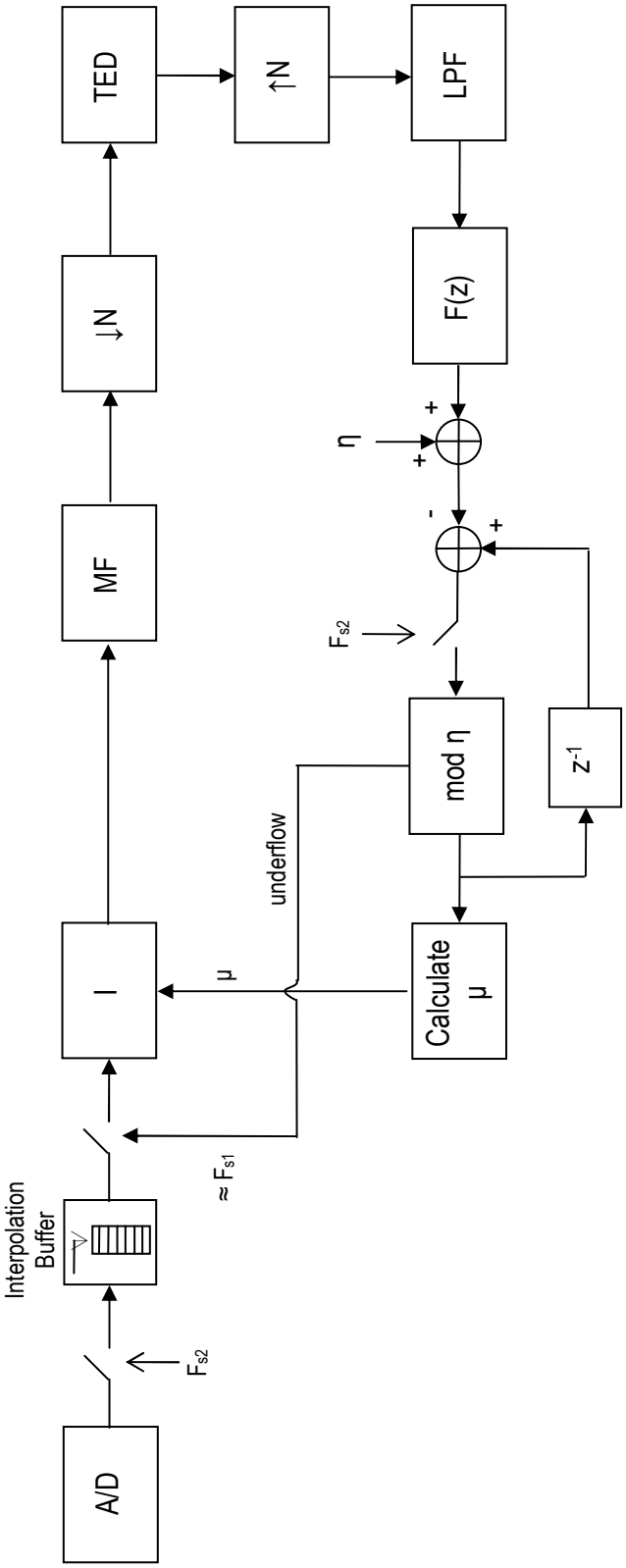

Fig. 2.4: Sampling frequency offset correction receiver structure.

1 (1.21), drives the feedback system and the control word $W(n)$ is set to the known value of η.

2.3 Maximum Likelihood Estimation of η

The receiver structure developed in Sec. 2.2 was shown to work with the correct sampling frequency ratio, η. Therefore, what follows is a derivation of the parameter η using the ML optimum criteria. For this derivation let $r(t) = s(t) + n(t)$ be the received signal, where $s(t)$ is the transmitted signal and $n(t)$ is AWGN (1.6):

$$s(t) = \sum_n a(n)\, p(t - nT_{s1}), \tag{2.10}$$

where $T_{s1} = N_1/F_{s1}$ is the symbol period at the transmitter. This signal is sampled at the analog-to-digital converter by a free running oscillator with frequency F_{s2}:

$$\begin{aligned}
s(kT_2) &= s(t)\,|_{t=kT_2} && (2.11)\\
&= \sum_{n=0}^{L_0-1} a(n)\, p(kT_2 - nT_{s1}) && (2.12)\\
&= \sum_{n=0}^{L_0-1} a(n)\, p\left(kT_2 - n\frac{N_1}{F_{s1}}\right) && (2.13)\\
&= \sum_{n=0}^{L_0-1} a(n)\, p\left(k\frac{1}{F_{s2}} - n\frac{N_1}{F_{s1}}\frac{F_{s2}}{F_{s2}}\right) && (2.14)\\
&= \sum_{n=0}^{L_0-1} a(n)\, p\left(\frac{1}{F_{s2}}\left(k - nN_1\frac{F_{s2}}{F_{s1}}\right)\right) && (2.15)\\
&= \sum_{n=0}^{L_0-1} a(n)\, p\left(\frac{1}{F_{s2}}\left(k - nN_1\eta\right)\right). && (2.16)
\end{aligned}$$

To find the log-likelihood function $p(\underline{\mathbf{r}}|\underline{\mathbf{a}}, \eta)$ recall that the noise $n(t)$ is Gaussian, white and zero-mean, therefore its probability density function (pdf) is:

$$p(\underline{\mathbf{n}}) = \frac{1}{(2\pi\sigma^2)^{L_0N/2}} \exp\left\{-\frac{1}{2\sigma^2}\sum_{k=0}^{NL_0-1} n^2(kT_2)\right\}, \tag{2.17}$$

where the bold and underline text is used to represent vectors, so $\underline{\mathbf{r}} = \underline{\mathbf{s}} + \underline{\mathbf{n}}$. The joint pdf $p\left(\underline{\mathbf{r}}|\underline{\mathbf{a}}, \eta\right)$ can be expressed as

$$p\left(\underline{\mathbf{r}}|\underline{\mathbf{a}}, \eta\right) = \frac{1}{\left(2\pi\sigma^2\right)^{L_0 N/2}} \exp\left\{-\frac{1}{2\sigma^2} \sum_{k=0}^{NL_0-1} \left|r\left(kT_2\right) - s\left(kT_2; \underline{\mathbf{a}}, \eta\right)\right|^2\right\}, \tag{2.18}$$

where $s\left(kT_2; \underline{\mathbf{a}}, \eta\right)$ symbolizes that the signal $s\left(kT_2\right)$ depends on the symbol sequence $\underline{\mathbf{a}}$ and the ratio η. The log-likelihood function is obtained by applying the logarithm to (2.18):

$$\Lambda\left(\underline{\mathbf{a}}, \eta\right) = -\frac{L_0 N}{2} ln\left(2\pi\sigma^2\right) - \frac{1}{2\sigma^2} \sum_{k=0}^{NL_0-1} \left|r\left(kT_2\right)\right|^2 - 2r\left(kT_2\right) s\left(kT_2\right) + \left|s\left(kT_2\right)\right|^2. \tag{2.19}$$

Note that the first term does not depend on η, and the log-likelihood function can be rewritten as:

$$\Lambda\left(\underline{\mathbf{a}}, \eta\right) = -\frac{1}{2\sigma^2} \sum_{k=0}^{NL_0-1} \left|r\left(kT_2\right)\right|^2 - 2r\left(kT_2\right) s\left(kT_2\right) + \left|s\left(kT_2\right)\right|^2. \tag{2.20}$$

The derivative log-likelihood function is:

$$\frac{\partial}{\partial\eta}\Lambda\left(\underline{\mathbf{a}}, \eta\right) = -\frac{1}{2\sigma^2}\frac{\partial}{\partial\eta} \sum_{k=0}^{NL_0-1} \left|r\left(kT_2\right)\right|^2 - 2r\left(kT_2\right) s\left(kT_2\right) + \left|s\left(kT_2\right)\right|^2, \tag{2.21}$$

$$\frac{\partial}{\partial\eta}\Lambda\left(\underline{\mathbf{a}}, \eta\right) = -\frac{1}{2\sigma^2}\frac{\partial}{\partial\eta} \sum_{k=0}^{NL_0-1} -2r\left(kT_2\right) \sum_{n=0}^{L_0-1} a\left(n\right) p\left(\frac{1}{F_{s2}}\left(k - nN_1\eta\right)\right), \tag{2.22}$$

$$\frac{\partial}{\partial\eta}\Lambda\left(\underline{\mathbf{a}}, \eta\right) = \frac{1}{\sigma^2}\frac{\partial}{\partial\eta} \sum_{k=0}^{NL_0-1} r\left(kT_2\right) \sum_{n=0}^{L_0-1} a\left(n\right) p\left(\frac{1}{F_{s2}}\left(k - nN_1\eta\right)\right). \tag{2.23}$$

Equation (2.22) comes from replacing $s\left(kT_2\right)$ by (2.16) and observing that in (2.21) the first term inside the summation does not depend on η and the third term is assumed to be approximatedly 0.

Interchanging the order of summation, (2.23) becomes

$$\frac{\partial}{\partial\eta}\Lambda\left(\underline{\mathbf{a}},\eta\right)=\frac{1}{\sigma^2}\sum_{n=0}^{L_0-1}a\left(n\right)\sum_{k=0}^{NL_0-1}r\left(kT_2\right)\dot{p}[\frac{1}{F_{s2}}\left(k-nN_1\eta\right)]\left(-n\frac{N_1}{F_{s2}}\right). \tag{2.24}$$

Note that the second summation,

$$\sum_{k=0}^{NL_0-1}r\left(kT_2\right)\dot{p}[\frac{1}{F_{s2}}\left(k-nN_1\eta\right)], \tag{2.25}$$

is recognized as the derivative-matched filter ouput, $\dot{x}\left(\frac{n\eta}{F_{s2}}\right)$. Thus, (2.24) becomes:

$$\frac{\partial}{\partial\eta}\Lambda\left(\underline{\mathbf{a}},\eta\right)=\frac{1}{\sigma^2}\sum_{n=0}^{L_0-1}a\left(n\right)\dot{x}\left(\frac{n\eta}{F_{s2}}\right)\left(-n\frac{N_1}{F_{s2}}\right). \tag{2.26}$$

The maximum likelihood sampling frequency ratio estimate is the value of η that maximizes the log-likelihood function. The ML estimate $\hat{\eta}$ is the value of η that drives the following equation to zero:

$$\sum_{n=0}^{L_0-1}a\left(n\right)\dot{x}\left(\frac{n\eta}{F_{s2}}\right)\left(n\frac{N_2}{F_{s2}}\right)=0. \tag{2.27}$$

Note that this derivation was performed for the data-aided case. Proceeding in a similar way, the ML sampling frequency ratio estimate for the non-data-aided case is obtained:

$$\sum_{n=0}^{L_0-1}\hat{a}\left(n\right)\dot{x}\left(\frac{n\eta}{F_{s2}}\right)\left(n\frac{N_2}{F_{s2}}\right)=0. \tag{2.28}$$

2.4 Architecture of Sampling Frequency Ratio Error Detector

After deriving a formulae to find $\hat{\eta}$, a similar procedure to that detailed in Sec. 1.3 for building the TED is used. The error signal that drives the estimation of the sampling frequency ratio is obtained in (2.28). The sampling frequency ratio recovery system is thus a feedback circuit with a PLL structure driven by this error signal.

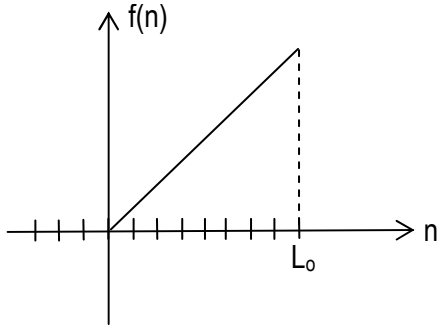

Fig. 2.5: Loop filter impulse response.

In the timing error case (1.21), the sum obtained at the ML estimate derivation represented a low pass filter applied to the timing error signal:

$$\sum_{k=0}^{L_0-1} a\left(k\right) \dot{x}\left(\frac{k}{F_{s2}}+\tau\right)=0. \tag{2.29}$$

From (2.28), the sum on n is interpreted as a filter that works at the symbol rate on the error signal. The impulse response of this filter (Fig. 2.5) is defined by:

$$f\left(n\right)=n\left(u\left(n\right)-u\left(n-L_0\right)\right). \tag{2.30}$$

From this impulse response it can be infered that there are several parameters that influence the response of the loop filter and thus the behavior of the loop. Filter parameters such as offset, length or slope can be varied widely.

Recall from Sec. 2.2 that the trigger signal of the NCO is generated by η and that η was set as a known parameter in that structure. The control word $W\left(m\right)$ was, on average, equal to η. Now, the ML sampling frequency ratio estimate $\hat{\eta}$ is obtained in an adaptive way. The error estimate derived with the ML criteria and from (2.28) should drive η to its true value.

A complete structure for a baseband binary PAM receiver with a ML sampling frequency ratio error detector (Fig. 2.6) is obtained by incorporating this sampling frequency

ratio error detector (2.28) in the structure derived in Sec. 2.2.

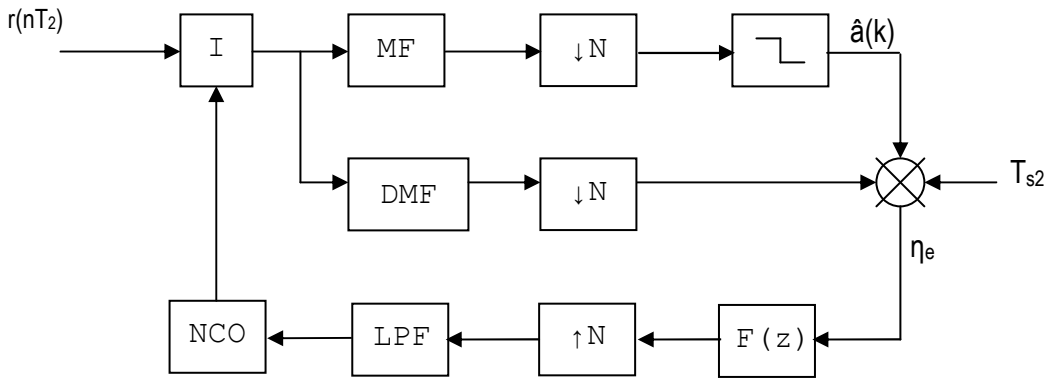

Fig. 2.6: Sampling frequencies ratio estimation for binary PAM.

Chapter 3

Feed Forward Architecture for Sampling Rate Estimation and Correction

This chapter presents a feed forward receiver structure designed to correct the sampling frequency offset between transmitter and receiver. First, the receiver obtains a rough estimate of the sampling frequency ratio η. Then, sampling frequency recovery interpolation is performed with this estimated η. Finally, the timing adjustment of the sampled signal is performed by a standard digital PLL receiver.

3.1 Feed Forward Spectral Estimation of η

As stated previously, a large sampling frequency offset must be corrected before estimating other unknown parameters (e.g., symbol timing, carrier phase and carrier frequency). An estimator of the sampling frequency offset that works independently of a standard receiver structure is developed in this section.

The estimation of η is obtained at the receiver from the information in the signal's frequency spectrum. The signal is assumed to be sampled at the transmitter at F_{s1} using N_1 samples per symbol. With these assumptions, the receiver calculates the expected spectral peak location. Using the receiver's sampling frequency F_{s2} and N_2 samples per symbol, the actual spectral peak is obtained. The value of η is simply the ratio of the expected and actual spectral peaks. A symbol synchronization sequence is transmitted before the data to help extract the actual spectral peak at the receiver. A buffer of the length of the synchronization sequence is defined in the receiver, this buffer introduces a delay of $\frac{L}{N}$ symbols to the detection process, where L is the length of the buffer and N is the number of samples per symbol. After the buffer is filled, a DFT is applied to the buffer's contents and the actual spectral peak is found (Fig. 3.1). Once a rough estimate of η is obtained,

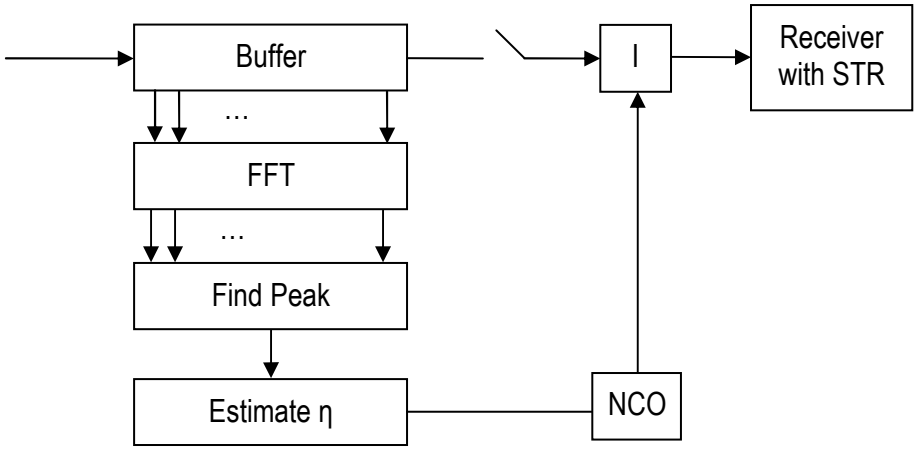

Fig. 3.1: Feed forward spectral estimator for η.

the interpolation function for sampling frequency recovery processes the data in the buffer.

The fixed estimate $\hat{\eta}$ is fed to an interpolation control unit to sample the incoming signal at approximately the transmitter's sampling rate. The interpolation control structure was described in Sec. 2.2, where an architecture for sampling rate correction that works with the correct η was presented.

The assumption of the transmitter parameters and the frequency resolution in estimating the actual spectral peak influence the error of the η estimation. For a finer frequency resolution the number of data points (in this case, the length of the synchronization sequence) must be increased. Conversely, to efficiently use the available transmission bandwith and transmitter power the length of the symbol synchronization sequence must be minimize and yet produce sufficiently accurate estimate of η.

The actual spectral peak may lie between two DFT samples. In general, zero padding is used to better characterize the spectrum of a signal [9]. However, zero padding fails to improve accuracy or resolution and an alternative algorithm, detailed in E. Jacobsen et al. [10], was used to find a more accurate frequency estimator. This algorithm refines the frequency estimation based on the samples of the DFT withouth increasing the DFT

size. To obtain a more accurate estimate of the location of the spectral peak, a fractional correction term, δ, is calculated and added to the integer peak index, k. The correction term is obtained through

$$\delta = -Re\left[\frac{(X_{k+1} - X_{k-1})}{(2X_k - X_{k-1} - X_{k+1})}\right], \tag{3.1}$$

where X_{k-1}, X_k and X_{k+1} are DFT samples, and X_k is the frequency-domain peak sample. Thus the peak location will be

$$k_{peak} = k + \delta, \tag{3.2}$$

and the frequency location of the peak is

$$f = \frac{k_{peak} F_s}{N_{DFT}}, \tag{3.3}$$

where F_s is the sampling frequency in Hz and N_{DFT} is the DFT size.

It is critical that the rough estimate of η be accurate enough to properly perform the timing recovery loop (second stage of this receiver architecture) as the STR circuit will only synchronize with a frequency offset of $\Delta f_{pull-in}$ (1.22).

If the bin spacing of the DFT is equated to the pull-in range $\Delta f_{pull-in}$, then

$$\frac{F_{s2}}{N_{FFT}} = bin\ spacing\ (Hz), \tag{3.4}$$

$$\frac{F_{s2}}{N_{FFT}} \approx \Delta f_{pull-in}, \tag{3.5}$$

$$N_{FFT} \approx \frac{F_{s2}}{\Delta f_{pull-in}}, \tag{3.6}$$

where N_{FFT} is the number of points in the DFT (or FFT) computation. Therefore a synchronization sequence of length N_{FFT} guarantees that the digital PLL of this receiver will lock.

3.2 Standard Digital PLL for Timing Recovery

The second stage of the receiver is a standard structure that performs demodulation, detection and digital PLL based symbol timing recovery in the presence of a residual sampling frequency offset. Recall that at the transmitter the relationship between symbol and sample rates is:

$$sample\ rate = N \times symbol\ rate, \tag{3.7}$$

$$\frac{1}{T} = N\frac{1}{T_s}. \tag{3.8}$$

Because the estimate $\hat{\eta}$, and not the true η, is used in this receiver structure, there is a small offset in the frequency of the resampled signal compared to the transmitter's sampling frequency. This difference can be stated as:

$$estimated\ sample\ rate \approx N \times symbol\ rate, \tag{3.9}$$

$$\frac{1}{T_\epsilon} = (N + \epsilon)\frac{1}{T_s}, \tag{3.10}$$

where ϵ is a small error associated with estimating η.

Therefore, the estimated sampling frequency is $\frac{\epsilon}{T_s}$ different from N samples/symbol and thus the desired samples will not be spaced at exactly T_s/N apart in the interpolation function. This residual timing error accumulation will be reflected in the behavior of the NCO parameters [3]. Note that the NCO and interpolation function performed at this stage are to recover the symbol timing as opposed to the interpolation performed intially to recover the sampling frequency.

To analyze the effects of ϵ on the receiver, recall from Sec. 2.1 that the control word is set to $W(n) = \frac{1}{N} + v(n)$. Since the error $v(n)$ is driven to zero by the PLL, $W(n)$ is on average equal to $\frac{1}{N}$. The control word $W(n)$ decrements by $\frac{1}{N}$ even when there is a sampling frequency offset (i.e., $T_s \neq NT_\epsilon$). At each instant the error, ϵ, increases and approaches the sample period T_ϵ. When $\epsilon > 0$ and $\epsilon = T_\epsilon$, the NCO produces a non-required trigger signal. Conversely, when $\epsilon < 0$ its absolute value will approach T_ϵ and when $|\epsilon| = T_\epsilon$, the

NCO trigger is suppresed. Both outcomes are undesirable because they produce errors in the detection of the signal.

Simultaneously to the trigger signal, the residual timing error also causes the fractional interval μ_k to continuously increase (or decrease). Similar to above, the sign of the error ϵ determines which case occurs. If $\epsilon > 0$, then $T_s > NT_\epsilon$ and μ_k increases and resets from a value of 1 to 0. In addition, an extra interpolant is calculated from the available matched filter output because a spurious trigger signal was produced. Because the extra interpolant interferes with the correct detection, a practical solution is to discard it and not update the timing error detector circuit.

Conversely, if $\epsilon < 0$ then $T_s < NT_\epsilon$ and μ_k decreases and resets from a value of 0 to 1. The trigger signal is not produced at the desired instant and the required interpolant is not calculated. To counteract the effect of this case a zero is "stuffed" to generate a timing error detector output and the circuit is updated with the "dummy" interpolant at that instant. The relationship between T_s and T_ϵ can be compared to the relationship between T_1 and T_2 in Fig. 2.2.

The receiver structure that uses the feed forward spectral estimator for η (Fig. 3.2) takes into account this residual sampling frequency offset scenario, and is built as follows: (1) the feed forward spectral estimator detailed in Sec. 3.1 calculates $\hat{\eta}$ based on the synchronization sequence, (2) the interpolation for clock frequency recovery is performed with this estimate $\hat{\eta}$ and (3) a standard digital PLL for timing recovery corrects the residual sampling frequency offset.

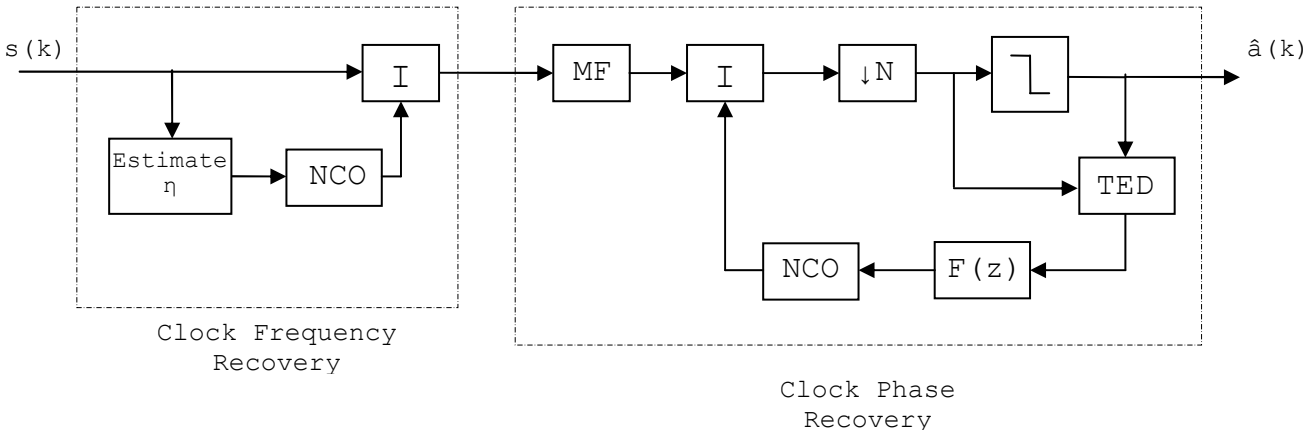

Fig. 3.2: Receiver structure with feed forward spectral estimator for η.

Chapter 4

Results

This chapter presents the results of implementing the receiver structures detailed in Chapters 2 and 3. The performance of the proposed structures were evaluated through computer simulations. The simulations where implemented in Matlab using: 7000 random symbols, 4 samples per symbol, frequency ratios of 0.90 up to 0.99 with $F_{s1} = 8000$ Hz, noise variance of 5×10^{-3}, SRRC pulse with 50% excess bandwith and pulse trunctation $L_p = 6$ to expand $2L_p + 1$ symbols.

4.1 Receiver with ML Sampling Frequency Ratio Estimator

The receiver structure detailed in Chapter 2 was implemented with the parameter η initialized to 1 (i.e., $F_{s1} = F_{s2}$) because the sampling frequencies are assumed to be very similar. In addition, other values of η near the true value were used as initialization values to test the behavior of the estimator. The loop filter (described in eq. 2.30) is a low pass filter with a frequency response shown in Fig. 4.1. The filter's parameters (length, offset and slope) were varied in a trial/error way to determine which combination best drove the error to zero.

The receiver structure with ML sampling frequency ratio estimator failed to drive η to zero as derived in Sec. 2.3. The parameter η stayed in the assigned initial value with a variance proportional to the filtered loop error. It was therefore not possible to succesfully estimate η from the incoming signal in any of the simulations.

One reason this structure could not succesfully estimate η is because the ML estimation depends on a priori knowledge of the true symbols a_n; instead, the estimated symbols $\hat{a}_n$ were used. However to use the known a_n, the signal timing information must be known, which in this case it is not. With a timing offset the true symbols are used at the receiver

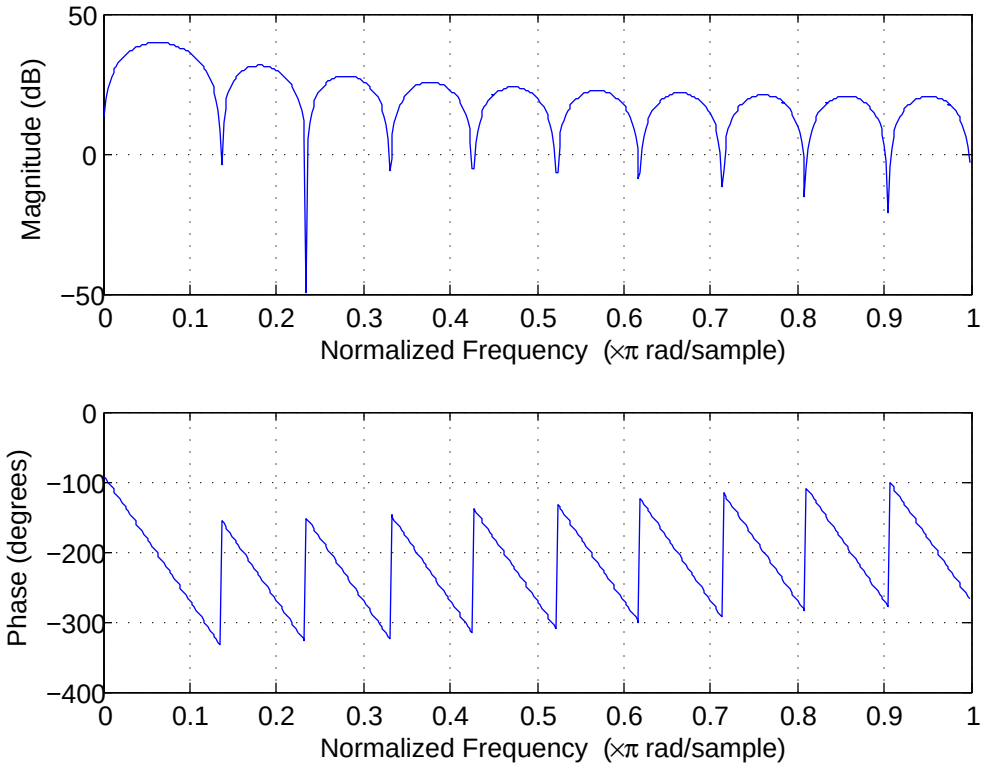

Fig. 4.1: Loop filter frequency response. In this case a loop filter with $f(n) = [-10 : 10]$.

but not at the correct time. As a consequence, when estimating η, samples of a previous or next symbol (depending on the sampling frequencies relationship) are used with a current known symbol.

The assumptions made when implementing the loop filter affect the ML estimation. In this simulation the parameters (oscillator sensitivity K_o and detector gain K_p) derived in M. Rice [3] for ML TED were used to estimate the loop filter parameters. Additional analysis of the loop error transfer function and the expected value of the error signal (S-curve) for this sampling rate error detector are needed to estimate more accurate loop filter parameters.

4.2 Receiver with Feed Forward Spectral Estimator

The receiver with feed forward spectral estimator was implemented using the MLTED loop filter parameters $K_p = 0.235$, $K_o = -\frac{1}{N_2}$ and $\zeta = \frac{1}{\sqrt{2}}$. The length of the synchronization sequence was set to $N_{FFT} = 2^{10}$ to perform the FFT. When the receiver assumed transmitter parameters (F_{s1}, N_1) that were equal or approximately equal to the actual parameters, the receiver structure successfully recovered the signal's information. In addition, correct detection of signal information was possible only when $\hat{\eta}$ generated a sampling rates difference within the permissible range $\Delta f_{pull-in}$. Values of η as low as 0.90 where tested (a sampling frequencies difference of approximately 800 Hz).

The behavior of the receiver with feed forward spectral estimator is shown in the presence of a sampling frequency offset of 400 Hz (Figs. 4.2 - 4.4). Frequencies $F_{s1} = 8000$ Hz and $F_{s2} = 7600$ Hz were assumed ($\eta = 0.95$). The receiver structure calculates the anticipated spectral peak assuming $F_{s1} = 8000$ Hz and $N_1 = 4$ samples per symbol, the rough estimate obtained is $\hat{\eta} = 0.948148$. The pull in range is defined to be $\Delta f_{pull-in} = 20$ Hz and the STR circuit corrects the error introduced from using $\hat{\eta}$, that in this case is approximately 16 Hz. The behavior of the loop filtered error and the fractional interval are shown in Figs. 4.2 and 4.3, respectively. As expected, the fractional interval continuously wraps around from a value of 1 to 0 to counteract the effect of ϵ in equation (3.10). The eye diagram and scatter plot (Fig. 4.4) show that the receiver structure correctly recovered

the information.

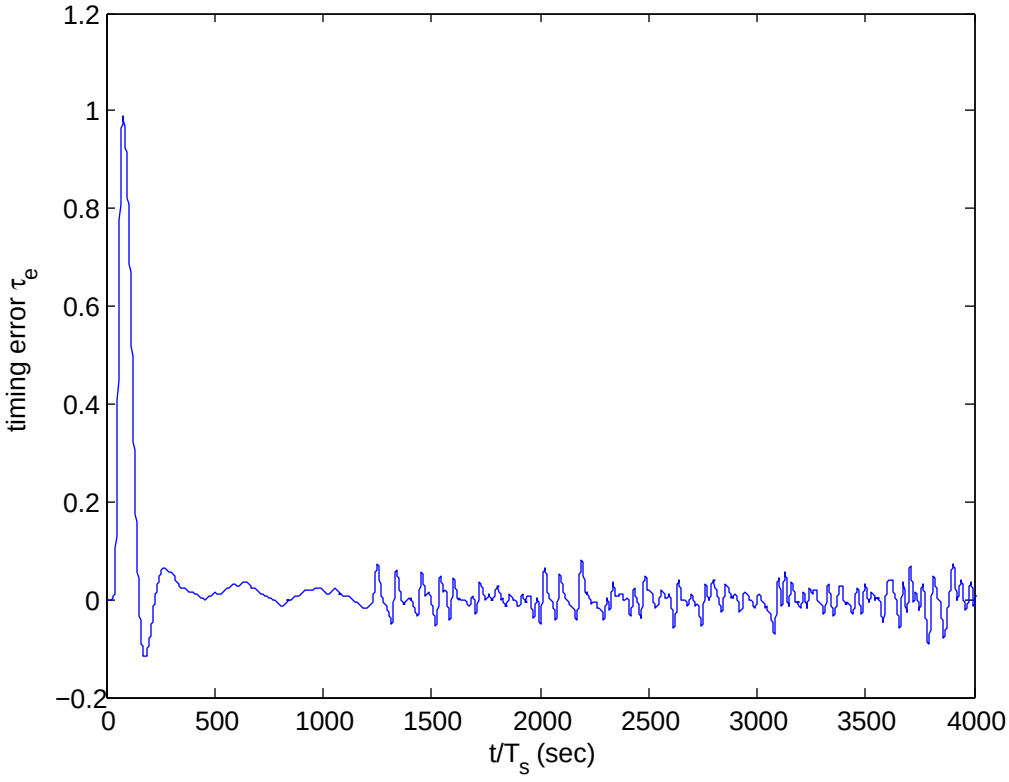

Fig. 4.2: Loop filtered timing error.

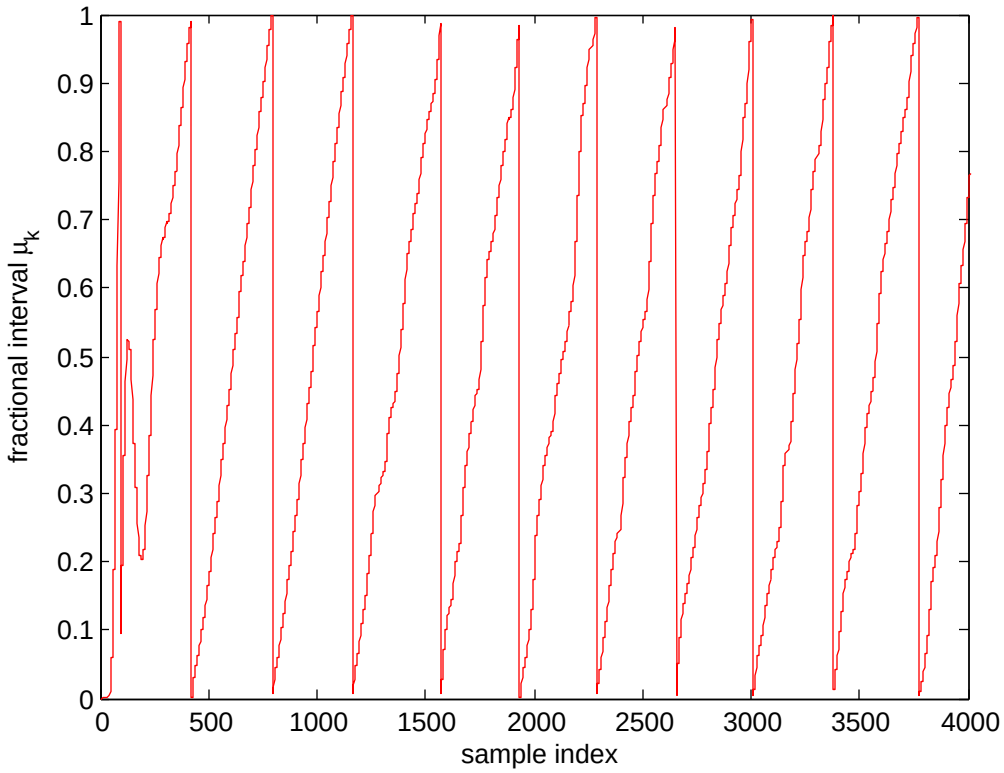

Fig. 4.3: Second stage fractional interval μ_k.

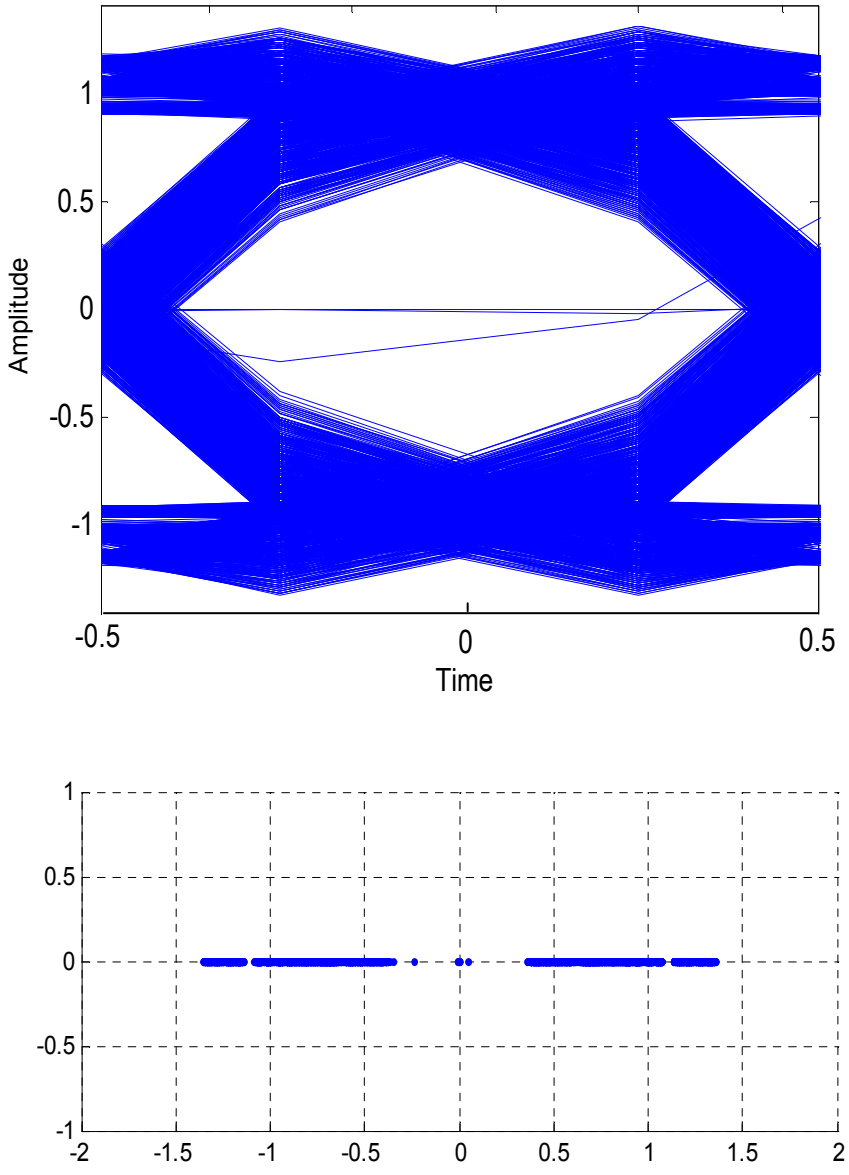

Fig. 4.4: Eye diagram (top) and Scatter plot (bottom).

Chapter 5

Conclusions

A summary of the contributions of this thesis and potential future work are discussed.

5.1 Summary

The mathematical expression of the effect of a sampling frequency offset on a baseband binary PAM signal was established. The expression was used to analyze the problem of synchronization in the presence of a clock frequency offset. A digital receiver structure, based on interpolation concepts, was presented that corrects the sampling frequency offset when the correct η is known. Two receiver structures that estimate the ratio η where designed. First, an estimator for the sampling frequency ratio was derived using the ML optimum criteria. This estimator lead to the design of a feedback receiver structure to extract the sampling frequency ratio error. This estimator did not drive the η error to zero as it was implemented here. The second structure presented was a feed forward estimator of the sampling frequency ratio that relies on the information in the spectrum of the signal to estimate the ratio η. The estimator depends on the assumption of specific transmitter parameters and a synchronization sequence. It is independent from a standard digital PLL based receiver.

5.2 Future Work

This research creates new opportunities for study. The receiver structure developed here corrected the sampling frequency offset of the signal and can be used with any circuit that detects the sampling frequency ratio. Therefore, other sampling frequency ratio detectors or error detectors can be explored mathematically and in an ad-hoc manner. Further research on the behavior of the ML estimator is needed because it failed to estimate the

error and detect the incoming signal information. The loop filter for the ML sampling rate error detector should be analyzed in detail in order to derive more accurate filter parameters. An analysis of the implementation and behavior of higher order loop filters could be of interest since it has been shown [11] that the order of the prediction error filter influences the accuracy of the frequency estimation error.

An alternative approach to those presented here may be a standard digital PLL based receiver structure with adaptive parameters. This structure could be initialized with a large $\Delta f_{pull-in}$ and the parameters designed to adapt to the right pull-in range. In addition, other receiver structures that recover the sampling frequency but are not based on the ratio of the clock frequencies could be explored. The performance of synchronizers under a small clock frequency offset have been analyzed in M. Rice [1], but the performance of synchronizers under a larger clock frequency offset and in the presence of a sampling frequency recovery circuit could be explored. Finally, these derivations can be extended to other linear modulation schemes and higher order constellations.

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