BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

CSE 306

Computer Architecture Sessional

Name of the experiment: 4-bit ALU Simulation

Level/Term : **3/1**

Group : **6**

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Introduction :

An arithmetic unit or ALU is one of the most important parts of CPU. It is a simple binary calculator. It can perform binary addition or subtraction and more other arithmetic and logical operation on two inputs. In this experiment, we have to design an ALU according to design specification

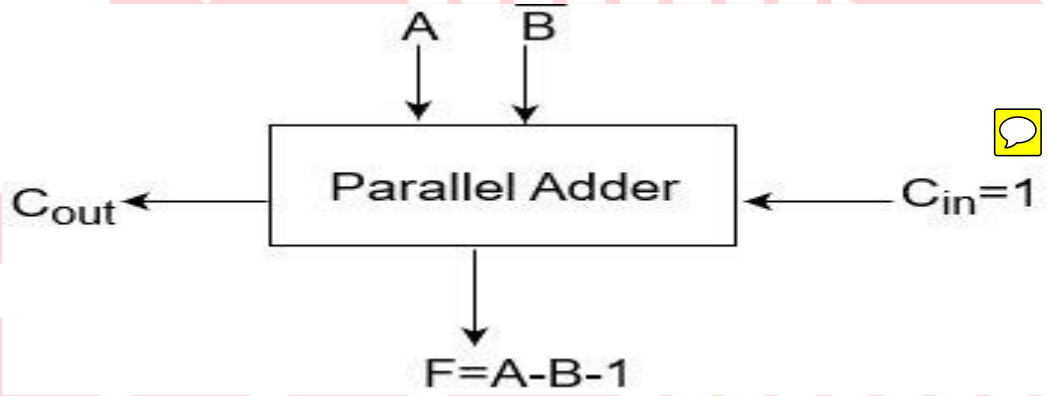
Problem Specification :

cin			Functions
cs2	cs1	cs0	
0	0	0	Subtract with borrow
0	1	0	Decrement A
1	0	0	Subtract
1	1	0	Transfer A
x	0	1	AND
x	1	1	Complement A

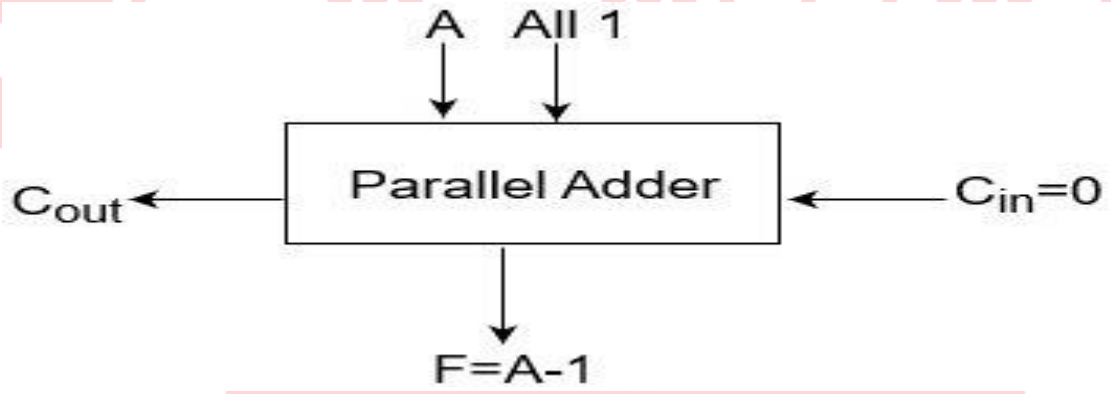
Arithmetic Part :

When cs0 = 0 Arithmetic part will be activated

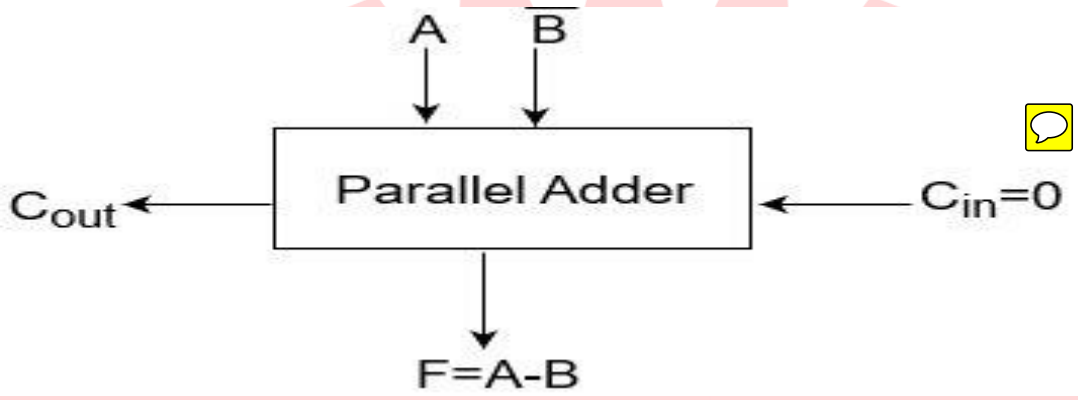
(a) Subtract with borrow



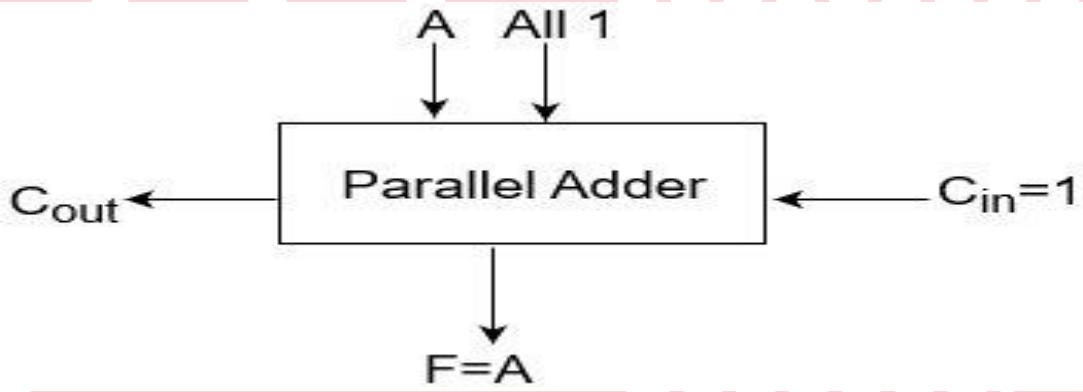
(b) Decrement A



(c) Subtract



(d) Transfer A

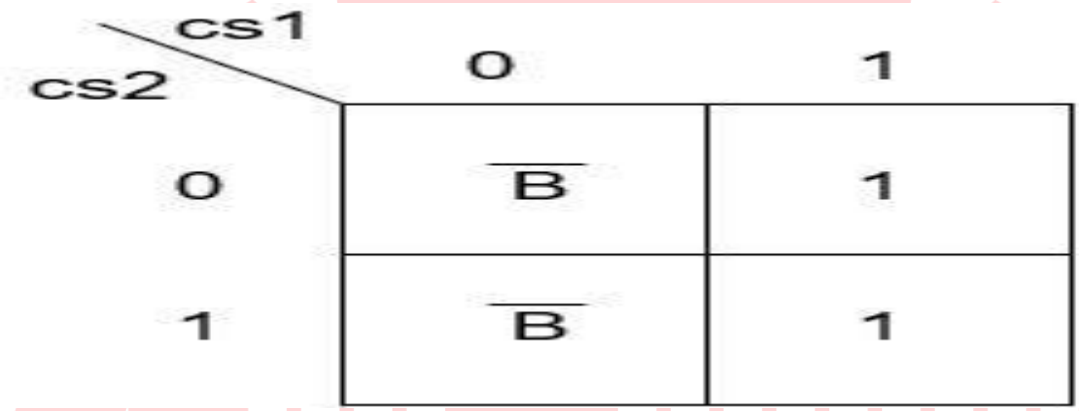


Truth Table :

cs2	cs1	X	Y
0	0	A	B’
0	1	A	All 1
1	0	A	B’

1	1	A	All 1

K-Map : for Y,



So, from K-Map Y= B' + cs1 and from Trurh Table X=A

Logical Part :

When cs0 =1 Logical part will be activated. At this time , cs2 is don't care. We can make Cin =0 forcefully for each adder by taking Cin=cs0'cs2 for first full adder and Cin=cso'Cout for other full adder.

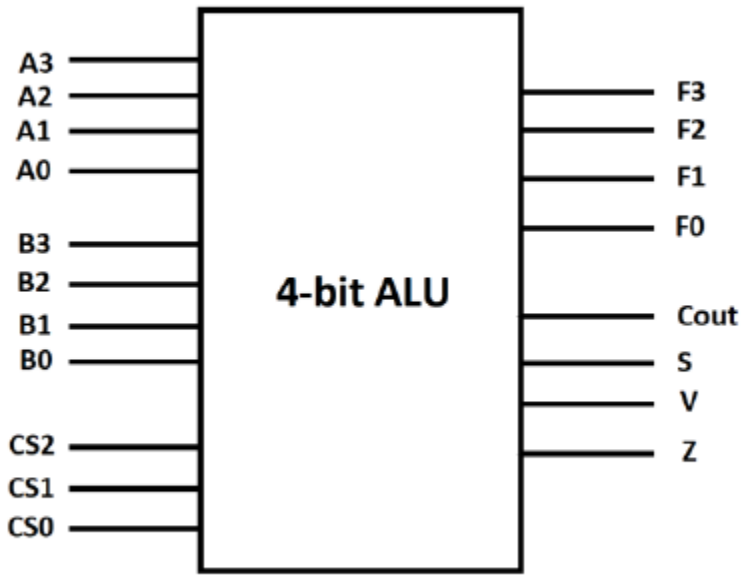
cs2	cs1	cs0	x	y	Cin	Function	Required Operation
x	0	1	A	B'	0	$A \oplus B'$	AND

x	1	1	A	1	0	A’	Complement A

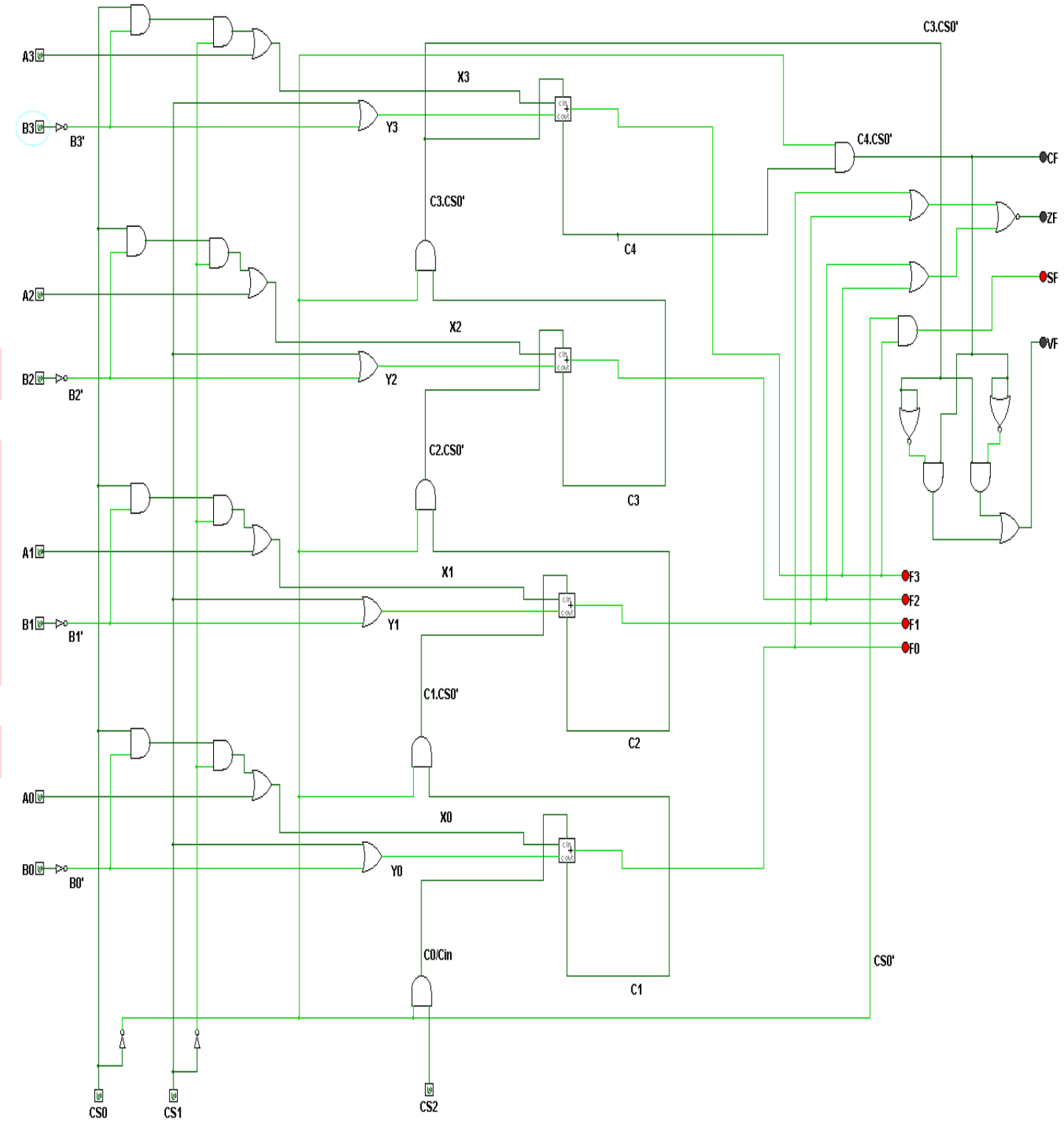
We get required result in the second case. But in the first case we get A ⊕ B’ in lieu of AB. We can easily get this if we give X= A V B’ in this case.
So,

X= A+ B’cs0cs1’

BLOCK DIAGRAM :



Complete Circuit Diagram :



ICs used with count as a chart:

GATE	Count of Gates	IC Number	Count of IC'S
AND	16	IC74LS08	4
OR	11	IC74LS32	3
NOT	6	IC74LS04	1
NOR	3	IC74LS02	1
4-bit full Adder	4	IC74LS83	4

Simulator Used along with the version number:

The simulator used in this 4-bit ALU simulation experiment is "logisim-win-2.7"

Discussion:

In this experiment, we used cs0 as the selection bit to choose arithmetic or logical operation and cs2 as Cin. For 4-bit ALU simulation, it was required to use 1-bit full Adder. But we used 4-bit full Adder because 1-bit full adder is not available and we tried to use minimum number of IC'S. Cout of each full Adder was handled as per the operation. The inputs and the flags were designed as design specification.