Department of Electronics and Electrical Engineering

EE101, Quiz 6 Timings: 8:00 – 9:30 AM

27 February 2021

Duration: 90 minutes

Total Marks:14

Instructions:

All Questions are to be answered

Enter the solutions up to two decimal points.

Units and signs have to be mentioned with the answers.

Evaluation will be based on the submitted answer sheets only.

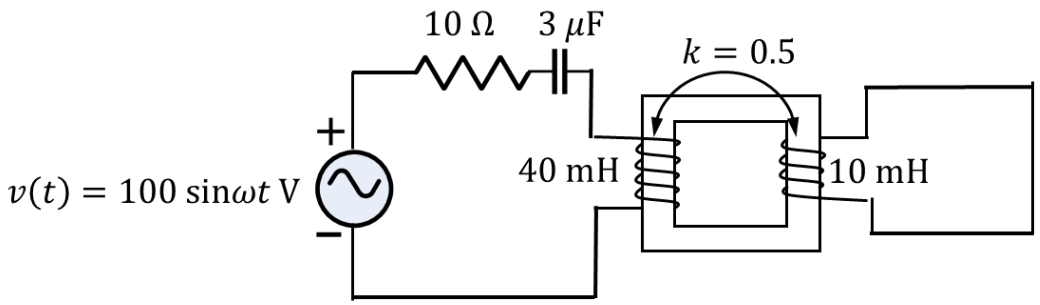
Start a new question on a fresh page

Answer all part of the question together, failing which the answers of that question won't be evaluated.

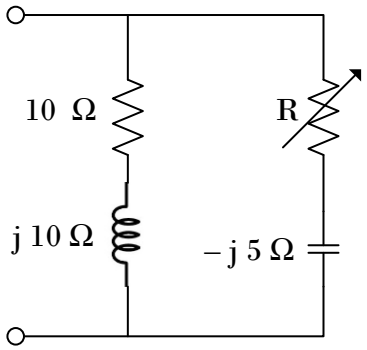
On every page of the answer sheet, students must mention their name, roll number. Page number should also be mentioned at the top right corner of the answer sheet.

Q1. Determine [5]

(a) The value of the resonant frequency (f_0) in Hz and
(b) The magnitude of the impedance seen from the source at half power frequencies for the network shown below.
(c) The type of filter, if the output will be taken across the 10 W resistor. Give justification with amplitude-frequency plot.



Q2. For the parallel network shown in figure, find the value of R for resonance. [2]



Q3. Consider a synchronous sequential circuit consisting of two D-type flip flops. Assume that initial state of circuits is 00. The partially filled state table of that circuit is given below for four clock cycles. Give the completely filled state table. (Symbol y' denote the complement of logic variable y) [1]

Present state		Flip-flip inputs		Next state	
Q0	Q1	D0=(Q0+Q1)'	D1=Q0'	Q0	Q1
0	0				

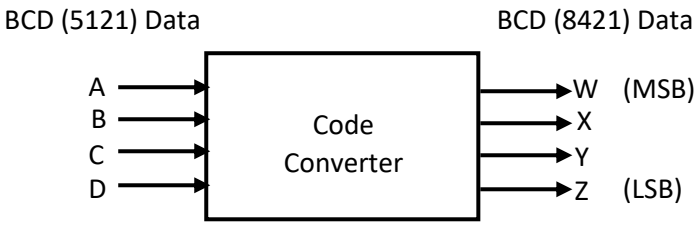
Q4. The skeleton of the excitation table of a synchronous sequential circuit having states (AB), input (x) and output (z) is shown below. Let the state 'A' be implemented using a T flip-flop and the state 'B' be implemented using a SR flip-flop. Given the completed excitation table. Also deduce the minimized expressions for flip-flip inputs and the output (z).

[2]

Present state		Input	Next state		Flip-flop inputs			Output
A	B	X	A	B				Z
0	0	0	0	1				1
0	0	1	1	0				1
0	1	0	0	0				0
0	1	1	1	1				0
1	1	0	0	0				0
1	1	1	0	1				0
1	0	0	0	0				1
1	0	1	0	1				1

Q5. A 'code converter' is to be designed to convert from the BCD (5121) code to normal BCD (8421) code. The input BCD combinations for each digit are given below. A block diagram of the converter shown in figure. Give the minimized expressions for code converter outputs. [2]

Decimal	BCD (5121)			
	A	B	C	D
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	1	1
5	1	0	0	0
6	1	0	0	1
7	1	0	1	0
8	1	0	1	1
9	1	1	1	1

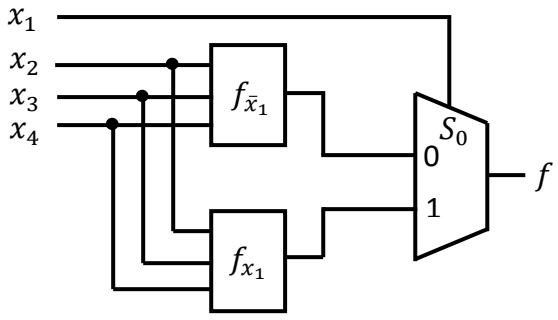


Q6. Realize the Boolean function

$$f(w_1, w_2, w_3, w_4, w_5) = w_1\overline{w}_2 w_4 + \overline{w}_1\overline{w}_4 + \overline{w}_1\overline{w}_3 w_4\overline{w}_5 + w_1 w_4\overline{w}_5 + w_1\overline{w}_2\overline{w}_3\overline{w}_4$$

using a 4-to-1 multiplexer and as few other gates as possible. Assume that only the uncomplemented inputs are available. [2]

Hint: Use Shannon expansion theorem. Note, a four variable function $f(x_1, x_2, x_3, x_4)$ can be expanded with respect to (say) x_1 as $f(x_1, x_2, x_3, x_4) = \bar{x}_1 f_{\bar{x}_1} + x_1 f_{x_1}$ where $f_{\bar{x}_1}$ and f_{x_1} denote the simplified expressions corresponding to $f(0, x_2, x_3, x_4)$ and $f(1, x_2, x_3, x_4)$, respectively. The expanded function can be realized using a 2-to-1 multiplexer as shown below.



For realizing the function with 4-to-1 multiplexer, we need to expand the function with respect to chosen two variables (say) x_1 and x_2 as given below:

$$f(x_1, x_2, x_3, x_4) = \bar{x}_1\bar{x}_2 f_{\bar{x}_1\bar{x}_2} + \bar{x}_1 x_2 f_{\bar{x}_1 x_2} + x_1\bar{x}_2 f_{x_1\bar{x}_2} + x_1 x_2 f_{x_1 x_2}$$