

1) Representar a tabela verdade das expressões abaixo:

a.  $S = \overline{A.B} + \overline{A(B+C)} + \overline{BC}$

A	B	C				
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

b.  $S = A.[\overline{(B+C)} + \overline{(A+B)}]$

A	B	C				
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

c.  $S = \overline{\overline{A.B.C}} + \overline{\overline{A.B.C}}$

A	B	C				
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

d.  $S = \overline{\overline{A+C}} + \overline{\overline{B}} + \overline{(A.B)}$

A	B	C				
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

e.  $S = (\overline{\overline{A.C}} + D + \overline{\overline{A.B}})$

A	B	C	D				
0	0	0	0				
0	0	0	1				
0	0	1	0				
0	0	1	1				
0	1	0	0				
0	1	0	1				
0	1	1	0				
0	1	1	1				
1	0	0	0				
1	0	0	1				
1	0	1	0				
1	0	1	1				
1	1	0	0				
1	1	0	1				
1	1	1	0				
1	1	1	1				

f.  $S = \overline{\overline{A.B.CD}} + \overline{\overline{A.B.CD}} + \overline{\overline{A.B.CD}} + \overline{\overline{A.B.CD}}$

A	B	C	D				
0	0	0	0				
0	0	0	1				
0	0	1	0				
0	0	1	1				
0	1	0	0				
0	1	0	1				
0	1	1	0				
0	1	1	1				
1	0	0	0				
1	0	0	1				
1	0	1	0				
1	0	1	1				
1	1	0	0				
1	1	0	1				
1	1	1	0				
1	1	1	1				

g.  $S = (\overline{A+B}).\overline{C} + \overline{D.(C+B)}$

A	B	C	D				
0	0	0	0				
0	0	0	1				
0	0	1	0				
0	0	1	1				
0	1	0	0				
0	1	0	1				
0	1	1	0				

0	1	1	1				
1	0	0	0				
1	0	0	1				
1	0	1	0				
1	0	1	1				
1	1	0	0				
1	1	0	1				
1	1	1	0				
1	1	1	1				

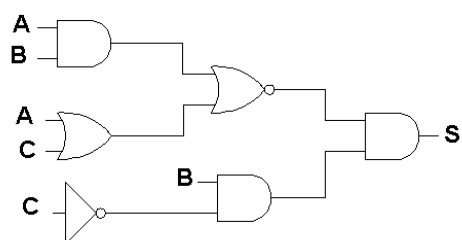
h.  $S = \overline{A}\overline{B}\overline{C} + A\overline{B}\overline{C}.D + A\overline{B}\overline{C}$

A	B	C	D				
0	0	0	0				
0	0	0	1				
0	0	1	0				
0	0	1	1				
0	1	0	0				
0	1	0	1				
0	1	1	0				
0	1	1	1				
1	0	0	0				
1	0	0	1				
1	0	1	0				
1	0	1	1				
1	1	0	0				
1	1	0	1				
1	1	1	0				
1	1	1	1				

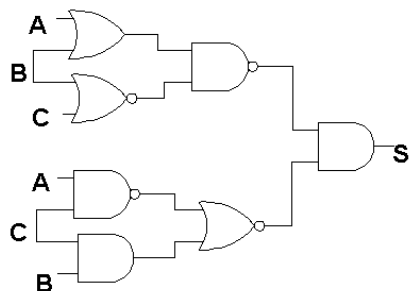
2) Desenhar o diagrama de portas lógicas para cada uma das expressões do exercícios anterior.

3) Escrever a expressão booleana correspondente aos diagramas abaixo:

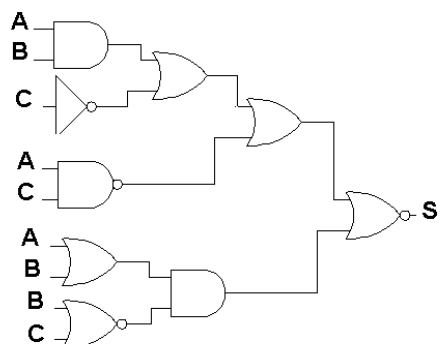
a)



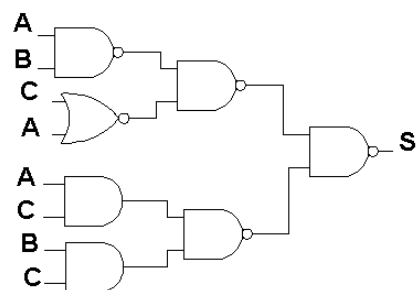
b)



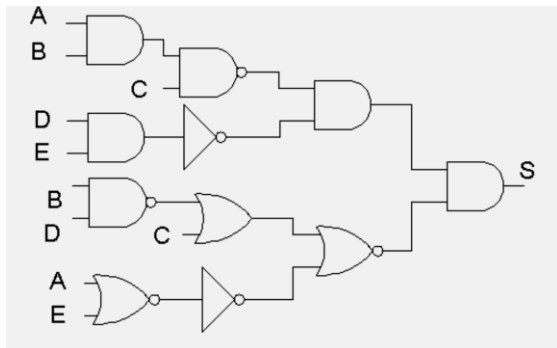
c)



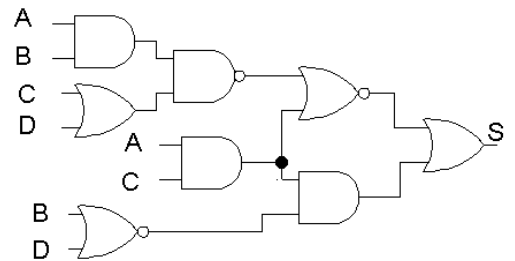
d)



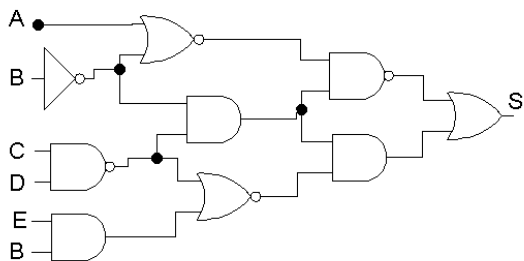
e)



f)



g)



4) Obter a tabela verdade de cada um dos circuitos da questão anterior.

5) Para cada tabela verdade abaixo, obter o circuito lógico correspondente na forma de soma de mintermos.

a)

A	B	C	S
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

b)

A	B	C	S
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

c)

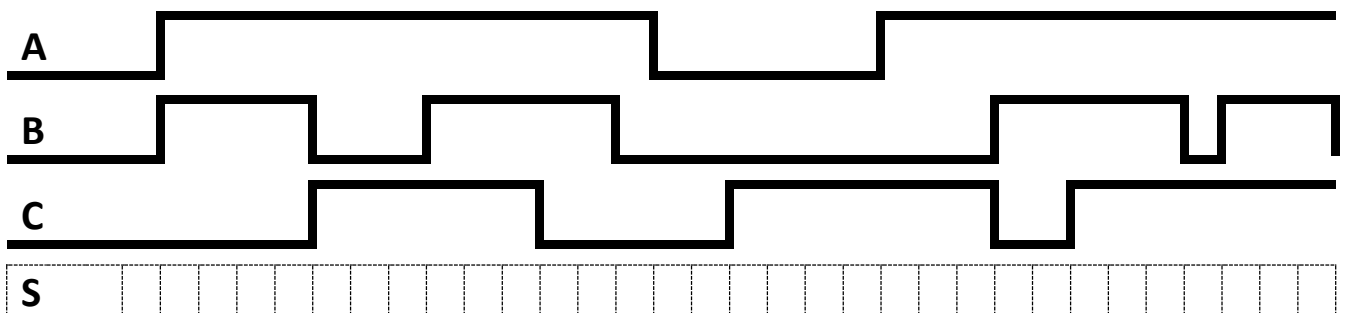
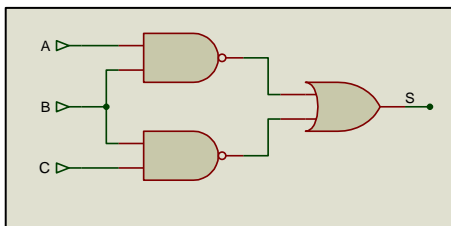
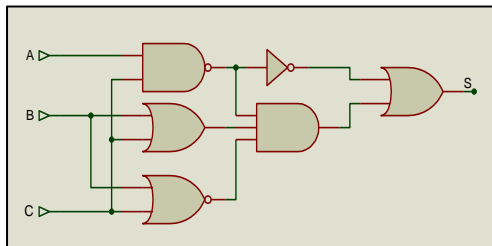
A	B	C	S
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

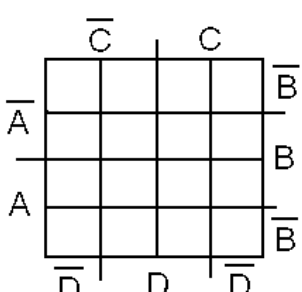
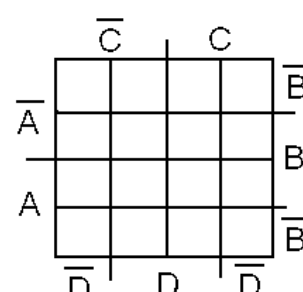
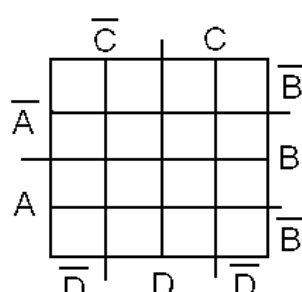
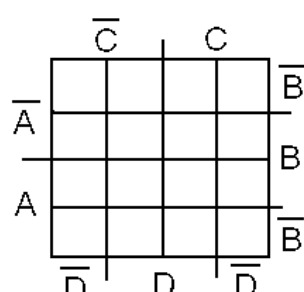
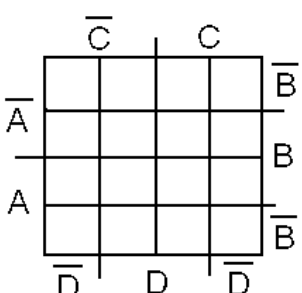
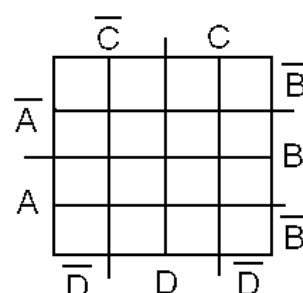
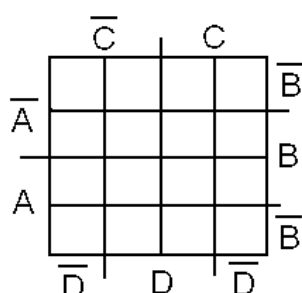
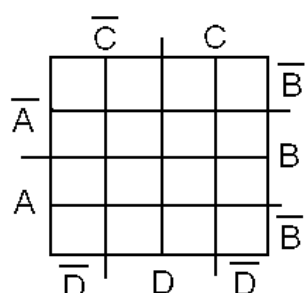
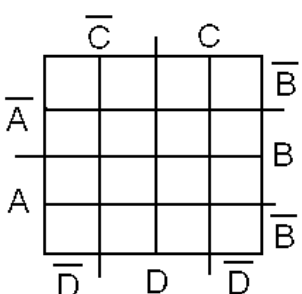
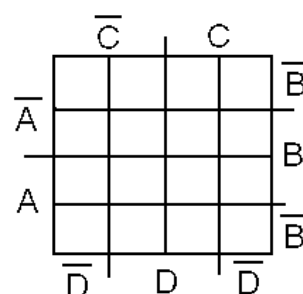
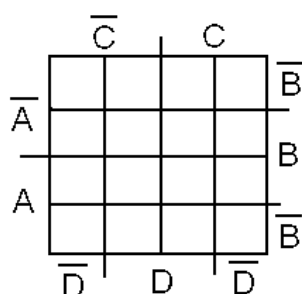
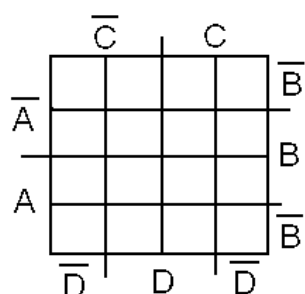
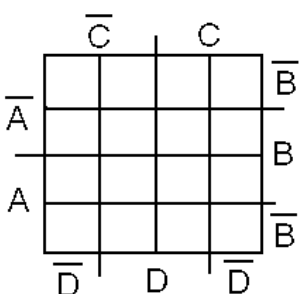
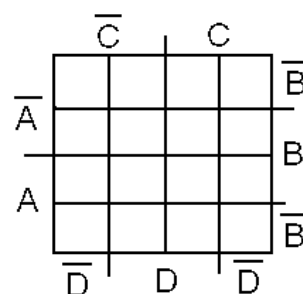
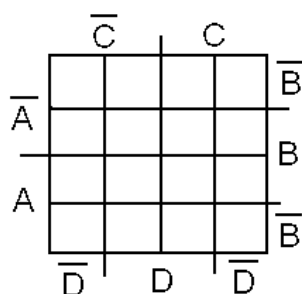
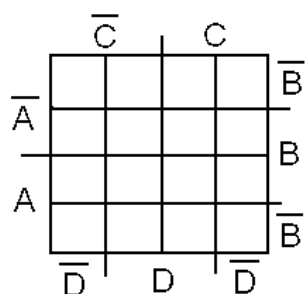
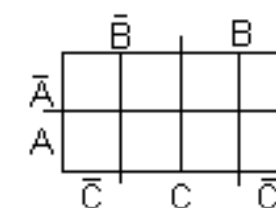
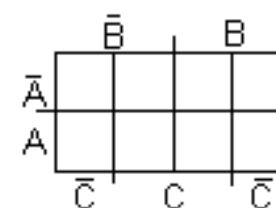
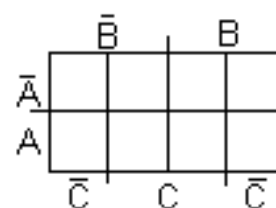
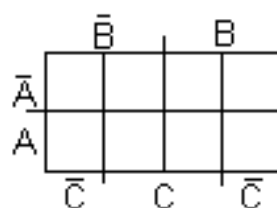
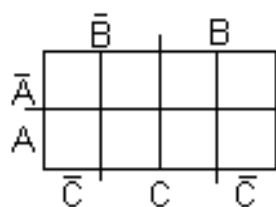
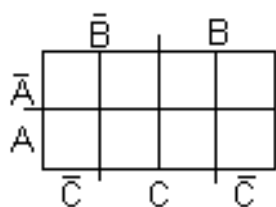
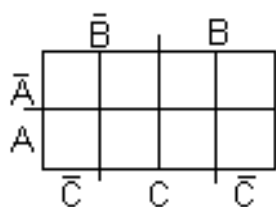
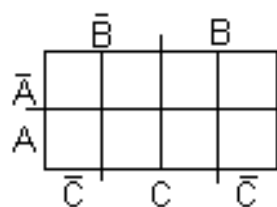
d)

A	B	C	S
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

6) Desenhar o diagrama de formas de onda para os circuitos abaixo:

The diagram shows a logic circuit with three inputs: A, B, and C. The circuit consists of three logic gates: two 2-input gates and one 3-input gate. The first 2-input gate is an AND gate with inputs A and B. Its output is connected to a NOT gate. The second 2-input gate is an OR gate with inputs A and B. The output of the NOT gate and the output of the OR gate are connected to the two inputs of the 3-input AND gate. The third input of the 3-input AND gate is input C. The output of the 3-input AND gate is labeled S.





A	B	C				
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

A	B	C				
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

A	B	C				
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

A	B	C				
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

A	B	C				
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

A	B	C	D				
0	0	0	0				
0	0	0	1				
0	0	1	0				
0	0	1	1				
0	1	0	0				
0	1	0	1				
0	1	1	0				
0	1	1	1				
1	0	0	0				
1	0	0	1				
1	0	1	0				
1	0	1	1				
1	1	0	0				
1	1	0	1				
1	1	1	0				
1	1	1	1				

A	B	C	D				
0	0	0	0				
0	0	0	1				
0	0	1	0				
0	0	1	1				
0	1	0	0				
0	1	0	1				
0	1	1	0				
0	1	1	1				
1	0	0	0				
1	0	0	1				
1	0	1	0				
1	0	1	1				
1	1	0	0				
1	1	0	1				
1	1	1	0				
1	1	1	1				

A	B	C	D				
0	0	0	0				
0	0	0	1				
0	0	1	0				
0	0	1	1				
0	1	0	0				
0	1	0	1				
0	1	1	0				
0	1	1	1				
1	0	0	0				
1	0	0	1				
1	0	1	0				
1	0	1	1				
1	1	0	0				
1	1	0	1				
1	1	1	0				
1	1	1	1				