Sichuan University Quiz

(Closed Book)

(2019-2020 Academic Year 1stDECEMBER) Quiz-2

课程号 Course Number: 304131030-04　　课程名称 Course Title: Digital Logic
任课教师 Lecturer: Xuedong Yuan　　考试时间 Time Period: 70 minutes
学生姓名 Name:　　学号 Student ID:　　成绩 Total Mark:

考生承诺

Student Commitment

我已认真阅读并知晓《四川大学考场规则》和《四川大学本科学生考试违纪作弊处分规定（修订）》，郑重承诺：

I have read and comprehendedthe“Regulations of Sichuan University on Examinations”. I give my commitments as follows:

1、已按要求将考试禁止携带的文具用品或与考试有关的物品放置在指定地点；

1. I have put prohibited stationary and exam-related items at designated area as required.

2、不带手机进入考场；

2. I have not brought cell phone to the examination room.

3、考试期间遵守以上两项规定，若有违规行为，同意按照有关条款接受处理。

3. During the examination, I will comply with the above two provisions. If there is any violation, I agree to accept the punishments in accordance with the relevant provisions.

考生签名：

Signature:

题号	一(20%)	二(20%)	三(60%)	四(0%)	五(0%)
得分					
卷面总分		教师签名		阅卷时间	

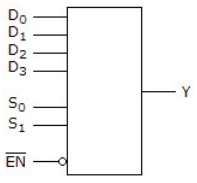
Notice: 1. Please write your student ID and your name in both exam papers and added answer papers precisely;

2.Please write all your answers on this exam paper;

3.After the exam, please hand in exam paper, added answer sheet and scratch papers to examiners all together.

评阅教师	得分

一、填空题 Fill in the blanks（本大题共 10 空，每空 2 分，共 20 分）。



1. For the device shown here, let all D inputs be LOW, both S inputs be HIGH, and the $\overline{EN}$ input be LOW. What is the status of the Y output?_____

2. A half-adder is characterized by _____ input(s) and ____ output(s).

3. Two 4-bit binary numbers (1011 and 1111) are applied to a 4-bit parallel adder. The carry input is 1. the values for the sum and carry output are $\Sigma_4\Sigma_3\Sigma_2\Sigma_1$=_____, C_{out}=_____.
4. How many inputs would two 8-line-to-3-line encoders, expanded to a 16-line-to-4-line encoder, have_____.
5. To implement the Boolean expression Y=A'B'C'+A'B'C+ABC+AB'C, it requires ____ 2-input-AND-GATE and ____ 2-input-OR-GATE.
6. The inputs to a full adder are A = ____ , B = 0, C_{in} = 1. The outputs are ____, C_{out} = 0.

评阅教师	得分

二、判断题 True/False Questions（本大题共 10 空，每空 2 分，共 20 分）。

_____ 1. When the input bits are both 1 and the input carry bit is 1, the sum output of a full adder is 1.

_____ 2. The 4-line-to-10-line decoder and the 1-of-10 decoder are two different types.

_____ 3. An encoder essentially performs a reverse decoder function.

_____ 4. AND-OR logic can have only two 2-input AND gates.

_____ 5. If the inputs of an exclusive-OR gate are the same, the output is LOW (0).

_____ 6. NAND gates can be used to produce the AND functions.

_____ 7. NOR gates cannot be used to produce the OR functions.

_____ 8. Negative-OR is equivalent to NAND.

_____ 9. A multiplexer is a logic circuit that allows digital information from a single source to be routed onto several lines.

_____ 10. The dual symbol for a NAND gate is a negative-AND symbol.

评阅教师	得分

三、问答题 Question and Answer（本大题共 3 小题，共 60 分）。

1. (1) Optimize the functions $f(a,b,c,d) = \Sigma m(0,13,14,15) + \Sigma d(1,2,3,9,10,11)$ in a minimum sum-of-products expression using a Karnaugh map.(10p)

(2) Draw the logic diagram with the least number of NAND gates.(10p)

2. Implement a logic circuit for the truth table. (20p)

Inputs				Output
A	*B*	*C*	*D*	*X*
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

3. Implement the logic function specified in Truth table by using a 74HC138 decoder. (20p)

A B C D	Y
0 0 0 0	0
0 0 0 1	0
0 0 1 0	1
0 0 1 1	1
0 1 0 0	0
0 1 0 1	1
0 1 1 0	0
0 1 1 1	1
1 0 0 0	0
1 0 0 1	0