# Sichuan University Examination

# (Closed Book)

# (2019-2020 Academic Year 1stDECEMBER) Quiz-3

课程号 Course Number: 304131030-04 课程名称 Course Title: Digital Logic
任课教师 Lecturer:Xuedong Yuan 考试时间 Time Period: 70 minutes
学生姓名 Name: 学号 Student ID: 成绩 Total Mark:

## 考生承诺

## Student Commitment

我已认真阅读并知晓《四川大学考场规则》和《四川大学本科学生考试违纪作弊处分规定（修订）》，郑重承诺：

I have read and comprehended the "Regulations of Sichuan University on Examinations". I give my commitments as follows:

1、已按要求将考试禁止携带的文具用品或与考试有关的物品放置在指定地点；

1. I have put prohibited stationary and exam-related items at designated area as required.

2、不带手机进入考场；

2. I have not brought cell phone to the examination room.

3、考试期间遵守以上两项规定，若有违规行为，同意按照有关条款接受处理。

3. During the examination, I will comply with the above two provisions. If there is any violation, I agree to accept the punishments in accordance with the relevant provisions.

**考生签名：**
**Signature:**

| 题号 | 一(20%) | 二(20%) | 三(60%) | 四(0%) | 五(0%) |
|---|---|---|---|---|---|
| 得分 | | | | | |
| 卷面总分 | | 教师签名 | | 阅卷时间 | |

**Notice: 1. Please write your student ID and your name in both exam papers and added answer papers precisely;**

**2.Please write all your answers on this exam paper;**

**3.After the exam, please hand in exam paper, added answer sheet and scratch papers to examiners all together.**

| 评阅教师 | 得分 |
|---|---|
| | |

**一、填空题 Fill in the blanks（本大题共 10 空，每空 2 分，共 20 分）。**

1. An active HIGH input S-R latch is formed by the cross-coupling of two _____(NOR/NAND/OR/AND) gates.
2. A flip-flop is SET when J=_____, K=_____.
3. To enter a byte of data serially into an 8-bit shift register, there must be _____ clock pulse(s).
4. A modulus-15 counter has 15 states requiring _____ flip-flops.
5. A 5-bit binary counter has a maximum modulus of _____.

6. If the initial count of a modulus-13 binary counter is 0100, what shall be the value of count after 10 clock edge?_____.
7. A 4-bit binary up/down counters is in the binary state of zero. The next state in the DOWN mode is _____.
8.A J-K flip-flop with J = 1 and K = 1 has a 10 kHz clock input. The Q output is _____kHz.
9.The group of bits 10110101 is serially shifted (right-most bit first) into an 8-bit parallel output shift register with an initial state of 11100100. After two clock pulses, the register contains _____.

| 评阅教师 | 得分 |
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**二、判断题 True/False Questions（本大题共 10 空，每空 2 分，共 20 分）。**

_____ 1. An edge-triggered D flip-flop changes state whenever the D input changes.

_____ 2. Synchronous counters cannot be realized using J-K flip-flops.

_____ 3. A shift register cannot be used as a time delay device.

_____ 4. A shift register with four stages can store a maximum count of fifteen.

_____ 5. A latch is considered to be in the RESET state when the *Q* output is low.

_____ 6. A clock input is necessary for an edge-triggered flip-flop.

_____ 7. A gated D latch cannot be used to change state.

_____ 8. When both the *J* and *K* inputs are HIGH, an edge-triggered J-K flip-flop changes state on each clock pulse.

_____ 9. If the present state is 1000, the next state of a 4-bit up/down counter in the DOWN mode is 0111.

_____ 10. To achieve a modulus of 100, ten decade counters are required.

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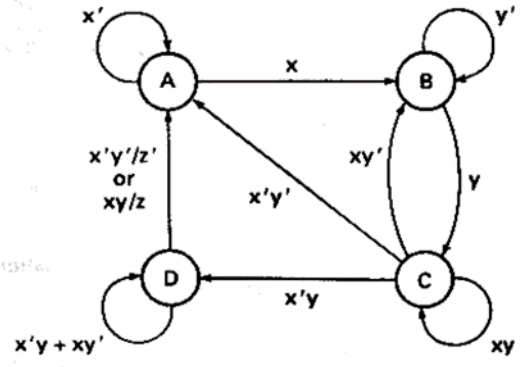
**三、问答题 Question and Answer（本大题共 4 小题，共 60 分）。**

1. List a state table for the following state diagram.

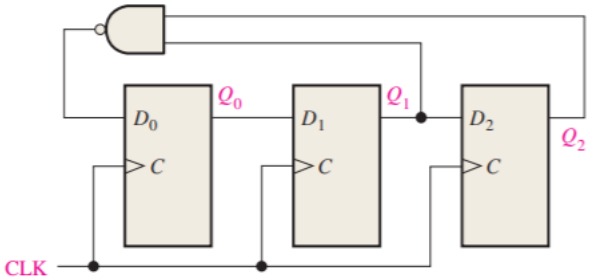
State machine $M_1$




**State Table**

| Present state | Next state $xy/z$ | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 00 | z | 01 | z | 11 | z | 10 | z |
| A | | | | | | | | |
| B | | | | | | | | |
| C | | | | | | | | |
| D | | | | | | | | |

2. Determine the sequence of the counter in the Figure.




3. Develop a logic circuit that will detect a serial input sequence of 10110. The detection of the required bit pattern can occur in a longer data string and the correct pattern can overlap with another pattern. When the input pattern has been detected, cause an output z to be asserted high. For example, let the input string be

x = 10110110110

z = 00001001001