四川大学第三次测验试题（2018~2019 - 1）

课程号： 304131030 课序号： 08 课程名称： 数字逻辑（双语） 任课教师：

适用专业年级： 计算机类2018 学号： 姓名：

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1. (10 points)A modulus-9 counter has 9 states requiring \_\_\_\_ flip-flops. A modulus-9 ring counter requiring \_\_\_\_\_\_ flip-flops.

2. (5 points)A register’s function include ( )

(a) data storage (b) data movement

(c) neither (a) not (b) (d) both (a) and (b)

3. (5 points)To parallel load a byte of data into a shift register with a synchronous load, there must be ( )

(a) one clock pulse (b) one clock pulse for each I in the data

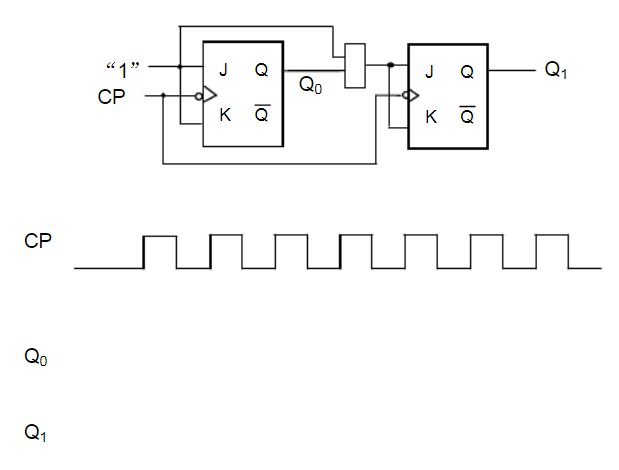
(c) eight clock pulses (d) one clock pulse for each 0 in the data

4. (12 points) List the characteristic equations of SR flip-flop, JK flip-flop and D flip-flop

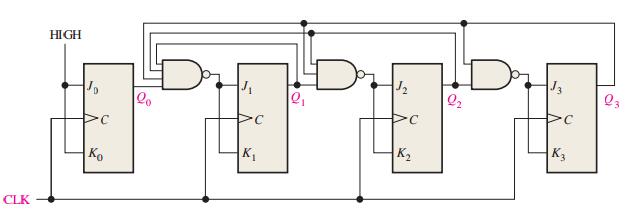
5. (10 points)In the figure for this problem, complete the timing diagram for a positive edge triggered J-Kflip-flop.



6. (10 points)Given the logic diagram for this problem, complete the partial timing diagram.



7. (15points)Determine the sequence of the counter in Figure. Begin with the counter cleared.



8. (18 points)Design a counter to produce the following binary sequence with J-K flip-flops: 0 🡪 7 🡪 6 🡪 1 🡪 0

9. (15 points)Construct a state diagram that will detect a serial input sequence of 01101.