Project 3: Designing your own semiconductor quantum processor

Mosescu Andrei-Mihnea
Student ID: 5980208

Nicolae Mario-Alexandru
Student ID: 5988543

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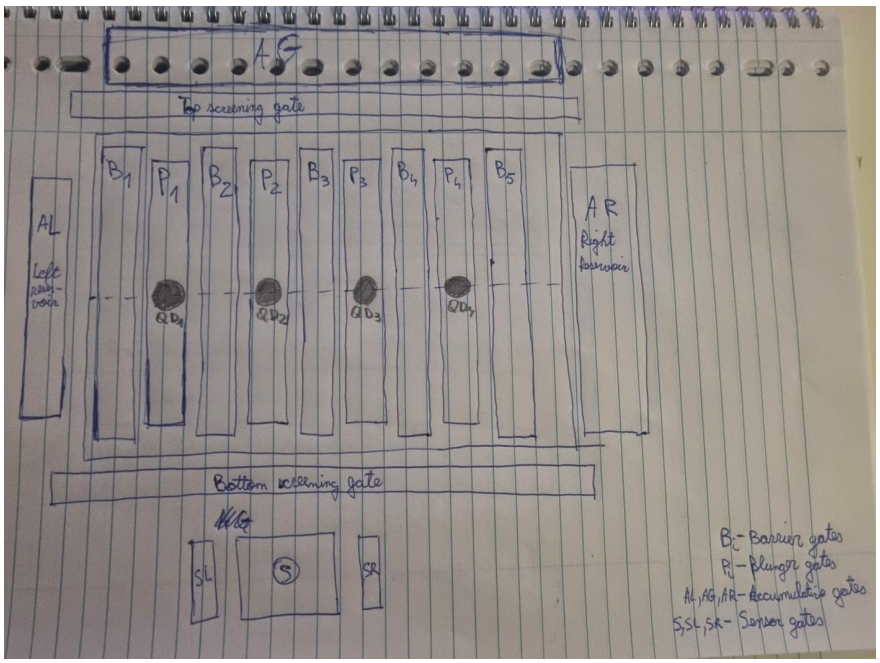
1 Top View: 4-Qubit Linear Quantum Dot Array



The figure shows the top view of the 4-qubit quantum dot system. Our device is based on a silicon/silicon-germanium (Si/SiGe) heterostructure, using an **over-**

lapping aluminum gate architecture. Four single electrons are confined under plunger gates (P1–P4) to form four spin qubits (QD1–QD4) arranged in a linear array. Each dot's electron spin encodes a qubit with states $\uparrow$ and $\downarrow$.

Our architecture allows precise control over each dot's potential, tunneling rates between neighbors, and coupling to the electron reservoirs on the left and right sides. A nearby charge sensor (S, SL, SR) is also included for high-fidelity readout.

Gate Layout and Function

From left to right, the structure consists of two electron reservoirs and four quantum dots separated by tunable barriers. Each dot is defined by a combination of barrier and plunger gates. Accumulation and screening gates shape the overall potential landscape.

- **Plunger Gates (P1–P4, orange):** These gates control the potential energy of each dot. By changing the plunger voltage, we can tune whether a dot holds one electron or is empty.
- **Barrier Gates (B1–B5, blue):** The barrier gates control the tunneling between dots and/or reservoirs. Adjusting their voltage allows us to turn coupling on or off, which is essential for performing two-qubit exchange operations. The coupling strength t_c between two dots determines the exchange interaction $J = 4t_c^2/U$, which is used for two-qubit gates.
- **Accumulation Gates (AG, AL, AR, red):** The accumulation gates are positively biased to create the two-dimensional electron gas (2DEG) in the quantum well. The global AG gate forms the conductive channel for the dots, while AL and AR define the left and right reservoirs for loading and unloading electrons.
- **Sensor and Screening Gates (S, SL, SR, gray/green/purple):** These form a separate charge sensor dot near QD4. It detects changes in nearby charge configurations and is used for spin-to-charge conversion during readout.

Materials and Device Dimensions

For the gate electrodes we chose metallic layers (typically Ti/Pd or Al) deposited on top of a thin Al_2O_3 dielectric (5–10 nm) that electrically isolates them from the semiconductor. The underlying Si/SiGe heterostructure consists of:

- a relaxed $Si_{0.7}Ge_{0.3}$ buffer layer,
- a strained Si quantum well (8–10 nm thick) where electrons are confined,
- and a $Si_{0.7}Ge_{0.3}$ barrier (50–60 nm thick) that prevents electrons from escaping to the surface.

When the accumulation gate is biased, a 2DEG forms in the quantum well. Our system has this parameters:

- Dot-to-dot spacing: ∼100 nm
- Gate width: 30–50 nm
- Lever arm: $\alpha \approx 0.1$–0.15 eV/V
- Charging energy: ∼3–5 meV
- Tunnel coupling: 0.1–10 GHz (tunable)

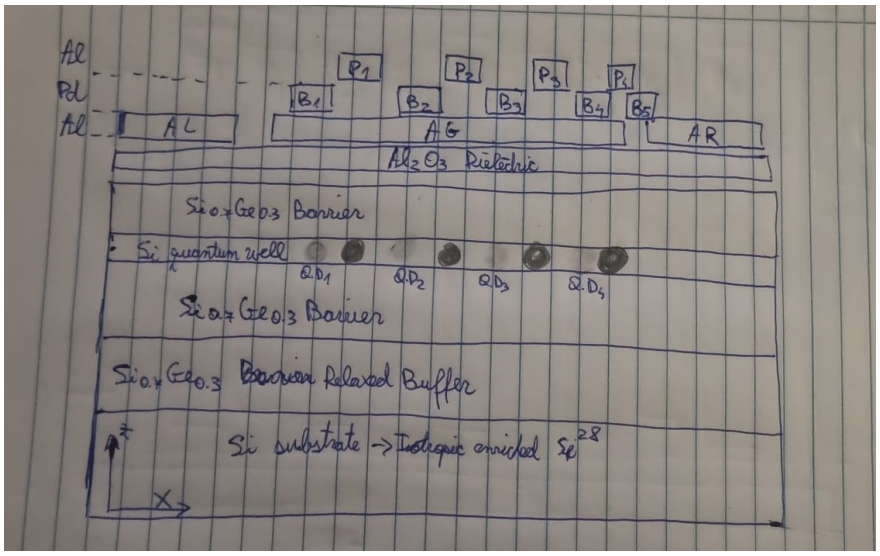
How the Top View Works

The top layer of gates defines the horizontal layout of the quantum dot array.

The reservoirs on the left (AL) and right (AR) sides provide a source and drain of electrons. These are used for initialization and readout.

The charge sensor (S) detects whether each dot is occupied or not by monitoring small changes in the electrostatic potential nearby.

2 Side View: Cross-Section Through the 4-Qubit Quantum Dot Array



The figure shows the side view of the four-qubit system, where we can see how the different materials and gate layers are stacked vertically to form the quantum dots. We chose the structure to be based on a silicon/silicon-germanium

(Si/SiGe) heterostructure with an overlapping gate design. Each quantum dot traps a single electron in the Si quantum well, and the electron's spin represents the qubit state ($\uparrow$ or $\downarrow$).

Material Layers and Structure

From bottom to top, the layers that make up our device are:

- **Silicon (Si) Substrate:** The base of the device. It is isotopically enriched ^{28}Si, which means most nuclear spins are removed. This helps keep the electron spins coherent for a long time (long T_2^*).
- **$Si_{0.7}Ge_{0.3}$ Relaxed Buffer (about 2 µm thick):** This layer smooths out the lattice mismatch between pure Si and SiGe and helps to grow a strained Si quantum well on top of it. The strain also lifts valley degeneracy, which is useful for qubit control.
- **$Si_{0.7}Ge_{0.3}$ Barrier (around 50–60 nm):** This barrier keeps the electrons confined vertically, stopping them from escaping to the surface.
- **Si Quantum Well (around 8–10 nm):** This is the key layer where the two-dimensional electron gas (2DEG) forms when a positive voltage is applied to the accumulation gate (AG). Electrons in this region are laterally confined by the gates above to form the quantum dots QD1–QD4.
- **Al_2O_3 Dielectric (5–10 nm):** A thin oxide that separates the metal gates from the semiconductor. It allows electrostatic control without current flow.
- **Metal Gate Layers (Aluminum and Palladium):** There are three main overlapping gate layers:
  - **Bottom layer (Al):** Used for accumulation and screening gates such as AL, AR, and AG.
  - **Middle layer (Pd):** Forms the plunger (P1–P4) and barrier gates (B1–B5), which define the actual quantum dots.
  - **Top layer (Al):** Used as a global screening or additional accumulation gate.

Gate Functions and Operation

In our device each gate has a specific role:

- **Accumulation Gate (AG):** When a positive voltage is applied, it pulls electrons into the Si quantum well, forming the 2DEG region where the quantum dots are created.

- **Barrier Gates (B1–B5):** These gates are negatively biased to locally block the flow of electrons, creating tunnel barriers between the dots or between a dot and a reservoir. By adjusting the barrier voltage, the tunnel coupling (t_c) can be changed.
- **Plunger Gates (P1–P4):** These control the potential energy inside each dot, deciding whether it holds one electron or none. They are used to tune the energy levels of each qubit.
- **Reservoir Gates (AL, AR):** On both sides, these gates define electron reservoirs that act as sources and drains for loading and unloading electrons during initialization or readout.

Typical Parameters

The device dimensions and electrical properties are within the same range as experimental four-qubit Si/SiGe devices:

- Quantum well thickness: ∼8 nm
- Barrier thickness: ∼50–60 nm
- Dot-to-dot spacing: ∼100 nm
- Gate width: 30–50 nm
- Charging energy E_C: 3–5 meV
- Lever arm α: 0.1–0.15 eV/V
- Operating temperature: 20 mK ($k_B T \ll E_C$)

3 Connection to the DiVincenzo Criteria and System Operation

In this section, we connect the design of our 4-qubit silicon quantum dot system to the five DiVincenzo criteria, which define the basic requirements for a physical quantum computing platform. Each criterion is explained, followed by how it is satisfied in our system. At the end we also describe how the device can be operated step-by-step.

Criterion 1: A scalable physical system with well-defined qubits

Meaning of the criterion.
This criterion means that the physical qubits must be clearly defined and that the architecture can be scaled to more qubits in the future (DiVincenzo, *The Physical Implementation of Quantum Computation*, 771–783, 2000).

How it is achieved in our system.
In this design, each qubit is encoded in the spin of a single electron confined in a silicon quantum dot (Zwanenburg et al., *Silicon Quantum Electronics*, 961–1019, 2013). Operating in the single-electron regime ensures a clean two-level spin system with basis states

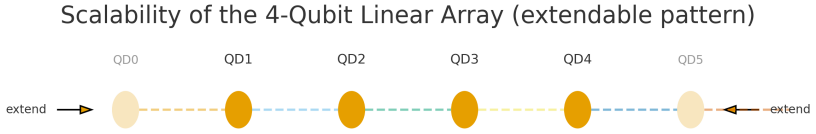
$$|0\rangle = |\uparrow\rangle, \quad |1\rangle = |\downarrow\rangle,$$

split by the Zeeman energy $E_Z = g\mu_B B$. Four identical dots (QD_1–QD_4) are created in a linear Si/SiGe heterostructure using the same accumulation, barrier, and plunger gates. Because all dots are defined in the same quantum well and share the same geometry, they have similar charging energies, g-factors, and lever arms, which makes their control uniform.

Each dot can be tuned individually using its plunger gate, while the barrier gates between them set the tunnel coupling t_c.

Each qubit is formed when the plunger voltage is tuned so that exactly one electron remains trapped in the corresponding dot, while the barrier gates isolate it from the reservoirs. A uniform external magnetic field B (a few hundred millitesla) lifts the spin degeneracy through the Zeeman effect, defining the $\uparrow$ and $\downarrow$ states. Single-qubit control can be achieved by applying an oscillating voltage to a nearby gate, producing an AC magnetic field at the electron's Larmor frequency. Two-qubit interactions are activated by momentarily lowering a barrier gate to increase the tunnel coupling t_c, which turns on the exchange interaction between neighboring spins. After the operation, the barrier is raised again to decouple the qubits.

The 1×4 array demonstrates a scalable and repeatable qubit design, where each additional qubit can be realized by duplicating the same gate pattern. However, as more qubits are added, this purely linear layout becomes less practical. For this reason, experimental efforts such as those reported by Hendrickx et al. (*A Four-Qubit Germanium Quantum Processor*, Nature, 487–491, 2020) and analyzed by Tadokoro (2021) explore transitions from simple linear chains to two-dimensional (2D) architectures, which offer better connectivity and control for larger systems. Our design therefore satisfies scalability in principle, but within the scope of small arrays.



Scalability of the 4-qubit Si/SiGe linear quantum dot array. The four active dots (QD1–QD4) represent the implemented qubits, while the faded dots (QD0 and QD5) indicate that the same pattern of plunger and barrier gates can be extended to form larger arrays. This modular design demonstrates that the

architecture is scalable while maintaining well-defined and individually controllable qubits.

Criterion 2: The ability to initialize qubits to a known state

Meaning of the criterion.
To perform reliable quantum operations, each qubit must be prepared in a known starting state, usually $\downarrow$ or logical 0. R.Hanson outlines the general principles of spin initialization and control in gate-defined quantum dots.(R. Hanson et al., *Spins in Few-Electron Quantum Dots*, 1217–1265 2007)

How it is achieved in our system.
Each quantum dot (QD_1–QD_4) in the array can be connected to its nearest electron reservoir through a tunable tunnel barrier. Initialization is performed by adjusting the voltages on the plunger and barrier gates as follows:

1. **Emptying the dot:** The plunger voltage V_{P_i} is made more positive so that the dot energy level rises above the Fermi level of the nearby reservoir (A_L or A_R). This allows the electron to tunnel out, leaving the dot empty.

2. **Loading a single electron:** The plunger voltage is then slowly reduced until the dot's lowest orbital level crosses the Fermi level. An electron from the reservoir tunnels in and occupies this ground orbital. Because the Zeeman energy $E_Z = g\mu_B B$ is larger than $k_B T$, the electron enters in the spin-down state $\downarrow$ with high probability.

3. **Isolating the qubit:** After the electron is loaded, the barrier gate between the dot and the reservoir is made slightly more negative, trapping the electron in the dot and isolating it from the environment.

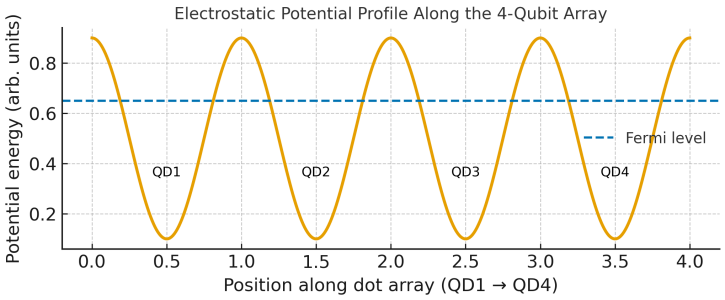
This way we can initializes each qubit into the $\downarrow$ state. For the two inner qubits (QD_2 and QD_3), initialization can be done by coupling them temporally to the other dot, since they don't have a direct connection to the reservoir. By opening the intermediate barrier gate (for example B_2 or B_3), an electron can tunnel through from another dot.

At the end of an operation cycle, the same gate sequence can be repeated to empty all dots and reload the array into the $(1, 1, 1, 1)$ charge configuration. This provides our system with a reliable way to reset the system between computations or measurement runs.

Successful initialization requires that the thermal energy is smaller than the Zeeman splitting, $k_B T \ll E_Z$, so that the ground spin state is occupied. An operating temperature of 20 mK and a magnetic field of 0.5 T, $k_B T \approx 2$ μeV and $E_Z \approx 60$ μeV, satisfy this condition. This method is the same spin-selective loading process described in the *Semiconductor Qubits* coursebook.

Initialization by spin-selective tunneling from a reservoir has been demonstrated in silicon and germanium quantum-dot devices similar to ours. The four-qubit processor by Hendrickx (2020) uses this method to prepare each hole spin in its ground state before control operations. Likewise, Pedicini (Giovanni

Pedicini et al 2025 Quantum Sci. Technol. 10 045012) simulated the same procedure for an all-silicon four-dot array, confirming that single-electron loading with Zeeman splitting produces reliable initialization within the temperature range of dilution refrigerators.

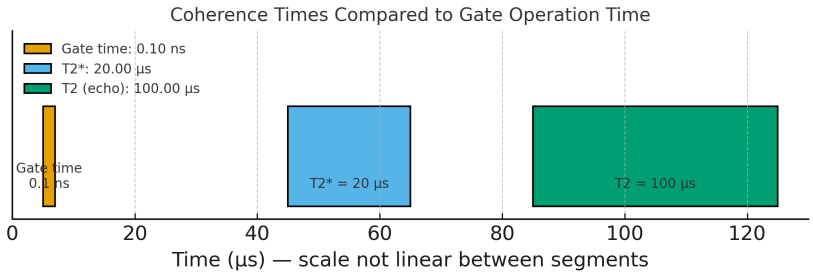


The electrostatic potential profile shown in supports both the scalability and initialization aspects of this quantum dot system. From the figure, we can see four distinct potential wells (QD1–QD4) formed by the gate-defined confinement in the Si/SiGe heterostructure. Each well corresponds to one spin qubit that can be individually tuned by adjusting the plunger and barrier gate voltages. At the same time, the repeating pattern of wells and barriers demonstrates how this layout can be extended to more qubits, illustrating the scalability of the design.

Criterion 3: Long coherence times compared to gate operation times

Meaning of the criterion.
Qubits must maintain their quantum state long enough to perform many operations before losing coherence.

How it is achieved in our system.
Silicon is an ideal material for this because it can be isotopically purified (^{28}Si) to remove almost all nuclear spins, greatly reducing magnetic noise. This strongly suppresses random fields that would otherwise cause dephasing. In the Si/SiGe heterostructure of my device, the electrons are also well isolated from charge fluctuations by the surrounding SiGe barriers and the thin Al_2O_3 oxide layer, which further improves coherence. Experiments in Si/SiGe have shown single-qubit coherence times (T_2^*) in the tens of microseconds, which is much longer than the gate times. In our device, the qubits operate at millikelvin temperatures and magnetic fields around 0.5–1 T, providing a stable environment for high-fidelity spin control. Simulations in similar architectures (Giovanni Pedicini et al 2025 Quantum Sci. Technol. 10 045012) confirm that long T2 times persist in linear four-dot arrays when operated under these conditions.



Comparison of spin-qubit coherence and operation times in a Si/SiGe quantum dot. The single-qubit gate operation time ($t_{\text{gate}} \approx 0.1\,\text{ns}$) is several orders of magnitude shorter than the dephasing time ($T_2^* \approx 20\,\mu\text{s}$) and the echo-extended coherence time ($T_2 \approx 100\,\mu\text{s}$). This large ratio ensures that many quantum gate operations can be performed before decoherence limits fidelity.

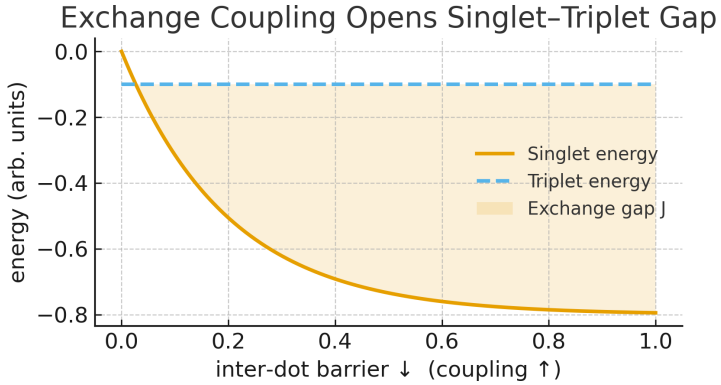
Criterion 4: A universal set of quantum gates

Meaning of the criterion.
To achieve universal quantum computation, we need both single-qubit and two-qubit gates. Any complex quantum algorithm can then be built by combining these gates.

How it is achieved in our system.
Single-qubit gates in this system are performed using **electric dipole spin resonance (EDSR)**. A microwave signal is applied to one of the gate electrodes in the presence of a magnetic field(0.5 - 1T) that defines the spin qunatization axis, allowing fast spin rotations around the X and Y axes. Z-rotations are done by waiting for phase accumulation under the Zeeman splitting. Single-qubit gate fidelities above 99.9% have been reported in silicon.

Two-qubit gates are realized by pulsing the inter-dot barrier to temporarily increase the tunnel coupling between neighboring dots. This coupling allows the implementation of gates such as the controlled-phase (CZ) or controlled-NOT (CNOT) by controlling the duration and strength of the exchange pulse. The underlying mechanism corresponds to the "Two Electrons in a Double Quantum Dot" model from the coursebook, where exchange coupling mixes singlet and triplet spin states. Both types of gates have been successfully demonstrated in Ge/SiGe devices(N.W.Hendrickx et al., "A Four-Qubit Germanium Quantum Processor", 487–491, 2020).

Because each qubit can be addressed individually and neighboring pairs can be coupled on demand, this architecture provides a universal set of quantum gates, fulfilling the fourth DiVincenzo criterion.



Exchange coupling between neighboring spin qubits. When the inter-dot barrier is lowered by tuning the gate voltage, tunnel coupling increases, which opens an energy gap J between the singlet and triplet spin states. This tunable exchange interaction forms the basis of two-qubit entangling gates such as CNOT or CZ operations.

Criterion 5: Qubit-specific measurement capability

Meaning of the criterion.
Each qubit must be measured individually to read out the result of a computation. In other words, after quantum operations are performed, the system must allow projective measurement of each qubit's basis state (for spin qubits, whether the electron is spin-up or spin-down). A good measurement method must be accurate, fast compared to the qubit's relaxation time, and ideally nondestructive.

How it is achieved in our system.
In this device, readout is achieved through **spin-to-charge conversion**, where the spin state of the electron is converted into a charge signal that can be detected by a nearby charge sensor dot.

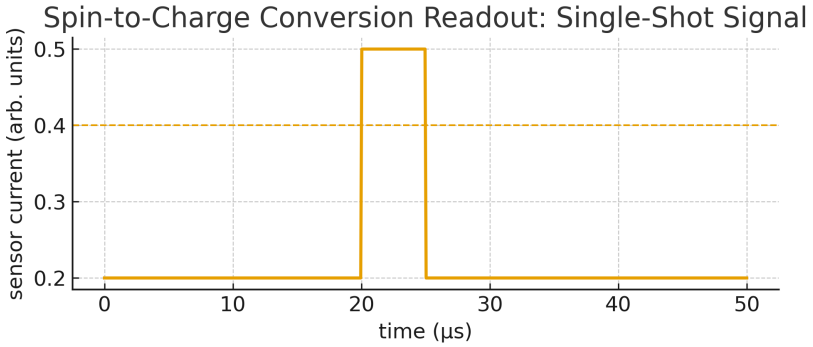
The outer qubits (QD_1 and QD_4) are measured using spin-to-charge conversion via the Elzerman method. During readout, the plunger gate voltage is pulsed so that the spin-up state $\uparrow$ lies above the Fermi level of the nearby reservoir, while the spin-down state $\downarrow$ remains below it. If the electron is in $\uparrow$, it tunnels out to the reservoir; if it is in $\downarrow$, it stays trapped in the dot. This converts the spin information into a detectable charge change, which is sensed by the nearby charge sensor (S, SL, or SR).

Hendrickx (2020) used the same technique to read out four coupled spin qubits in a Ge/SiGe processor. Pedicini (2025) simulated a nearly identical four-dot Si/SiGe layout and confirmed that charge-sensor signals clearly distinguish between spin-up and spin-down states under typical operating conditions.

In addition to spin-selective tunneling, spin readout can also be performed using Pauli spin blockade between two neighboring dots. In this method, the

qubit pair is pulsed from the (1,1) to the (0,2) charge configuration. Only a singlet state can make this transition, while triplet states are blocked by the Pauli exclusion principle. The resulting charge configuration is detected with the same nearby sensor dot. This readout technique is especially useful for the inner dots (QD_2 and QD_3), which do not have direct access to reservoirs, and has been demonstrated in Ge/SiGe devices such as Hendrickx (2020).

In our design, Elzerman readout is used for the outer qubits (QD_1 and QD_4), which are directly connected to reservoirs. For the inner qubits (QD_2 and QD_3), Pauli spin-blockade readout is used instead, since these dots have no direct reservoir access. Attempting Elzerman readout on them would require opening multiple barriers and disturb the neighboring qubits, whereas PSB provides a local, reservoir-free measurement method.



Single-shot qubit readout using spin-to-charge conversion. If the qubit is in the ↑ state, the electron tunnels out of the dot, producing a short current pulse ("blip") in the nearby charge sensor. If the qubit is in the ↓ state, no tunneling occurs and the signal remains flat. This allows fast and high-fidelity projective measurement of individual spin states.

System Operation Summary

Putting everything together, the operation cycle of the 4-qubit device works as follows:

1. **Tuning and stabilization:** The accumulation gate (AG) is turned on to form the 2DEG. Using the plunger and barrier gates, each dot is tuned to hold exactly one electron, resulting in the charge configuration (1,1,1,1). Charge stability diagrams are mapped to identify the correct bias points.

2. **Initialization:** The spin-selective tunneling method (Elzerman) is used to prepare all four spins in the ↓ state.

3. **Single-qubit control:** Microwave pulses are applied for EDSR rotations on individual spins, implementing X and Y rotations.

4. **Two-qubit operations:** Exchange coupling between neighboring dots is pulsed to perform CZ or CNOT gates, entangling the spins.

5. **Readout:** Each spin is measured via spin-to-charge conversion using the nearby charge sensor or through PSB for pairs of dots.

This sequence can be repeated and scaled up to larger arrays, as already demonstrated in multi-qubit Si/SiGe processors. The combination of long coherence times, tunable coupling, and reliable initialization and readout makes this system fully compatible with the DiVincenzo criteria for quantum computation.