Aayush Gautam

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SUMMARY

Final-year ECE student passionate about VLSI devices and fabrication, with hands-on 180 nm CMOS, cleanroom processing, and device reliability testing. Versatile builder who also explores AI/ML for hardware applications including compute-in-memory and vision pipelines. Strong communicator, multilingual, and comfortable working across cultures through Indo–Taiwan collaborations and team-based projects

EDUCATION

B.E. in Electronics and Communication Engineering

UIET, Panjab University • Chandigarh, India • Nov 2022 - May 2026 • 8.52/10

• Coursework: VLSI Design, Digital Logic Design, Embedded Systems, Analog and Digital Signal Processing, Antenna and Wave propagation.

Higher Education

Govt. Model Sen. Sec. School 19 • Chandigarh, India • 2022 • 89.9%

Secondary Education

St. Joseph's Sr. Sec. School • Chandigarh, India • 2020 • 90.9%

SKILLS

EDA Tools: Cadence Virtuoso, SystemVerilog, Verilog, VHDL, Xilinx Vivado (Design Suite), Tanner EDA / PSpice, Clewin

Fabrication & Characterization: Wafer cleaning, spin coating, photolithography, wet/dry etching, thin-film deposition, metallization

Programming & IoT : C/C++, Python, NumPy, Pandas, PyTorch, TensorFlow, I^2C/SPI/USART, Git

EXPERIENCE

Project Intern

Semiconductor Laboratory (SCL) **June 2025 - July 2025, Mohali, India**

• Characterized 50+ wafer sites of gate-oxide test structures on 180 nm CMOS under senior process supervision.
• Used Agilent B1500A with Summit 11000AP probe station to measure leakage, breakdown voltage, and TDDB for dielectric reliability.
• Correlated results with oxide thickness and process corners; mapped trends and identified weak conditions.
• Compiled findings that supported gate-oxide process qualification and reliability benchmarking.

Workshop Trainee

Indo-Taiwan Semiconductor Workforce Development Program **December 2024 - March 2025, NTHU, Taiwan**

• Completed a 35-day training program at IIT Hyderabad (20 days) and NTHU Taiwan (15 days), gaining hands-on experience in wafer cleaning, photolithography, wet etching, and aluminum metallization on 6-inch silicon wafers.
• Ran core steps: wafer cleaning, photolithography, wet etch, Al metallization; captured process windows and yields.
• Designed photomasks in Clewin and fabricated MEMS cantilever structures using laser/EUV lithography with follow-up etch and metal.
• Executed flow integration: thin-film deposition, dielectric patterning, plasma ashing; documented end-to-end parameters.
• Verified output via SEM, XRD, profilometry, probe-station I–V and presented a brief on Photonic Interconnects in Data Centers.

IoT Engineer Intern

IIT Roorkee **June 2024 - July 2024, Uttarakhand, India**

• Built an IoT acoustic monitor for hospitals that detects and tags noise sources in real time.
• Programmed an ESP8266 to capture and preprocess audio, send data over Wi-Fi, and issue SMTP email alerts to staff.
• Designed configurable time-series logging of noise levels and events, with hooks for adaptive AI to auto-tune thresholds.

Embedded Firmware Trainee

Menthosa Solutions **January 2024 - March 2024, UIET, Chandigarh**

• Developed flight-critical BMS firmware for surveillance drones to ensure safe, reliable power management.
• Implemented real-time battery health monitoring, dynamic cell balancing, and over/undervoltage protection algorithms onboard.
• Integrated low-level embedded interfaces (ADC, I^2C/SPI, GPIO/interrupts) and optimized timing, latency, and efficiency.
• Validated against safety standards; improved reliability, extended Li-ion cycle life, and documented production deployment.

PUBLICATIONS

IoT and Its Future Prospect: A Case Study on Smart Labs
Technical Report • Cyber Security Insights Magazine, Vol 4 • 2023
- **Authors: Aayush Gautam**, Vandana Sharma
- **Pages:** 20-23 **DOI:** 10.13140/RG.2.2.22910.46408

Integration of IoT and AI in Bioengineering of Natural Materials
Book Chapter • Calcium-Based Materials, CRC Press • 2024
- **Authors:** Jaswinder Singh Sandhu, Abhinav Jamwal, Devinder Mehta, **Aayush Gautam**
- **Pages:** 168-188 **ISBN:** 9781003360599

Indian Sign Language Recognition using YoloV5 on Custom Dataset
Conference Paper • ICSPED 2026 • 2026
- Submitted, under review

A 98.5-TOPS/W and 0.73-TOPS/mm2 Digital Compute-In-Memory Macro with a Novel 6T+MUX Bitcell For Sparsity-Aware MAC Operations
Conference Paper • VLSID 2026 • 2026
- Accepted, to appear

PROJECT

Design and Tapeout of CMOS Inverter using Cadence Virtuoso
UIET, Panjab University • August 2025 - September 2025
- Designed and verified a CMOS inverter in Cadence Virtuoso (180 nm), completing schematic-to-layout per foundry rules.
- Ran DRC/LVS/PEX and Monte-Carlo sweeps; analyzed Vth, delay, and power across PVT corners.
- Prepared the final tapeout: streamed GDSII with padframe, added I/O metal bond pads and labels, and re-verified DRC for fab readiness.

Indian Sign Language Recognition Using Computer Vision
UIET, Chandigarh • February 2025 - September 2025
- Built a real-time Indian Sign Language (ISL) pipeline with YOLOv5 for hand detection and a TensorFlow classifier for sign recognition.
- Collected image/video data and created 6,000+ labeled instances in CVAT; handled preprocessing and augmentation with Pillow and set up train/val/test splits.
- Trained and evaluated the models end-to-end and submitted a conference paper documenting the dataset, pipeline, and results.

Digital Compute-in-Memory (CIM) Architecture using MUX-based MAC Operations
IIT Roorkee • June 2025 - August 2025
- Designed and simulated an 8×8 MUX-based MAC array for a digital compute-in-memory architecture at IIT Roorkee, improving logic efficiency and data throughput.
- Developed the initial architecture and behavioral model in Xilinx Vivado using Verilog HDL and validated timing accuracy across more than 10 simulated MAC cells.
- Trained QAT models (ResNet-18/32/50) on CIFAR-10/100 to evaluate deployment on the CIM architecture.

Wafer-Scale Micro-Cantilever Fabrication
IIT Hyderabad • December 2024 - January 2025
- Utilized Clewin software to create EUV photolithography masks and implemented wafer-scale wet etching and aluminum metallization on 6-inch wafer.
- Integrated plasma ashing and dielectric patterning steps, utilizing EUV lithography and SEM analysis to verify process outcomes and optimize wafer-scale cantilever fabrication workflows.
- Trained QAT models (ResNet-18/32/50) on CIFAR-10/100 to evaluate deployment on the CIM architecture.

Coffee Break: A perfect companion for a mental break
Google AI • March 2024 - May 2024
- Built an AI-powered mental health chatbot for students to support well-being and outreach.
- Integrated the Gemini API with a ~4,000-word system prompt for natural, empathetic dialogue.
- Engineered a human-like experience with supportive tone, context memory, and resource guidance for students.

CERTIFICATIONS

CS50: Introduction to Computer Science
Harvard University • 2024
- Entry-level computer science course that covers Scratch, C, Python, SQL, HTML, CSS, JavaScript, and Flask.

Machine Learning
Mood Indigo IIT Bombay • 2023
- Python, NumPy, Pandas, scikit-learn; recommendation-system pipelines (model training & evaluation)