DIGITAL DESIGN

ASSIGNMENT 3

Deadline: *22:55, Tuesday 19 November 2019*

Lab sessions & Location:

1. **Lychee Garden 6, Room 406 (Wednesday 16:20-18:10 pm)**
2. **Lychee Garden 6, Room 408 (Wednesday 19:00-20:50 pm)**
3. **Lychee Garden 6, Room 402 (Thursday 8:00-9:50 am)**
4. **Lychee Garden 6, Room 402 (Thursday 10:10~12:10 am)**

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PART 1: DIGITAL DESIGN THEORY

Provide answers to the following questions:

1. Draw the multiple-level nor circuit for the following expression:
   F = AB(D + C) + (BC' + DE') + BD'
2. Implement the following Boolean function F, using the two-level forms of logic

   (a) AND-OR, (b) OR-NAND, (c) NOR-OR, (d) NAND-NAND, (e) OR-AND,

   (f) NOR-NOR, and (g) NAND-AND:

   $F(A, B, C, D) = \sum (1, 4, 5, 8, 9, 10, 11, 13, 15)$

   Please note that you only need to write the logic equation, no drawing needed
3. Derive the circuits for a four-bit parity generator and three-bit parity checker using an odd parity bit. Write the truth table, simplify your logic equation and draw circuit diagram.
4. Design a combinational circuit with three inputs, x , y , and z , and three outputs, A, B , and C. When the binary input is 3, 4, 5, 6, or 7, the binary output is one less than the input. When the binary input is 0, 1, or 2, the binary output is two greater than the input. Write the logic formula and draw circuit diagram.
5. An ABCD-to-seven-segment decoder is a combinational circuit that converts a decimal digit in BCD to an appropriate code for the selection of segments in an indicator used to display the decimal digit in a familiar form. The seven outputs of the decoder (a, b, c, d, e, f, g) select the corresponding segments in the display, as shown in figure (a). The numeric display chosen to represent the decimal digit is shown in (b). Using a truth table and/or Karnaugh maps, design the BCD-to-seven-segment decoder using a minimum number of gates. All the invalid input should display nothing.

(a) Segment designation (b) Numerical designation for display

Hint: You may use 74LS138 decoder

6. For a binary multiplier that multiplies two unsigned four-bit numbers : Using AND gates and binary adders, design the circuit. Briefly describe your design and list the logic formulas. Draw the circuit diagram. For adders, you can just use a block diagram with ports to represent them.
7. Implement the following Boolean function with a multiplexer.
    a. F(A, B, C, D) =∑ (0, 2, 5, 8, 10, 14)
    b. F(A, B, C, D) = ∏(2, 6, 11)
8. Implement a full subtractor with two 4x1 multiplexers. Write down your process.
9. An 8x1 multiplexer has inputs A, B, and C connected to the selection inputs S0, S1, and S2, respectively. The data inputs I0 through I7 are as follows: I0 = I2 = 1; I4 = I7 = 0; I3 = I5 = D'; I1 = I6 = D. Determine the Boolean function that the multiplexer implements. Write your process.

PART 2: DIGITAL DESIGN LAB

INTRODUCTION

In this lab, you are required to use Vivado 2017.4 and Minisys/EGO1 Practice platform (xilinx FPGA chip artix 7 inside) to design a combinational logic circuit and test it.

PREAMBLE

Before working on the coursework itself, you should master the following material.

1.’CH3-Minimisation-SUSTC-new.ppt’ and ‘CH4-COMBINATIONAL LOGiC-new.ppt’ in Sakai site.

2. ‘Digital design lab8’, ‘Digital design lab9’ in Sakai site.

3. Verilog: http://www.verilog.com

EXERCISE SPECIFICATION

TASK1:

Implement a full subtractor (described on question 8 of Part 1 in this document) with two 4x1 multiplexer. Write a circuit to realize this function and test.

- Do the design.
- Write testbench to verify the function of your design.
- Create the constraint file.
- Do the synthetic and implementation, generate the bitstream file and program the device, then test on the Minisys / EGO1 develop board.

TASK2:

I Implement an ABCD-to-seven-segment decoder (described on question 5 of Part 1 in this document) with decoders and gates.

- Do the design.
- Write testbench to verify the function of your design.
- Create the constraint file
- Do the synthetic and implementation, generate the bitstream file and program the device, then test on Minisys /EGO1 the develop board

SUBMISSION

Submit your assignment report to the Sakai on *Corresponding site* “Digital Design fall2019” by the deadline.

ASSESSEMENT

The full marks for this exercise is 100 and they are distributed as follows:

Theory: 50%

Question 1	2
Question 2	7
Question 3	2*(2*3)
Question 4	2*3
Question 5	2*3
Question 6	2*3
Question 7	2*3
Question 8	2*2
Question 9	1
Total	50 marks

Lab: 50%

Task 1: Design in Verilog, the truth-table Verilog code should include the 74151 and the full subtractor	1+4 marks
Task 1: Test bench in Verilog, simulation result	5*2 marks
Task 1: Constrains file, the description of the test result on Minisys/EGO1 practice board	5*2 marks
Task 2: Design in Verilog, the truth-table Verilog code should include the decoder and the ABCD-to-7 segment	1+4 marks
Task 2: Test bench in Verilog, simulation result	5*2 marks
Task 2: Constrains file and the description of the test result on Minisys/EGO1 practice board	5*2 marks
Total	50 marks

The template for the report is provided in the next pages.

DIGITAL DESIGN

ASSIGNMENTREPORT

ASSIGNMENT ID : xxxx

Student Name: xxxx

Student ID: xxxx

PART 1: DIGITAL DESIGN THEORY

Provide your answers here:

PART 2: DIGITAL DESIGN LAB (TASK1)

DESIGN

Describe the design of your system by providing the following information:

- *Verilog design (provide the Verilog code)*
- *Truth-table*

SIMULATION

Describe how you build the test bench and do the simulation.

- *Using Verilog(provide the Verilog code)*
- *Wave form of simulation result (provide screen shots)*
- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation.*

CONSTRAINT FILE AND THE TESTING

Describe how you test your design on the Minisys Practice platform.

- *Constraint file (provide the screen shots on the feature of a pin and the binding info between pins and the input /output ports)*
- *The testing result (provide the screen shots (at least 3 testing scene) to show state of inputs and outputs along with the related descriptions.*

THE DESCRIPTION OF OPERATION

Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.

- *Problems and solutions*

PART 2: DIGITAL DESIGN LAB (TASK2)

DESIGN

Describe the design of your system by providing the following information:

- *Verilog design while using data flow (provide the Verilog code)*
- *Verilog design while using structured design (provide the Verilog code)*
- *Block design (provide screen shots)*
- *Truth-table*

SIMULATION

Describe how you build the test bench and do the simulation.

- *Using Verilog (provide the Verilog code)*
- *Wave form of simulation result (provide screen shots)*
- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation*

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Describe how you test your design on the Minisys Practice platform.

- *Constraint file (provide the screen shots on the feature of a pin and the binding info between pins and the input /output ports)*
- *The testing result (provide the screen shots (at least 3 testing scene)) to show state of inputs and outputs along with the related descriptions.*

THE DESCRIPTION OF OPERATION

Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.

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