DIGITAL DESIGN

ASSIGNMENT 4

Deadline: *22:55, Tuesday 3 December 2019*

Lab sessions & Location:

1. **Lychee Garden 6, Room 406 (Wednesday 16:20-18:10 pm)**
2. **Lychee Garden 6, Room 408 (Wednesday 19:00-20:50 pm)**
3. **Lychee Garden 6, Room 402 (Thursday 8:00-9:50 am)**
4. **Lychee Garden 6, Room 402 (Thursday 10:10~12:10 am)**

Teaching Assistant:

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PART 1: DIGITAL DESIGN THEORY

Provide answers to the following questions:

1. Write down the characteristic tables of both JK flip-flop and T flip-flop. Based on the truth table, write down their characteristic equations. (Use character T, J, K, Q, Q_{t+1})
2. A sequential circuit has two JK flip-flops A and B, two inputs x and y, and one output z. The input and output equations are:

$$J_A = Bx + B'y' \qquad K_A = B'xy' \qquad J_B = A'x \qquad K_B = A + xy'$$

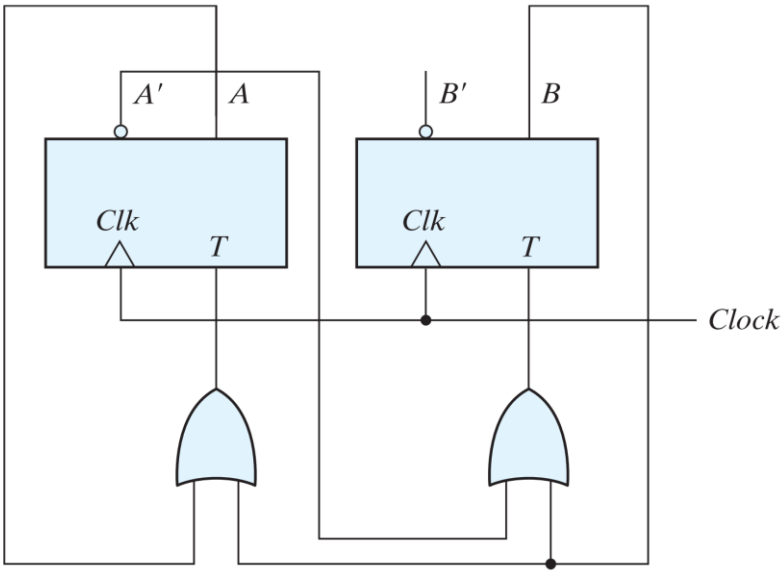
$$z = Ax'y' + Bx'y'$$

   (a) Draw the circuit diagram.

   (b) Write down the state table.

   (c) Derive the state equations for A and B.

3. Use a D flip-flop, a 2x1 multiplexer, and a NOT gate to build a JK flip-flop. Draw the circuit diagram. Explain your design.
4. Derive the state table and the state diagram of the sequential circuit shown in the figure below. Explain the function that the circuit performs.



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PART 2: DIGITAL DESIGN LAB

INTRODUCTION

In this lab, you are required to use Vivado 2017.4 and Minisys/EGO1 Practice platform (xilinx FPGA chip artix 7 inside) to design a combinational Sequential circuit and test it.

PREAMBLE

Before working on the course-work itself, you should master the following material.

1.' CH5-Synchronous Sequential Logic-SUSTC.ppt' in Sakai site.

2. 'Digital design lab10.pdf', 'Digital design lab11.pdf' in Sakai site.

3. Verilog: http://www.verilog.com

EXERCISE SPECIFICATION

TASK1:

Implement a T Flip Flop with gates. Write a circuit to realize this function and test.

- Do the design (using structure design is suggested).
- Write testbench to verify the function of your design.
- Create the constraint file.
- Do the synthetic and implementation, generate the bitstream file and program the device, then test on the Minisys / EGO1 develop board.

TASK2:

Implement a circuit with 3 inputs (x_in(5bit-width), clk and an asynchronous reset) and 1 output (y_out (its bit-width is determined by the circuit designer)). If the asynchronous reset is valid, then state of y_out is A, otherwise the circuit get the value of x_in at every posedge of clk, If the total number of received 1 in x_in is a

multiple of 2, then the state of y_out is B, otherwise the state of y_out is C.(the coding on A,B and C is determined by the circuit designer)

- Do the design by using FSM (DO NOT using 1-stage) in verilog.
- Write testbench to verify the function of your design.
- Create the constraint file
- Do the synthetic and implementation, generate the bitstream file and program the device, then test on Minisys /EGO1 the develop board

SUBMISSION

Submit your assignment report to the Sakai on *Corresponding site* “Digital Design fall2019” by the deadline.

ASSESSEMENT

The full marks for this exercise is 100 and they are distributed as follows:

Theory: 40%

Question 1	2.5 *4
Question 2	5*2
Question 3	5*2
Question 4	4+4+2
Total	40 marks

Lab: 60%

Task 1: Design in Verilog by using structure	10marks
Task 1: Test bench in Verilog, simulation result and the description on the simulation result	4+4+2 marks
Task 1: Constrains file, the description of the test result on Minisys/EGO1 practice board	5*2 marks
Task 2: Design in Verilog by using FSM	10 marks

Task 2: Test bench in Verilog, simulation result and the description on the simulation result	4+4+2 marks
Task 2: Constrains file and the description of the test result on Minisys/EGO1 practice board	5*2 marks
Total	60 marks

The template for the report is provided in the next pages.

DIGITAL DESIGN

ASSIGNMENTREPORT

ASSIGNMENT ID: xxxx

Student Name: xxxx

Student ID: xxxx

PART 1: DIGITAL DESIGN THEORY

Provide your answers here:

PART 2: DIGITAL DESIGN LAB (TASK1)

DESIGN

Describe the design of your system by providing the following information:

- *Verilog design (provide the Verilog code)*
- *Truth-table*

SIMULATION

Describe how you build the test bench and do the simulation.

- *Using Verilog (provide the Verilog code)*
- *Wave form of simulation result (provide screen shots)*
- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation.*

CONSTRAINT FILE AND THE TESTING

Describe how you test your design on the Minisys Practice platform.

- *Constraint file (provide the screen shots on the feature of a pin and the binding info between pins and the input /output ports)*
- *The testing result (provide the screen shots (at least 3 testing scene) to show state of inputs and outputs along with the related descriptions.*

THE DESCRIPTION OF OPERATION

Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.

- *Problems and solutions*

PART 2: DIGITAL DESIGN LAB (TASK2)

DESIGN

Describe the design of your system by providing the following information:

- *Verilog design while using data flow (provide the Verilog code)*
- *Verilog design while using structured design (provide the Verilog code)*
- *Block design (provide screen shots)*
- *Truth-table*

SIMULATION

Describe how you build the test bench and do the simulation.

- *Using Verilog (provide the Verilog code)*
- *Wave form of simulation result (provide screen shots)*
- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation*

CONSTRAINT FILE AND THE TESTING

Describe how you test your design on the Minisys Practice platform.

- *Constraint file (provide the screen shots on the feature of a pin and the binding info between pins and the input /output ports)*
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THE DESCRIPTION OF OPERATION

Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.

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