DIGITAL DESIGN

ASSIGNMENT 2

Deadline: *22:55, Tuesday 12 November 2019*

Lab sessions & Location:

1. **Lychee Garden 6, Room 406 (Wednesday 16:20-18:10 pm)**
2. **Lychee Garden 6, Room 408 (Wednesday 19:00-20:50 pm)**
3. **Lychee Garden 6, Room 402 (Thursday 8:00-9:50 am)**
4. **Lychee Garden 6, Room 402 (Thursday 10:10~12:10 am)**

Teaching Assistant:

Wang Wei, email: wangw6@sustech.edu.cn

Hua Zheng Chang, email: huazc@mail.sustech.edu.cn

PART 1: DIGITAL DESIGN THEORY

Provide answers to the following questions:

1. Convert the following binary numbers to hexadecimal and to decimal:
   (a) 1.10101,
   (b) 1101.01
   How many times the decimal answer in (b) is larger than that in (a)? Explain why.
2. Do the following conversion problems:
   (a) Convert decimal 37.875 to binary.
   (b) Calculate the binary equivalent of 1/7 out to eight places. Then convert from binary to decimal. How close is the result to 1/7?
   (c) Convert the binary result in (b) into hexadecimal. Then convert the result to decimal. Is the answer the same?
3. Represent the decimal number 7814 in (a) BCD, (b) excess-3 code, (c) 2421 code, and (d) 6311 code.
4. We can perform logical operations on strings of bits by considering each pair of corresponding bits separately (called bitwise operation). Given two eight-bit strings A = 10110101 and B = 00011100, evaluate the eight-bit result after the following logical operations: (a) AND (b) OR (c) XOR (d) NOT A (e) NOT B (f) NAND (g) NOR
5. Simplify the following Boolean expressions to a minimum or the indicated number of literals:
   a. (a + b + c')(a'b'+ c)
   b. a'b'c + ab'c + abc + a'bc
   c. (a + c)(a'+ b + c)(a'+ b'+ c)
   d. A'BD' + ABC'D'+ ABCD' to two literals
6. Given the Boolean functions F1 and F2 , show that
   a. The Boolean function E = F1 + F2 contains the sum of the minterms of F1 and F2

b. The Boolean function G = F1 · F2 contains only the minterms that are common to F1 and F2 .

7. Convert each of the following to the other canonical form.
   a. F(x, y, z) = ∑(1, 3, 5, 7)
   b. F(A, B, C, D) = ∏(3, 5, 8, 11, 13, 15)
8. Write the following Boolean expressions in:
   a. (b + d)(a'+ b'+ c)(a + c) SOP form
   b. a'b + a'c'+ bc POS form
9. Determine whether the following Boolean equation is true or false.
   a. y'z' + yz' + x'z = x'+ xz
   b. x'y'+ xz'+ yz = y'z' + xy + x'z
10. Simplify the following Boolean functions, using Karnaugh maps:
   a. F (w, x, y, z) = ∑(11, 12, 13, 14, 15)
   b. F (w, x, y, z) = ∑(8, 10, 12, 13, 14)
11. Simplify the following Boolean functions and expressions, using four-variable maps:
   a. F (A, B, C, D) = ∑ (2, 3, 6, 7, 12, 13, 14)
   b. F (w, x, y, z) = ∑ (1, 3, 4, 5, 6, 7, 9, 11, 13, 15)
   c. A'BCD + ABC + CD + B'D
   d. A'B'C'D' + BC'D + A'C'D + A'BCD + ACD
12. Implement the following logical functions with two-level NAND gate circuits. Write down the simplification process.
   a. F(A, B, C, D) = AD + BC'D+ ABC + A'BC'D
   b. F(A, B, C, D) = A'B'C'D + CD' + AC'D
   c. F(A, B, C, D)= (A'+ C'+ D')(A'+ C')(C'+ D')
   d. F(A, B, C, D) = A'+ AB + B'C + ACD

PART 2: DIGITAL DESIGN LAB

INTRODUCTION

In this lab, you are required to use Vivado 2017.4 and Minisys/EGO1 Practice platform (xilinx FPGA chip artix 7 inside) to design a combinational logic circuit and test it.

PREAMBLE

Before working on the coursework itself, you should master the following material.

1.‘Ch2-Boolean Algrebra-ICs-SUSTC.ppt’ and CH3-Minimisation-SUSTC ‘ in Sakai site.

2. ‘Digital design lab6’, ‘Digital design lab7’ and ‘Digital design lab8’ in Sakai site.

3. Verilog: http://www.verilog.com

EXERCISE SPECIFICATION

TASK1:

There are 4 wards, which are numbered from 1 to 4 respectively, among which the #1 ward has the lowest priority, and the #4 has the highest priority (Priority increases as the number increases). Each room has a call bell, it can be turn on and turn off. In the main control room there is a 7-seg tube which shows the ID of the room whose bell is on with the highest priority. Write a circuit to realize this function and test.

- Do the design.
- Write testbench to verify the function of your design.
- Create the constraint file.
- Do the synthetic and implementation, generate the bitstream file and program the device, then test on the Minisys/EGO1 develop board.

TASK2:

Implement a 4-16 decoder by two 3-8 decoders. You can either modify the provided 3-8 decoder in the or design 74138 decoder

- Do the design.
- Write testbench to verify the function of your design.
- Create the constraint file

- Do the synthetic and implementation, generate the bitstream file and program the device, then test on Minisys/EGO1 the develop board

SUBMISSION

Submit your assignment report to the Sakai on *Corresponding site* “Digital Design fall2019” by the deadline.

ASSESSEMENT

The full marks for this exercise is 100 and they are distributed as follows:

Theory: 40%

Question 1	3
Question 2	3
Question 3	2
Question 4	4
Question 5	4
Question 6	2
Question 7	2
Question 8	2
Question 9	2
Question 10	4
Question 11	6(4*1.5)
Question 12	6(4*1.5)
Total	40 marks

Lab: 60%

Task 1: Design in Verilog, the truth-table	5*2 marks
Task 1: Test bench in Verilog, simulation result	5*2 marks

Task 1: Constrains file, the description of the test result on Minisys/EGO1 practice board	5*2 marks
Task 2: Design in Verilog, the truth-table	5*2 marks
Task 2: Test bench in Verilog, simulation result	5*2 marks
Task 2: Constrains file and the description of the test result on Minisys/EGO1 practice board	5*2 marks
Total	60 marks

The template for the report is provided in the next pages.

DIGITAL DESIGN

ASSIGNMENTREPORT

ASSIGNMENT ID : xxxx

Student Name: xxxx

Student ID: xxxx

PART 1: DIGITAL DESIGN THEORY

Provide your answers here:

PART 2: DIGITAL DESIGN LAB (TASK1)

DESIGN

Describe the design of your system by providing the following information:

- *Verilog design (provide the Verilog code)*
- *Truth-table*

SIMULATION

Describe how you build the test bench and do the simulation.

- *Using Verilog(provide the Verilog code)*
- *Wave form of simulation result (provide screen shots)*
- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation.*

CONSTRAINT FILE AND THE TESTING

Describe how you test your design on the Minisys Practice platform.

- *Constraint file (provide the screen shots on the feature of a pin and the binding info between pins and the input /output ports)*
- *The testing result (provide the screen shots (at least 3 testing scene) to show state of inputs and outputs along with the related descriptions.*

THE DESCRIPTION OF OPERATION

Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.

- *Problems and solutions*

PART 2: DIGITAL DESIGN LAB (TASK2)

DESIGN

Describe the design of your system by providing the following information:

- *Verilog design while using data flow (provide the Verilog code)*
- *Verilog design while using structured design (provide the Verilog code)*
- *Block design (provide screen shots)*
- *Truth-table*

SIMULATION

Describe how you build the test bench and do the simulation.

- *Using Verilog (provide the Verilog code)*
- *Wave form of simulation result (provide screen shots)*
- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation*

CONSTRAINT FILE AND THE TESTING

Describe how you test your design on the Minisys Practice platform.

- *Constraint file (provide the screen shots on the feature of a pin and the binding info between pins and the input /output ports)*
- *The testing result (provide the screen shots (at least 3 testing scene)) to show state of inputs and outputs along with the related descriptions.*

THE DESCRIPTION OF OPERATION

Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.

- *Problems and solutions*