DIGITAL DESIGN

ASSIGNMENT 5

Deadline: *22:55, Thursday 19 December 2019*

Lab sessions & Location:

1. **Lychee Garden 6, Room 406 (Wednesday 16:20-18:10 pm)**
2. **Lychee Garden 6, Room 408 (Wednesday 19:00-20:50 pm)**
3. **Lychee Garden 6, Room 402 (Thursday 8:00-9:50 am)**
4. **Lychee Garden 6, Room 402 (Thursday 10:10~12:10 am)**

Teaching Assistant:

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PART 1: DIGITAL DESIGN THEORY

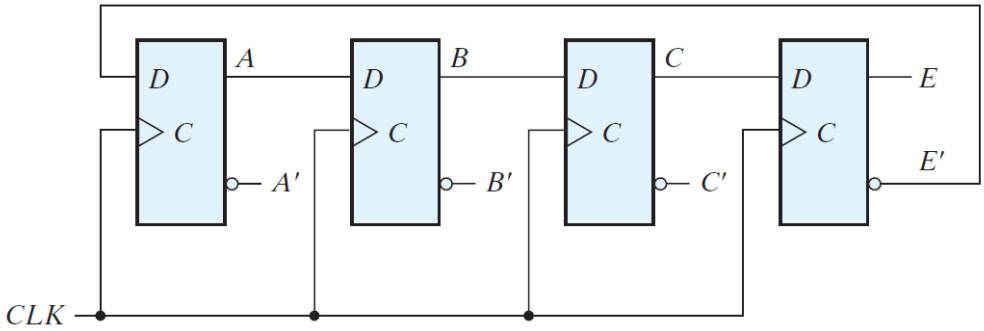
Provide answers to the following questions:

1. What is the difference between serial and parallel transfer? Explain how to convert serial data to parallel and parallel data to serial.
2. Design a four-bit shift left register with parallel load using D flip-flops and gates. There are two control inputs: *shift* and *load*. When *shift* = 1, the content of the register is shifted by one position. New data are transferred into the register when *load* = 1 and *shift* = 0. If both control inputs are equal to 0, the content of the register does not change. Briefly describe your design and draw the circuit diagram.
3. Design a serial 2's complementer with a shift register, a flip-flop and gates. The binary number is shifted out from one side and it's 2's complement shifted into the other side of the shift register. Provide the state diagram and draw the circuit diagram.

   Hint: - 2's complement of a number can be obtained by keeping the least significant bits as such until the first 1, and then complementing all bits

   eg: 001010 → 110110

4. List the all unused states in a 4-bit switch-tail ring counter show in the figure below. Determine the next state for each of these states and show that, if the counter finds itself in an invalid state, it does not return to a valid state. Modify the circuit to avoid this. Show that your modified counter produces the same sequence of states and that the circuit reaches a valid state from any one of the unused states.



PART 2: DIGITAL DESIGN LAB

INTRODUCTION

In this lab, you are required to use Vivado 2017.4 and Minisys/EGO1 Practice platform (Xilinx FPGA chip Artix 7 inside) to design a Sequential circuit and test it.

PREAMBLE

Before working on the course-work itself, you should master the following material.

1. ’CH6-Registers and Counters-SUSTC.ppt’ in Sakai site.
2. ‘Digital design lab12.pdf’, ‘Digital design lab13.pdf’, ‘Digital design lab14.pdf’ in Sakai site.
3. Verilog: http://www.verilog.com

EXERCISE SPECIFICATION

TASK1:

Use two 74194 shift register to implement a 8-bit serial-parallel converter. Write a circuit to realize this function and test.

- Do the design (Using structure design is suggested).
- Write testbench to verify the function of your design.
- Create the constraint file.

- Do the synthetic and implementation, generate the bitstream file and program the device, then test on the Minisys / EGO1 develop board.

TASK2:

Using JK flip-flops, design a counter with the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6.

- Do the design in Verilog.
- Write testbench to verify the function of your design.
- Create the constraint file
- Do the synthetic and implementation, generate the bitstream file and program the device, then test on Minisys /EGO1 the develop board

SUBMISSION

Submit your assignment report to the Sakai on *Corresponding site* “Digital Design fall2019” by the deadline.

ASSESSEMENT

The full marks for this exercise are 100 and they are distributed as follows:

Theory: 40%

Question 1	4+6
Question 2	10
Question 3	10
Question 4	10
Total	40 marks

Lab: 60%

Task 1: Design in Verilog, block diagram	5+5marks
Task 1: Test bench in Verilog, simulation result and the description on the simulation result	4+4+2 marks
Task 1: Constrains file, the description of the test result on Minisys/EGO1 practice board	5*2 marks
Task 2: Design in Verilog, block diagram	5+5 marks
Task 2: Test bench in Verilog, simulation result and the description on the simulation result	4+4+2 marks
Task 2: Constrains file and the description of the test result on Minisys/EGO1 practice board	5*2 marks
Total	60 marks

The template for the report is provided in the next pages.

DIGITAL DESIGN

ASSIGNMENTREPORT

ASSIGNMENT ID: xxxx

Student Name: xxxx

Student ID: xxxx

PART 1: DIGITAL DESIGN THEORY

Provide your answers here:

PART 2: DIGITAL DESIGN LAB (TASK1)

DESIGN

Describe the design of your system by providing the following information:

- *Verilog design (provide the Verilog code)*
- *Block diagram of your design*

SIMULATION

Describe how you build the test bench and do the simulation.

- *Using Verilog (provide the Verilog code)*
- *Wave form of simulation result (provide screen shots)*
- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation.*

CONSTRAINT FILE AND THE TESTING

Describe how you test your design on the Minisys/EGO1 Practice platform.

- *Constraint file (provide the screen shots on the feature of a pin and the binding info between pins and the input /output ports)*
- *The testing result (provide the screen shots (at least 3 testing scene) to show state of inputs and outputs along with the related descriptions.*

THE DESCRIPTION OF OPERATION

Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.

- *Problems and solutions*

PART 2: DIGITAL DESIGN LAB (TASK2)

DESIGN

Describe the design of your system by providing the following information:

- *Verilog design (provide the Verilog code)*
- *Block diagram of your design*

SIMULATION

Describe how you build the test bench and do the simulation.

- *Using Verilog (provide the Verilog code)*
- *Wave form of simulation result (provide screen shots)*
- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation*

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