

**DIGITAL DESIGN**

**ASSIGNMENT 1**

**Deadline: *22:55, Tuesday 8 October 2019***

**Lab sessions&Location:**

1. **Lychee Garden 6, Room 406 (Wednesday 16:20-18:10 pm)**
2. **Lychee Garden 6, Room 408 (Wednesday 19:00-20:50 pm)**
3. **Lychee Garden 6, Room 402 (Thursday 8:00-9:50 am)**
4. **Lychee Garden 6, Room 402 (Thursday 10:10~12:10 am)**

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## PART 1: DIGITAL design THEORY

Provide answers to the following questions:

1. List the octal and hexadecimal numbers from 12 to 28. Using A, B, C and D for the last four digits, list the numbers from 12 to 28 in base 14.
2. What is the largest signed and unsigned binary number that can be expressed with 14 bits? What are the equivalent decimal and hexadecimal numbers?
3. Convert the decimal number 240 to binary in two ways: (a) convert directly to binary; (b) convert first to hexadecimal and then from hexadecimal to binary. Which method is faster?
4. Describe the three basic types of logic calculation (write the truth table).
5. Give the 1s’ and 2s’ complement code of the following decimal numbers, the answer should be 32 bit-width in hexadecimal notation.

a. 14274836

b. -27854048

## PART 2: DIGITAL design lab

##### Introduction

In this lab, you are required to use Vivado 2017.4 and Minisys Practice platform (xilinx FPGA chip artix 7 inside) to design a simple logic circuit: Do the addition on two unsigned 2bit numbers, do the simulation and verify its function on the board. You should submit the description of the operation steps, the Verilog design, the wave form from the simulation, and the on board testing steps and results.

##### Preamble

Before working on the coursework itself, you should master the following material. A separate tutorial document (on the Sakai site) has be provided to you which includes:

* Vivado: The Vivado software provides a complete design environment for system-on-a-programmable-chip (SOPC) design. Regardless of whether you use a personal computer or a Linux workstation, Vivado ensures easy design entry, fast processing, and straightforward device programming.
* Minisys Practice platform: a platform designed for Digital design ,Principles of Computer Organization and many other courses. This platform include FPGA chip ,storage chip and lots of Dial switches, LEDs for input and output.
* Verilog : standardized as IEEE 1364, is a [hardware description language](https://en.wikipedia.org/wiki/Hardware_description_language) (HDL) used to model [electronic systems](https://en.wikipedia.org/wiki/Electronic_system). It is most commonly used in the [design and verification](https://en.wikipedia.org/w/index.php?title=Design_and_verification&action=edit&redlink=1) of [digital circuits](https://en.wikipedia.org/wiki/Digital_electronics) at the [register-transfer level](https://en.wikipedia.org/wiki/Register-transfer_level) of [abstraction](https://en.wikipedia.org/wiki/Abstraction_(computer_science)). It is also used in the verification of [analog circuits](https://en.wikipedia.org/wiki/Analogue_electronics) and [mixed-signal circuits](https://en.wikipedia.org/wiki/Mixed-signal_integrated_circuit), as well as in the design of [genetic circuits](https://en.wikipedia.org/w/index.php?title=Genetic_circuit&action=edit&redlink=1). http://www.verilog.com/

##### Exercise specification

**TASK1:**

Create a project named as Lab2\_Addition, design the source code to get the addition of two input numbers: one is 2bit and another is 1bit. do the simulation and generate the bitstream which is used to program the FPGA chip and verify your design.

Note: there should be two inputs (we need input two operands through dial switch) and three outputs (three led groups needed to demonstrate the value of two operands and the result)

***module*** *Lab2\_Addition(addend, augend, addend\_led, augend\_led, sum\_led);*

*input [1:0] addend;*

*input augend;*

*output [1:0]addend\_led;*

*output augend\_led;*

*output [2:0] sum\_led;*

*……*

***endmodule***

You will focus on how to use Vivado to do the design, simulation, generate the bitstream file which is used to program the FPGA chip (a part of the Minisys practice platform), you will also learn some basic concepts of Verilog. The steps you need to follow are:

1. Create an empty project.
2. Edit a design file (Verilog file) & add it to the project.
3. Edit a simulation file (Verilog file) & add it to the project.
4. Do the simulation using to verify if the function of design is ok. If not, modify your design and do the simulation again.
5. Do the synthesize.
6. Edit a constraints file (to define the Specifications of pins and the binding info between pins and the designed ports) & add it to the project.
7. Do the implementation.
8. Generate the bitstream file.
9. Turn on the board (Minisys & FPGA chip inside) and connect Vivado to the board
10. Program the device with the bitstream
11. Test the design on the board (using dial switch as input, using led to see the state of output)

**TASK2:**

1. Do the design using data flow, block style and structured style respectively (While doing the design with structured style, It is optional to use primitive or encapsulated IP) to verify the following theorem (you can find the design on the lab3 and lab4 courseware as a reference):

**DeMorgan**: a) **(x+y)’ = x’y’**  b) **(xy)’ = x’+y’**

1. Create a test bench, do the simulation to verify the function of the design.
2. Edit a constraints file (to define the Specifications of pins and the binding info between pins and the designed ports) & add it to the project.
3. Do the synthesis and implementation.
4. Generate bitstream file, program the device with the bitstream
5. Test the design on the board (using dial switch as input, using led to see the state of output).

**TIPS:**

1. Putting all the circuit ( (x+y)’ , x’y’ ,(xy)’ and x’+y’) to one design file, and naming ports in different design file(corresponding to the different design style) with same name so that you can reuse the testbench file and constraint file with just a little modification (as in labs courseware, just modify the module name in your design file).
2. Namingthe file:
   1. For data flow design, the source file should be demorgan\_df.v
   2. For block design, source file should be demorgan\_bd.bd
   3. For structured design, the source file should be demorgan\_sd.v
3. All the 3 design could share the same test bench file because the number and name of ports are same while only name of module are different. If you want use test bench file of demorgan\_df.v on demorgan\_bd.bd ,just change the module name from demorgan\_df to demorgan\_bd is enough.
4. All the 3 design could also share the same constrain file because the number and name of ports are the same.

##### SUBMISSION

Submit your assignment report to the Sakai on *Corresponding site* by the deadline.

“Digital Design fall2019”

##### Assessement

The full marks for this exercise is 100 and they are distributed as follows:

**Theory: 20%**

|  |  |
| --- | --- |
| Question 1 | 4 |
| Question 2 | 4 |
| Question 3 | 4 |
| Question 4 | 4 |
| Question 5 | a: 2 marks, b:2 marks |
| Total | 20 marks |

**Lab: 80%**

|  |  |
| --- | --- |
| Task 1: Design in Verilog, the truth-table | 5\*2 marks |
| Task 1: Test bench in Verilog, simulation result | 5\*2 marks |
| Task 1: Constrains file, the description of the test result on Minisys practice board | 5\*2 marks |
| Task 2: Design with data-flow style, design with block-design style, design with structure-design style, the truth-table | 5\*4 marks |
| Task 2: Test bench in Verilog, simulation result | 5\*2 marks |
| Task 2: Constrains file and the description of the test result on Minisys practice board | 5\*2 marks |
| Problems and solutions | 5\*2 marks |
| Total | 80 marks |

The template for the report is provided in the next pages.



**DIGITAL DESIGN**

**ASSIGNMENTREPORT**

**ASSIGNMENT ID : xxxx**

**Student Name: xxxx**

**Student ID: xxxx**

PART 1: DIGITAL design THEORY

Provide your answers here:

PART 2: DIGITAL design LAB (Task1)

##### Design

*Describe the design of your system by providing the following information:*

* *Verilog design (provide the Verilog code)*
* *Truth-table*

##### simulation

*Describe how you build the test bench and do the simulation.*

* *Using Verilog(provide the Verilog code)*
* *Wave form of simulation result (provide screen shots)*
* *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation.*

##### Constraint file and the testing

*Describe how you test your design on the Minisys Practice platform.*

* *Constraint file (provide the screen shots on the feature of a pin and the binding info between pins and the input /output ports)*
* *The testing result (provide the screen shots (at least 3 testing scene) to show state of inputs and outputs along with the related descriptions.*

##### the description of operation

*Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.*

* *Problems and solutions*

PART 2: DIGITAL design LAB (Task2)

##### Design

*Describe the design of your system by providing the following information:*

* *Verilog design while using data flow (provide the Verilog code)*
* *Verilog design while using structured design (provide the Verilog code)*
* *Block design (provide screen shots)*
* *Truth-table*

##### simulation

*Describe how you build the test bench and do the simulation.*

* *Using Verilog (provide the Verilog code)*
* *Wave form of simulation result (provide screen shots)*
* *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation*

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* *Problems and solutions*