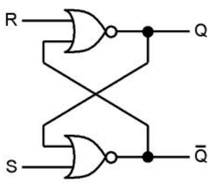
1. More on latches
    a. S-R NOR latch below



Circuit Diagram

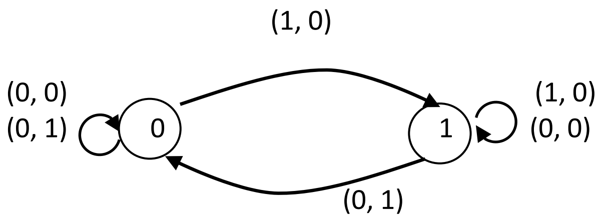
S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	Undefined

Characteristic Table

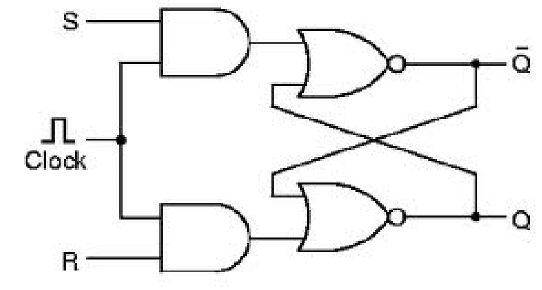
b. State transition table for S-R NOR latch
    i. State transition table for sequential circuits similar to truth table for combinational circuits
    ii. Need to list out all possible current states and inputs, like below
        1. Combination of inputs and present state form entire list of possible outcomes
        2. Same as a regular truth table, just need to consider present state as well

State Transition Table for S-R NOR Latch				
Present Inputs		**Present State**	**Next State**	**Type of Circuit**
S	**R**	**Q**	**Q’**	
0	0	0	0	Memory
0	0	1	1	Memory
0	1	0	0	Combinational
0	1	1	0	Combinational
1	0	0	1	Combinational
1	0	1	1	Combinational
1	1	0	?	Combinational
1	1	1	?	Combinational

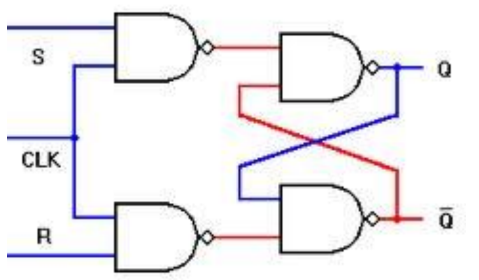
c. State transition diagram
    i. Visual representation of circuit’s output based on current state and input
        1. The values in the circles are Q, the output of the latch
        2. The values in parentheses (0, 1) are the combination of (S, R) respectively
        3. The arrows are transitions from one state to the next (or staying in the same state)
    ii. For every state, all possible output combinations need to be listed
        1. All possible transitions from a state to other states (or the same state)
        2. (1, 1) isn’t listed below as it leads to undefined behavior



2. Other latches
    a. Clocking the latches
        i. Prevent the latch from changing, except at specific times as determined by the clock

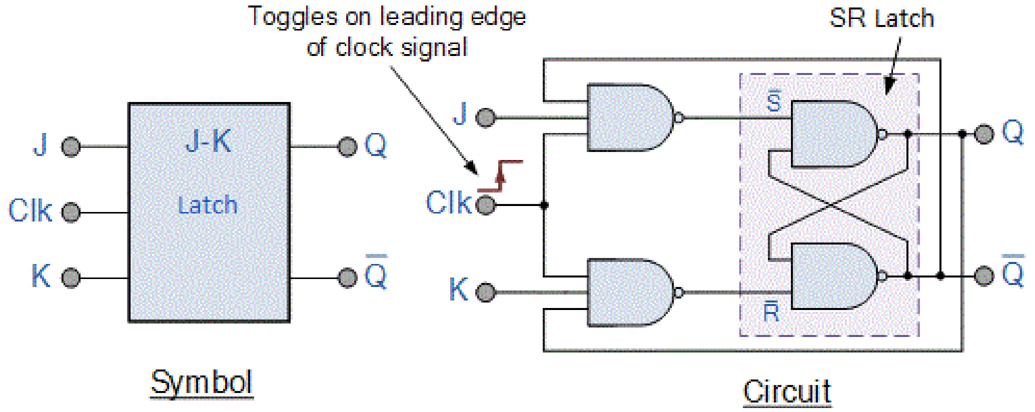


Clocked S-R NOR Latch

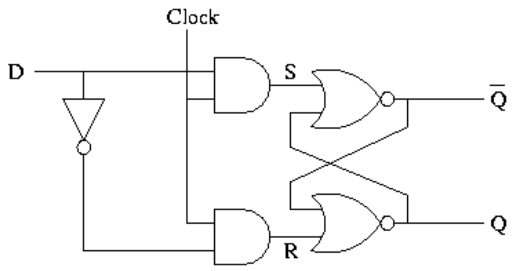


Clocked S-R NAND Latch

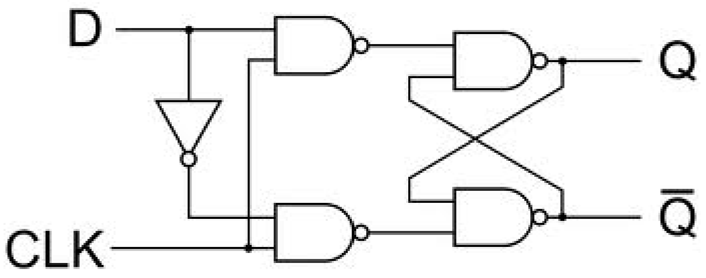
    b. Clocked J-K latch
        i. Like a S-R latch
            1. However, passing in (S, R) = (1, 1) toggles/inverts Q
                a. Doesn't lead to undefined behavior
            2. Uses feedback from outputs to do so



    b. Clocked D latch
        i. Only takes one input, ensures that inputs that cause unpredictable states don't occur
        ii. Output of latch is equal to the most recent value applied to the input
            1. When clock is 1, sample the current value of D
            2. Store that value in the latch
            3. Can retrieve the value at output Q

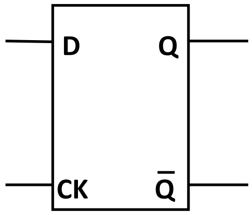
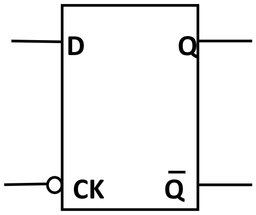
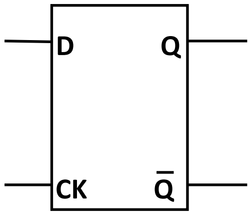
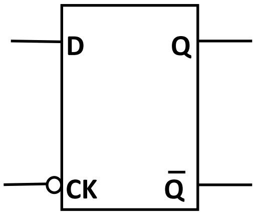


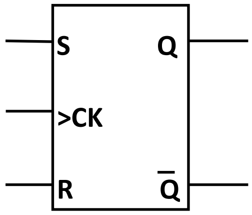
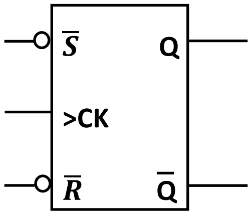
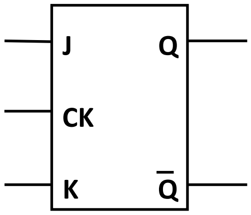
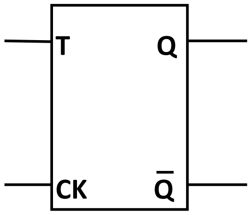
Clocked NOR D Latch



Clocked NAND D Latch

2. Flip-flops
    a. Circuit terminology
        i. Level sensitive – output controlled by the level of the clock input
        ii. Edge triggered – output changes only when the clock changes from one value to the other
            1. Positive / rising edge – when clock “rises” from 0 to 1
            2. Negative / falling edge – when clock “falls” from 1 to 0
    b. Back to flip-flops
        i. Clocked (gated) latches are level sensitive
        ii. Unlike latches, flip flops are edge-triggered
        iii. Named so because they flip and flop from one stable state (0) to another (1)
    c. Advantages
        i. Signal on input pin captured as soon as the clock changes
        ii. Subsequent changes of the input are ignored until clock changes again
        iii. Better timing control on complex circuits
    d. Disadvantage
        i. More complicated than a latch
            1. Benefits outweigh this drawback, though
    e. Types of flip flops

			
Positive D Latch	**Negative D Latch**	**Rising Edge D Flip-Flop**	**Falling Edge D Flip-Flop**
Can change when the clock is high.	Can change when the clock is low.	Can change when clock goes from 0 to 1.	Can change when clock goes from 1 to 0.

	 $\overline{S}$ Q >CK $\overline{R}$ $\overline{Q}$		
S-R Flip-Flop (NOR)	**S-R Flip-Flop (NAND)**	**J-K Flip-Flop**	**T Flip-Flop**

S	**R**	***Q(t + 1)***
0	0	*Q(t)*
0	1	0
1	0	1
1	1	Undefined

S	**R**	***Q(t + 1)***
0	0	Undefined
0	1	1
1	0	0
1	1	*Q(t)*

J	**K**	***Q(t + 1)***
0	0	*Q(t)*
0	1	0
1	0	1
1	1	$\overline{Q}(t)$

T	***Q(t + 1)***
0	*Q(t)*
1	$\overline{Q}(t)$

    f. Named flip flops work similarly to their latch counterparts
        i. One new addition – T flip flop
        ii. When T is high, on next clock the output is “toggled” and is inverted
        iii. Same as (1, 1) input on J-K flip flop and latch

3. Flip flop timing terminology
    a. Setup time t_{su}
        i. Minimum time before clock arrives that inputs must be stable and unchanging to ensure first latch in flip flop is stable
    b. Hold time t_h
        i. Minimum time after clock arrives that inputs must remain stable and unchanging to ensure first latch clock NAND is off
        ii. Not important for this course, but exists