<ol> <li>Fully associative (FA) cache</li> </ol>	1.
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a. Won't have conflicts like with a DM cache

b. However, extremely expensive to implement in terms of both power and money

- c. Example
  - i. Same cache parameters as before, except now a FA cache
  - ii. 8-byte FA cache with line size of 2, and 4-bit address

ſ	Tag	Set	Offset	Address Bits
				=
				=

## 27 FA caches, SA caches, cache replacement and write policies

- 2. Set associative (SA) caches
  - a. Compromise between DM and FA
  - b. N-way SA cache

c. Advantages and disadvantages of both DM and FA

- d. Example
  - i. Same cache parameters as before, except now a 2-way SA cache
  - ii. 8-byte 2-way SA cache with line size of 2, and 4-bit address

Tag	Set	Offset	Address Bits
			=
			_

3.	Cache	ren	lacement	algorithi	mς
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- a. How do we evict lines from a given set for non-DM caches?
- b. Least recently used (LRU)
- c. First in, first out (FIFO)
- d. Least frequently used (LFU)
- e. Random

## 4. Cache write policies

- a. If we change values that reside in main memory, we make changes in cache first
- b. What happens when we need to evict a line?
- c. Write-back

d. Write-through

