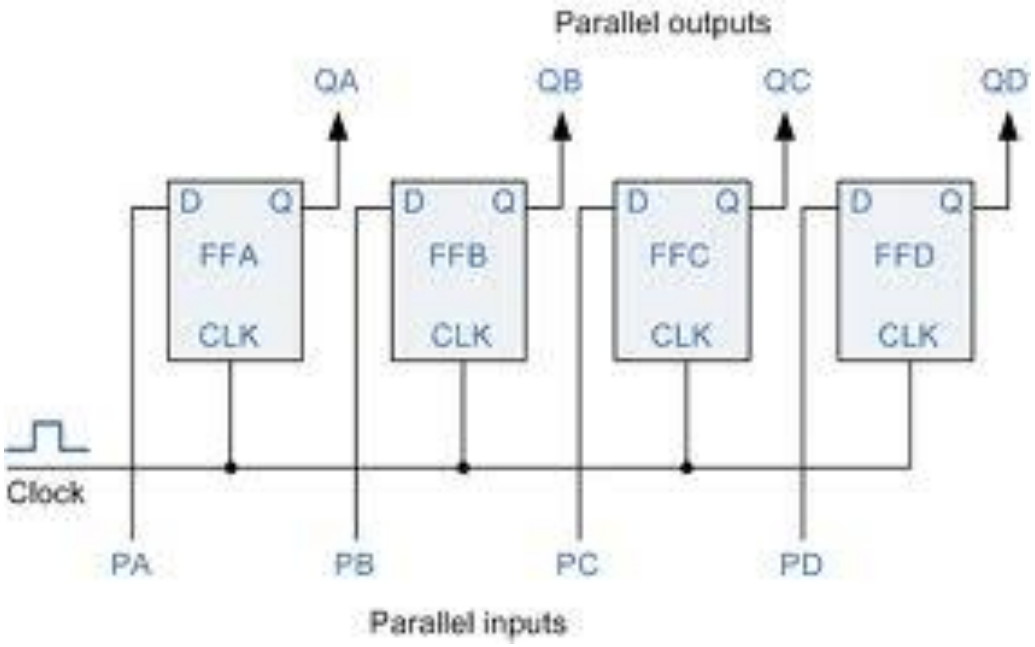
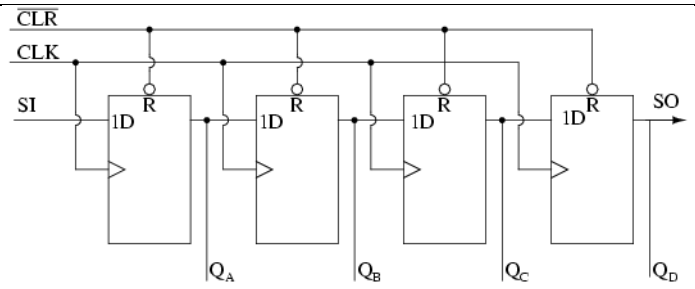
1. Registers

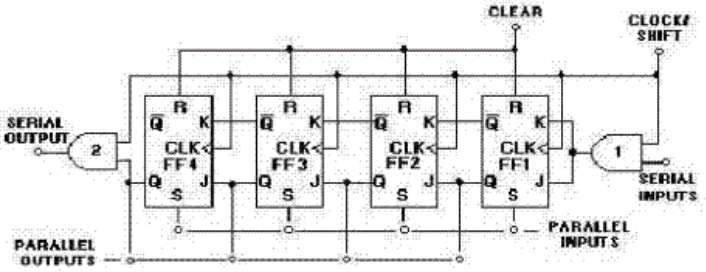
a. Parallel register



b. Shift register



Serial-in/ Parallel out shift register details



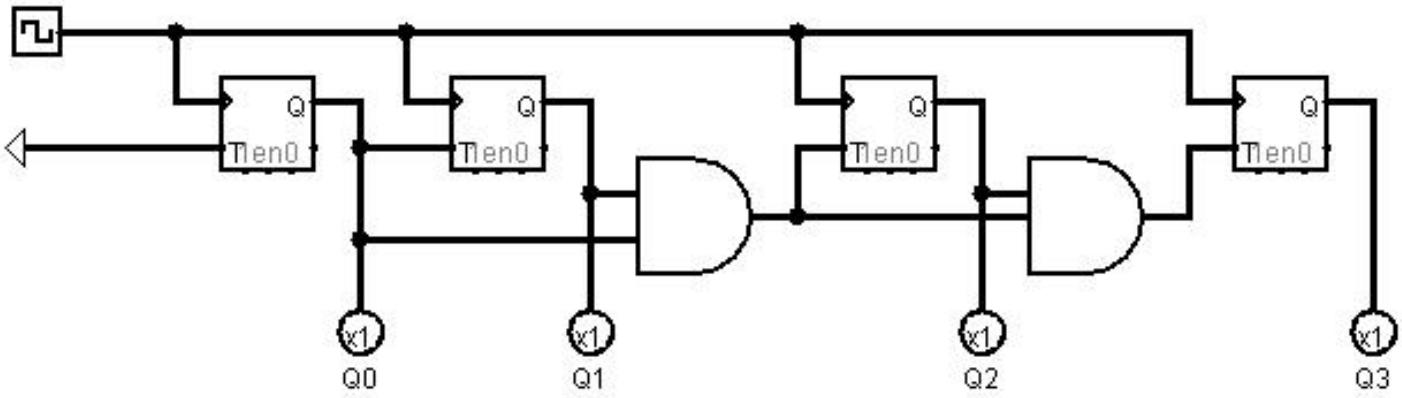
Shift register with variety of function modes

2. Counter

    a. Ripple (asynchronous) counters

    b. Synchronous counter

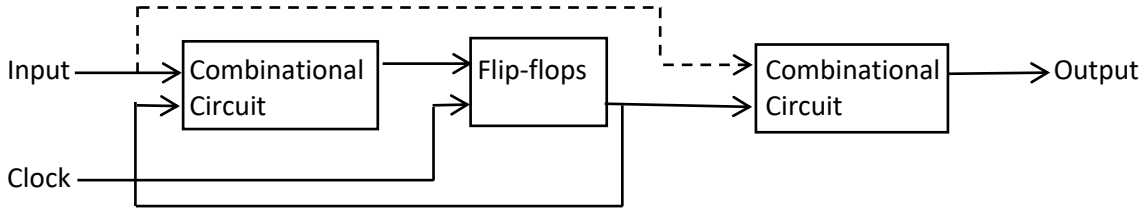
        i. Below: synchronous implementation using T flip flops



2. Finite state machines (FSMs)

    a. Definition

3. FSM general format



   a. Moore model FSMs

   b. Mealy model FSMs

4. FSM basic design steps

5. Our word problem

6. State transition diagram to minimize the number of states
    a. Convert word description

    b. For this problem

    c. Mealy model differences