A PROJECT REPORT ON

THE ANALYSIS OF A 4 BIT ALU

SUBMITTED BY

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8

AGENDA

- Introduction
- Project Details
- Explanation
- Conclusion

ABSTRA

The aim of this projects is to design a 4-b arithmetic logic unit to perform four arithmetic operations and four logic operations. Here, we will need

- Logic unit
- Arithmetic unit
- Multiplexer
- Full adder

INTRODUCTION

- The Arithmetic logic unit of several combinations circuits .Learning ALU design aids in designing complex circuits
- All arithmetic operations are performed by the carry look adder using a B-input logic.
- The logic operations are performed using basic logic gates.
- Two selected lines are used to perform operations on two 4-bits in both the A.U and L.U
- The third selected line is used to select either one of the units (A.U or the L.U).

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PROJECT DETAILS

- The A.L.U is made up of 3 parts which we will see in detail below
- The arithmetic unit, logical unit and a 2-1 Mux.

THE ARITHMETIC UNIT

- The A.U is divided into 3 parts that is,
- The arithmetic units, logical unit and a 2-mux.

The Arithmetic unit

- The A.U is divided into 3 parts :
- B1 Generator which selects which input of B will be taken I.e either B o B'.
- The carry in input which is generated at the beginning of the operation.
- The full adder which adds 3-bit input and gives the output in 2-bits is sum 1.
  DIAGRAM OF AN A.U

THE LOGICAL UNIT

This is a circuit divided into 2:

- The circuit which has built in logic gates such as the AND, OR,NOT and XOR gates.

- And a 2-1 mux to select the output to display

  DIAGRAM OF L.U
- Finally there a 2-1 mux which selects which unit to display I.e either A.U or LU.

  DIAGRAM OF THE A.L.U

EXPLANATION

- The inputs are taken
- Firstly the two selectors lines S1 and S2 decided which operation to take.
- Both the A.U and L.U perform their respective operations simultaneously with respect to S1 and S2
- The carry-in input is generated and added to the two inputs.
- After the operations are performed the output are sent to a 2-1 mux and the last line S2 decide which of the outputs units it's to display.
- For the 2-bit input the right bit of the result I.e output display as sum and the left most bit is sent as the carry-In for the next A.L.U and the process continues.
- At the last A.L.U, the right- most of the results bit is displayed and the left most bit of the results if present, is declared.

  DIAGRAM OF THE 4-BIT ALU