Checkpoint 1:

Report:

We decided to make a Tomasulo processor with superscalar, branch prediction, advanced multiplication, and potentially speculative loads.

Cameron designed the parameterizable queue. A testbench to test filling then emptying the queue multiple times was used to verify that the design works.

Bobby and Zhihao created the design block diagram of the datapath, and instruction fetching using the queue.

Checkpoint 2(RoadMap):

Main Feature:

Bob & Zhihao: ROB, RS, CDB, ScoreBoard
Cameron: RegFile
Bob & Zhihao & Cameron: ALU(Arith)

Extra Feature(For further plan):

LSQ, StoreBuffer, etc.
Multiplier
BP
Cache