Checkpoint 3 Progress Report:

Bobby & Zhihao:

1. Added support for control instructions. Bobby wrote the backbone of the code while Zhihao modified and debugged the code with extensive tests.
2. Added support for memory instructions. Zhihao tried implementing a complicated load/store queue with store buffer and forwarding but found it too complicated for this checkpoint's deadline. Bobby and Zhihao then designed and implemented the load/store reservation stations that meet the minimum requirement (stall issuing load until the store is committed).
3. Tested all instructions with coremark using magic_dual_port memory.
4. As of 8 pm on 4/15, Zhihao is working on integrating mp_cache with banked memory.

Cameron:
Wrote some half-finished cache integration, lacking d-cache/i-cache arbiter and cache line adaptor for burst memory access. Zhihao decided to start integrating the cache himself.

Checkpoint 3 Roadmap:

Bobby & Zhihao: (design and implement together)

- Superscalar (estimated 15 points)
- Improve existing load/store by implementing store buffer with forwarding for competition's purpose
- Other advanced features if time permits

Cameron:

- Dadda multiplier (estimated 6 points)