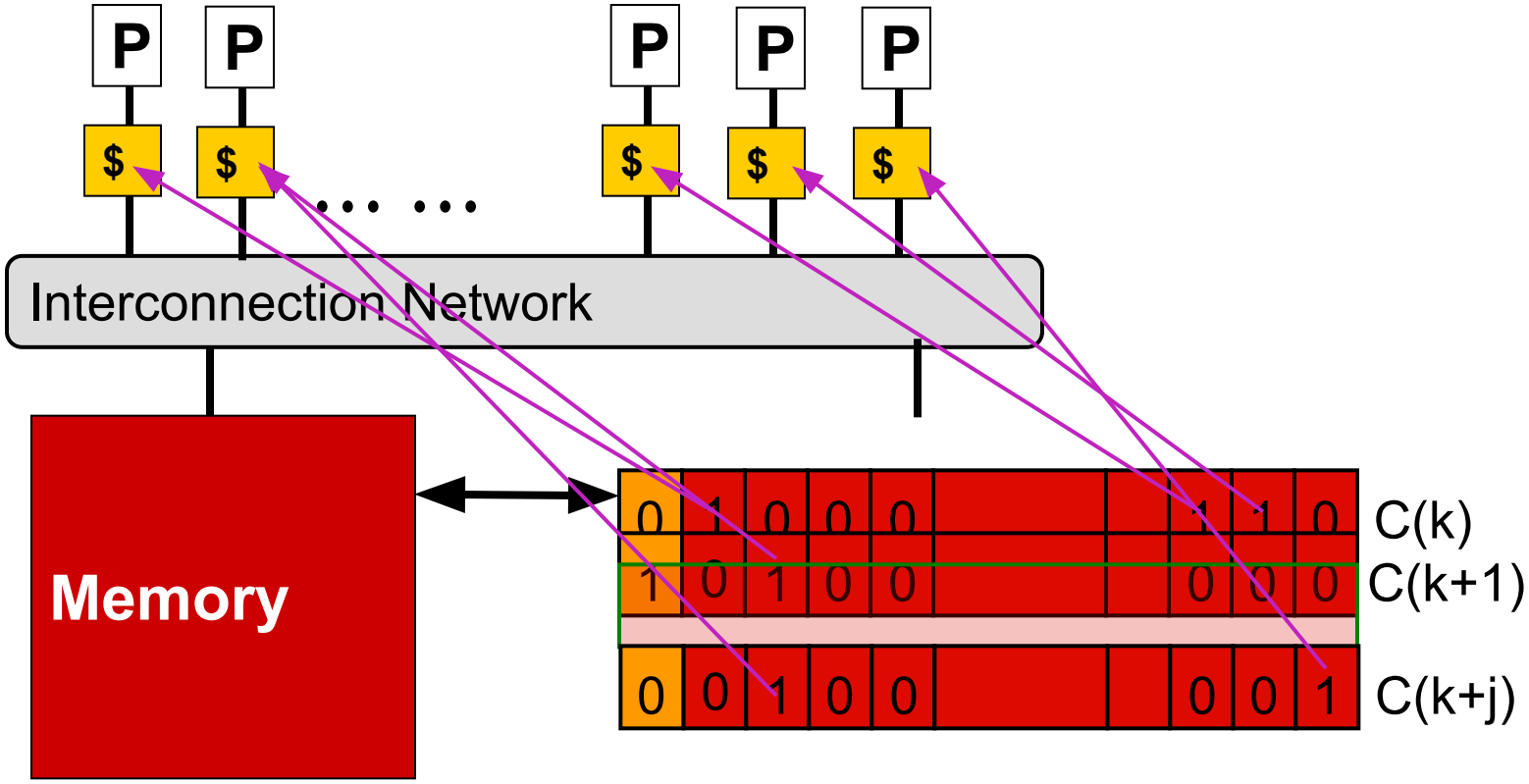
1

Directory-based Coherence Protocol

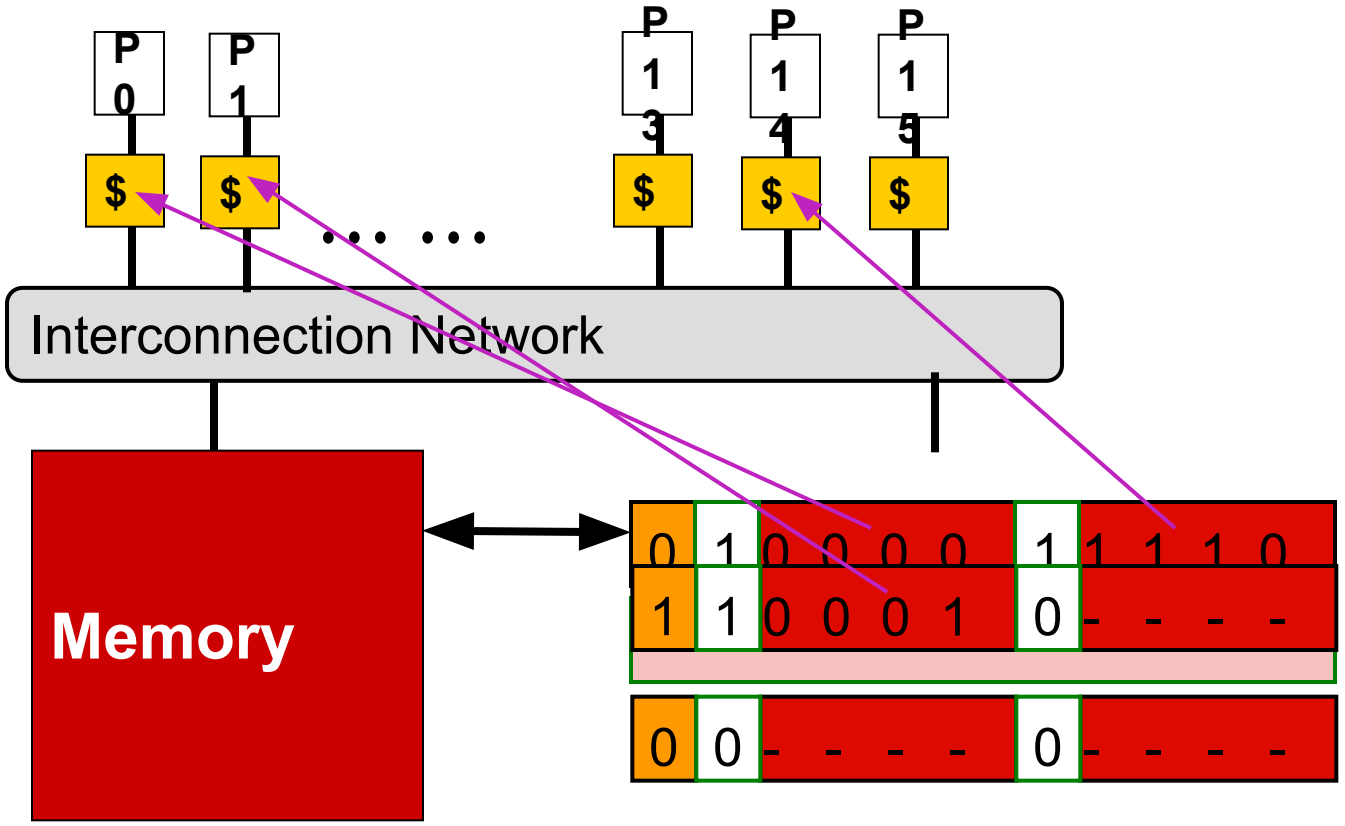


1 modified bit for each cache block in memory

1 presence bit for each processor, each cache block in memory

2

Directory-based Coherence Protocol (Limited Dir)



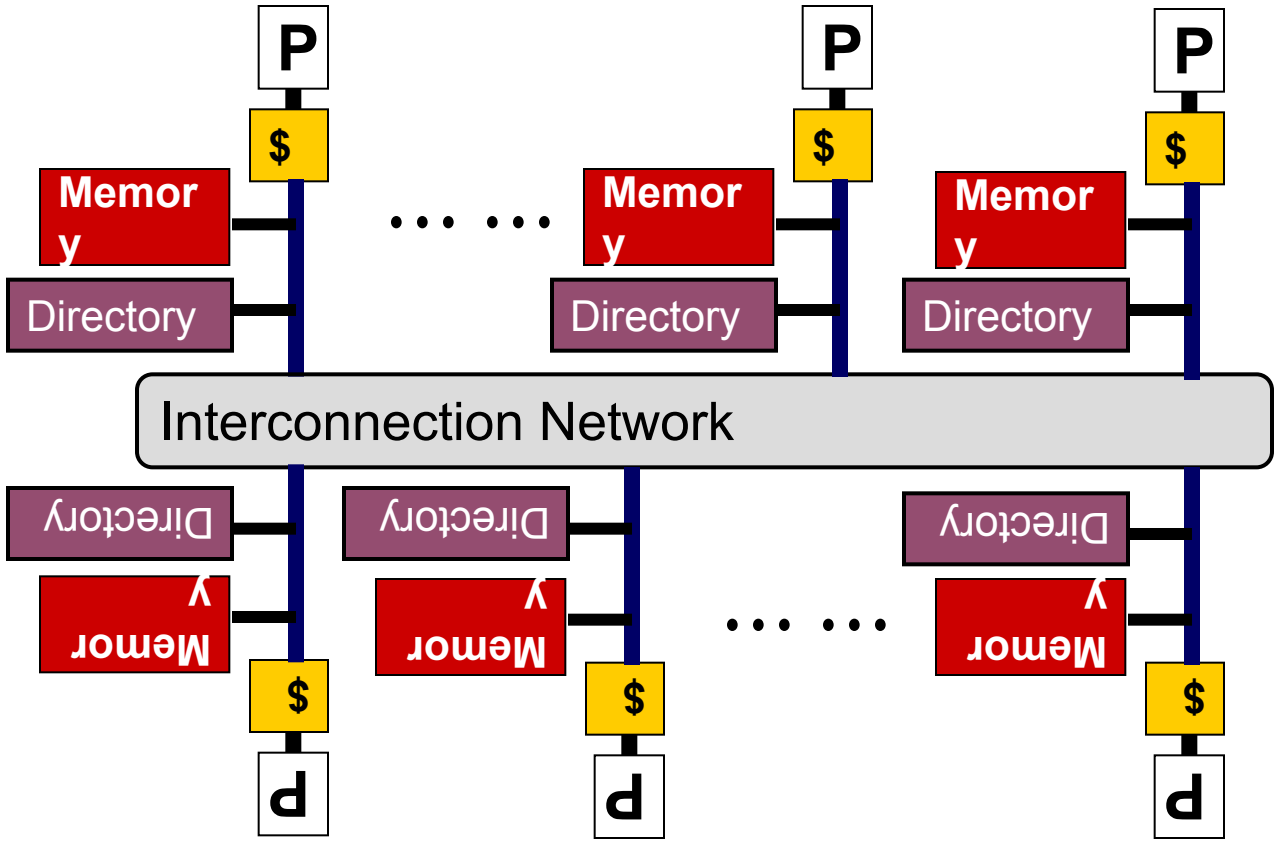
1 modified bit for each cache block in memory

Presence encoding is NULL or not

Encoded Present bits (lg_2N),
each cache line can reside in **2 processors in this example**

3

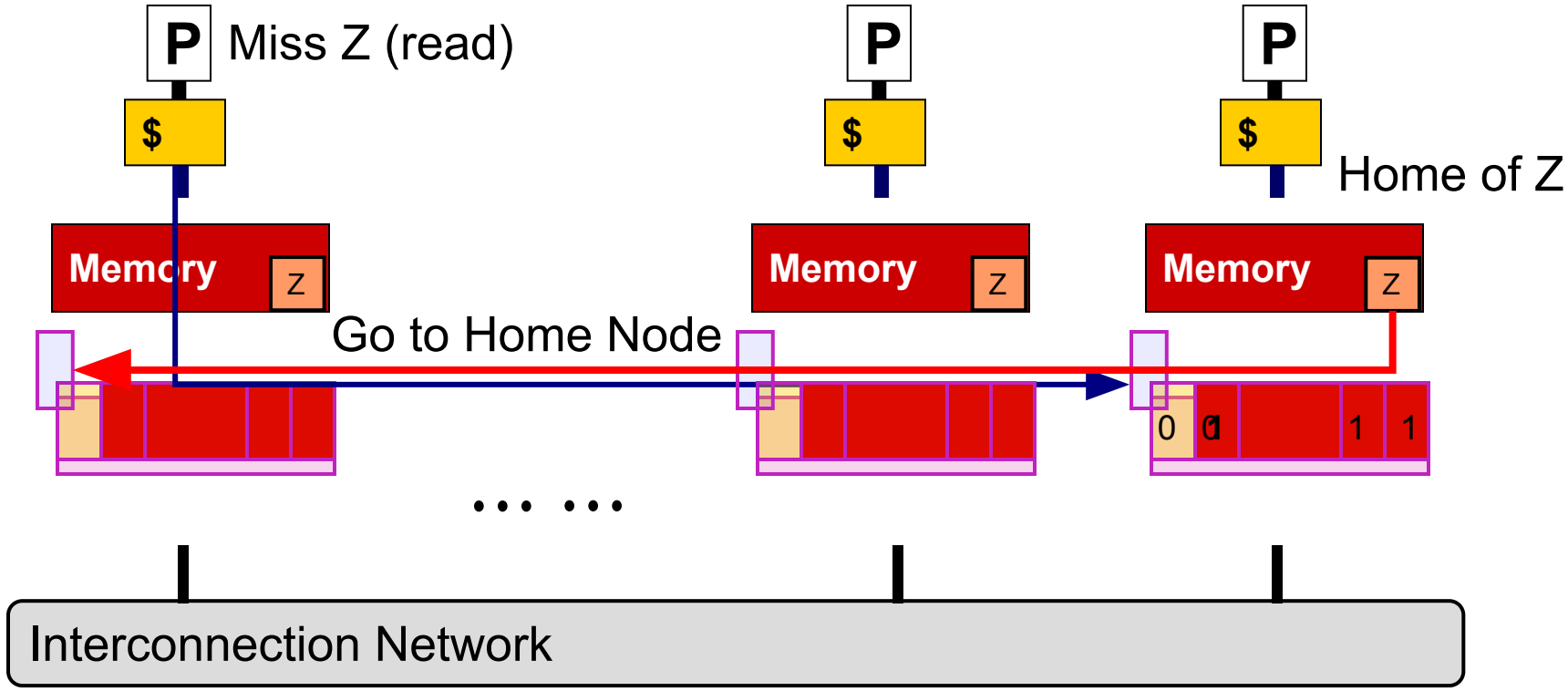
Distributed Directory Coherence Protocol



- Centralized directory is less scalable (contention)
- Distributed shared memory (DSM) for a large MP system
- Interconnection network is no longer a shared bus
- Maintain cache coherence (CC-NUMA)
- Each address has a “home”

4

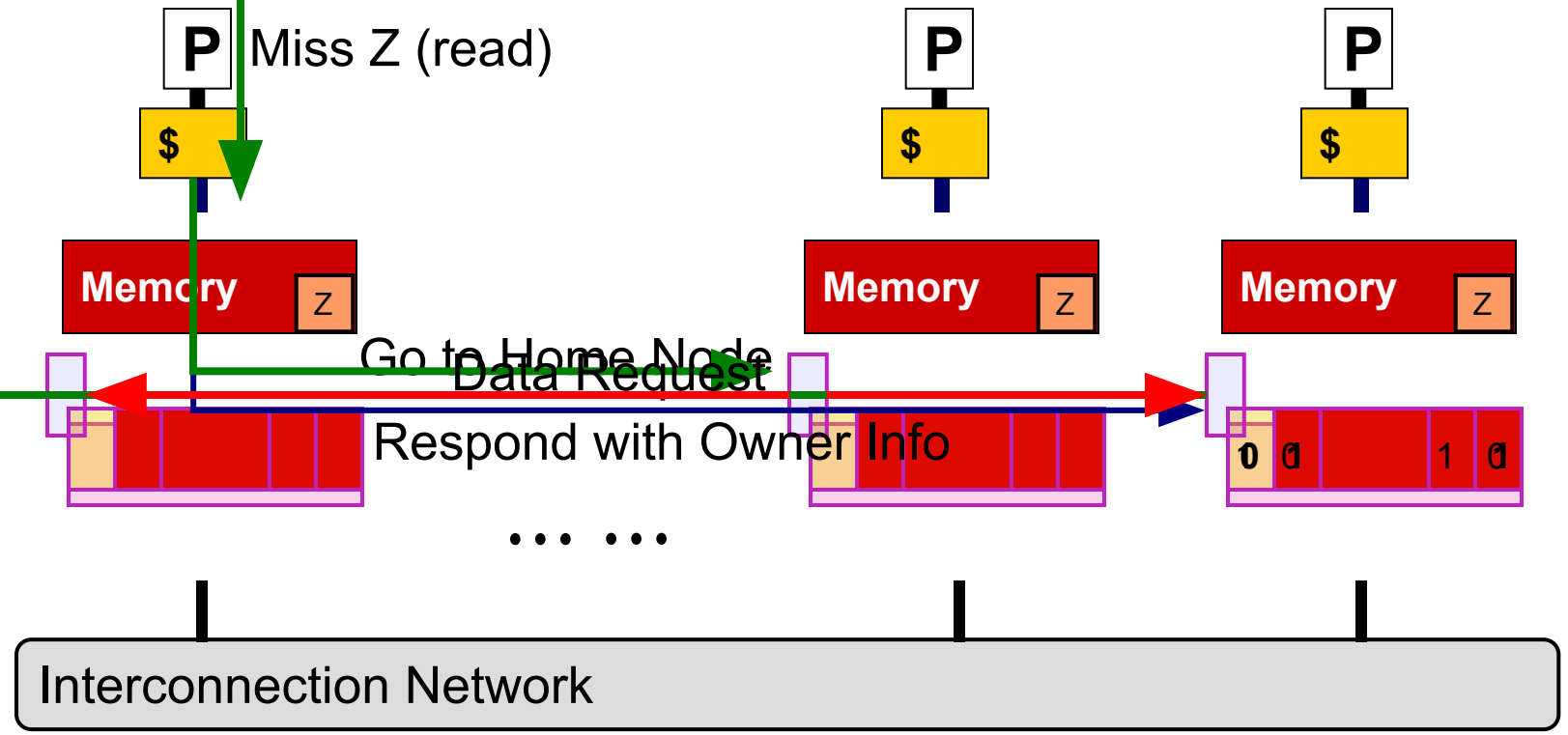
Directory Coherence Protocol: Read Miss



Data Z is shared
(clean)

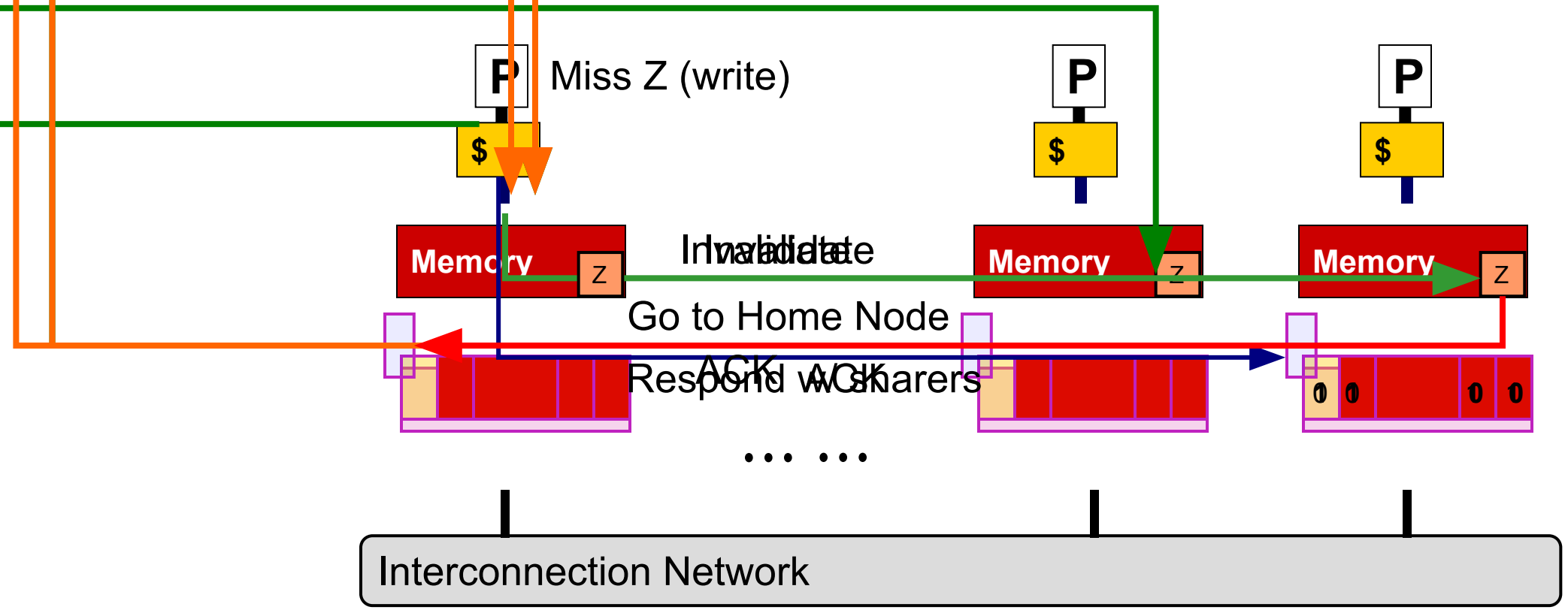
5

Directory Coherence Protocol: Read Miss



Data Z is Clean, Shared by 3 nodes

Directory Coherence Protocol: Write Miss



Write Z can proceed in P0