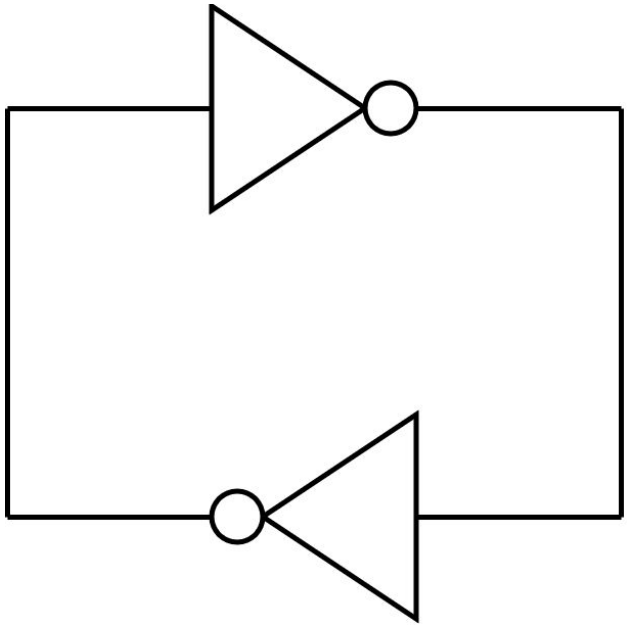
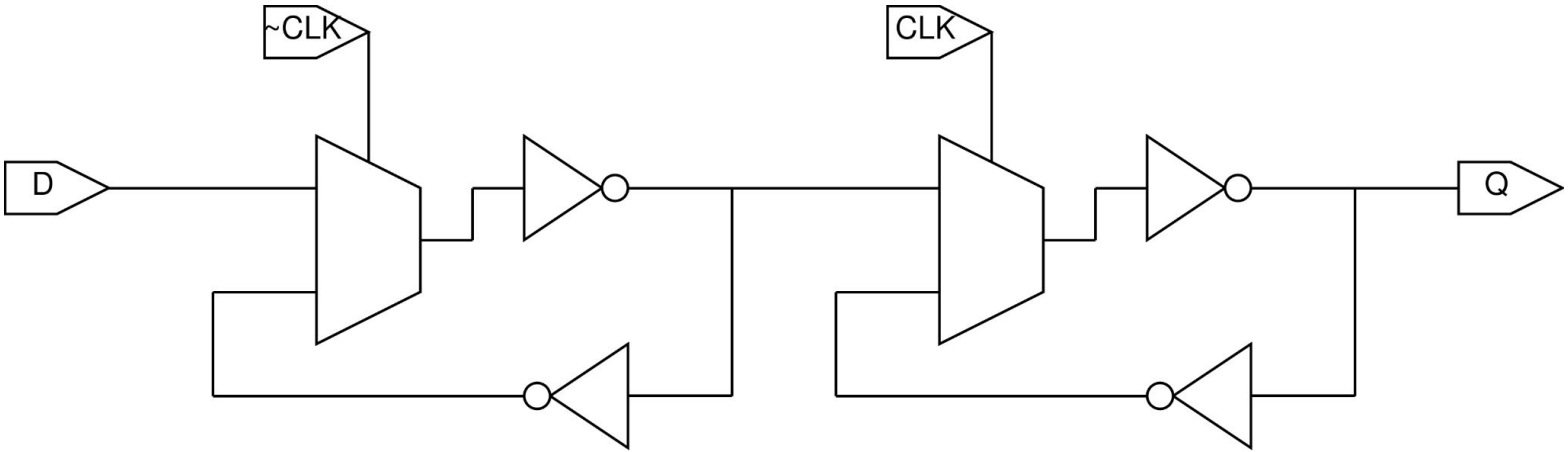
ECE411 Lecture 15
Memory Subsystem

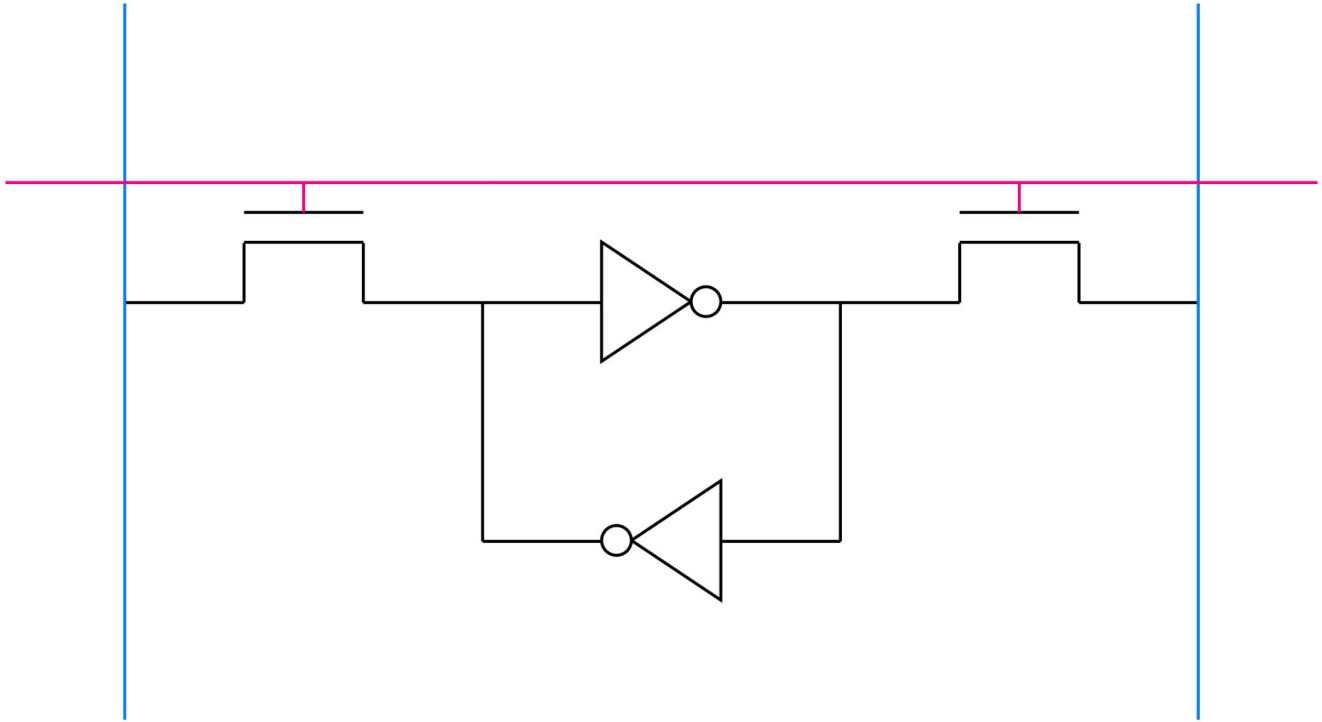
How to store a bit?



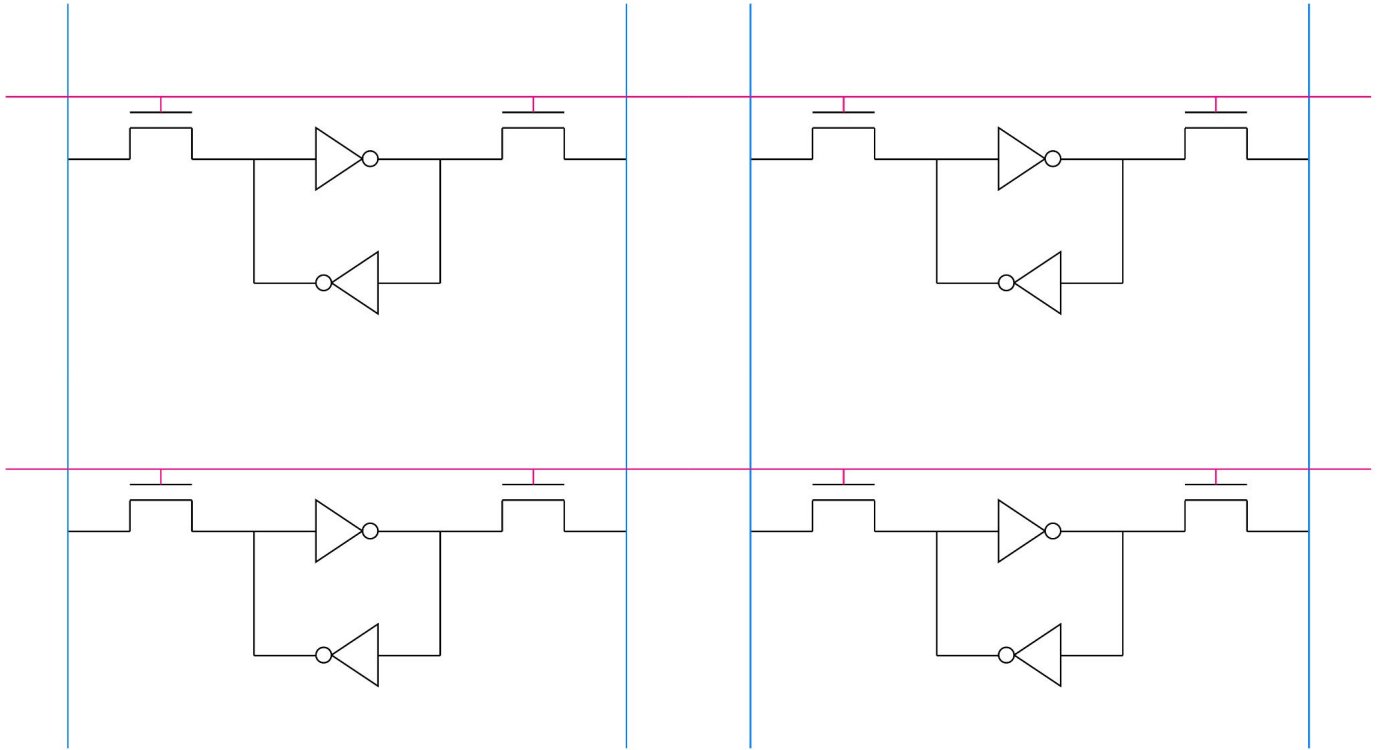
D-flip-flop



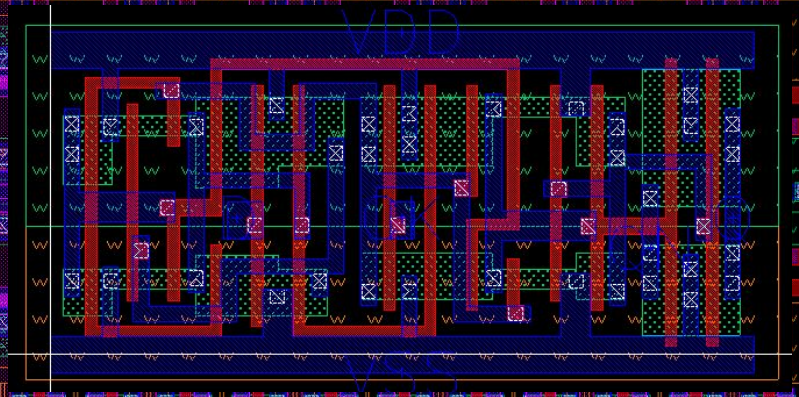
SRAM Bit



SRAM Array



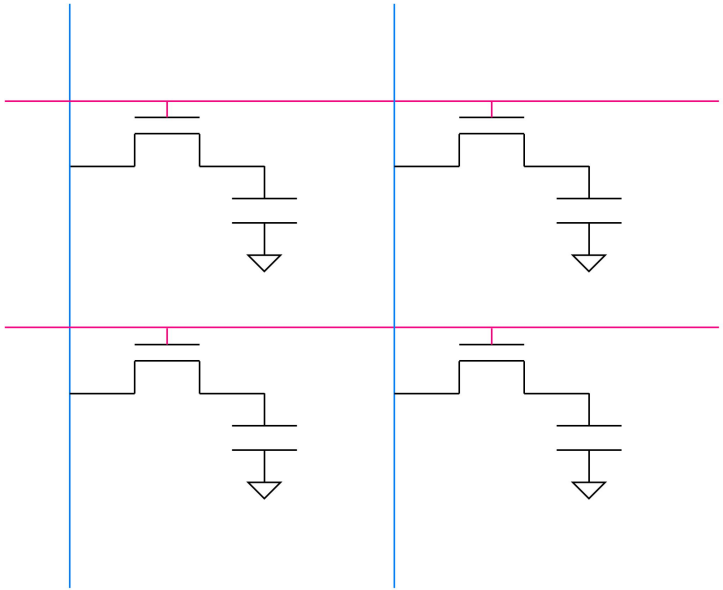
SRAM Array

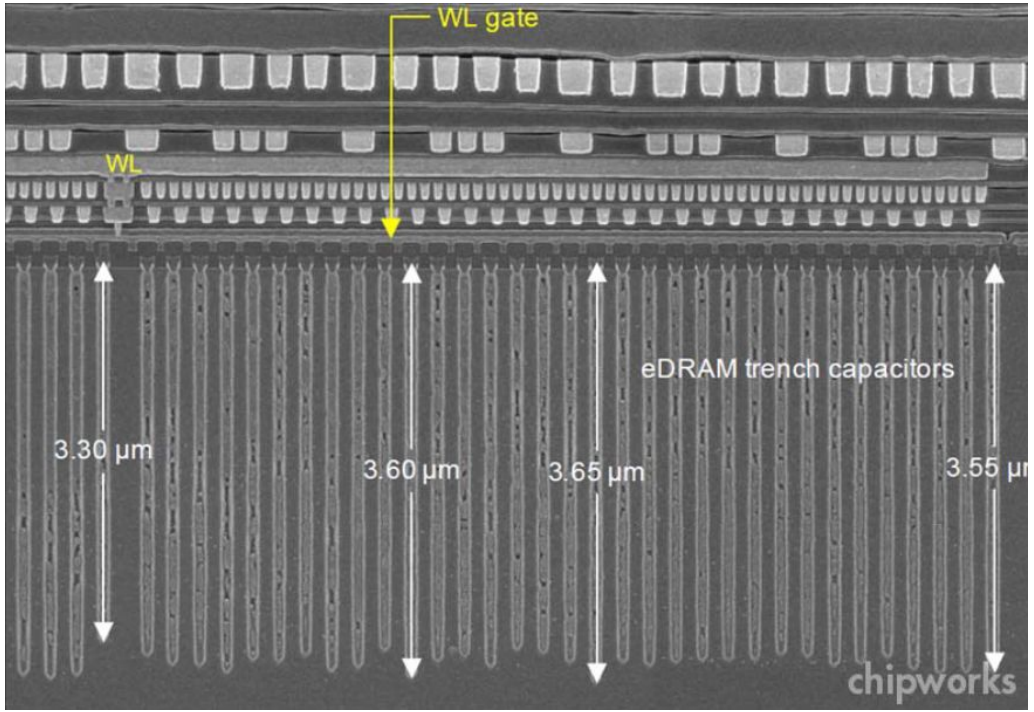


SRAM

- Fast (usually)
- CMOS compatible
  - Can be fabricated on the same die as logics
- Relatively area efficient
  - At least compared to D-flip-flop
- But can we be more area efficient?

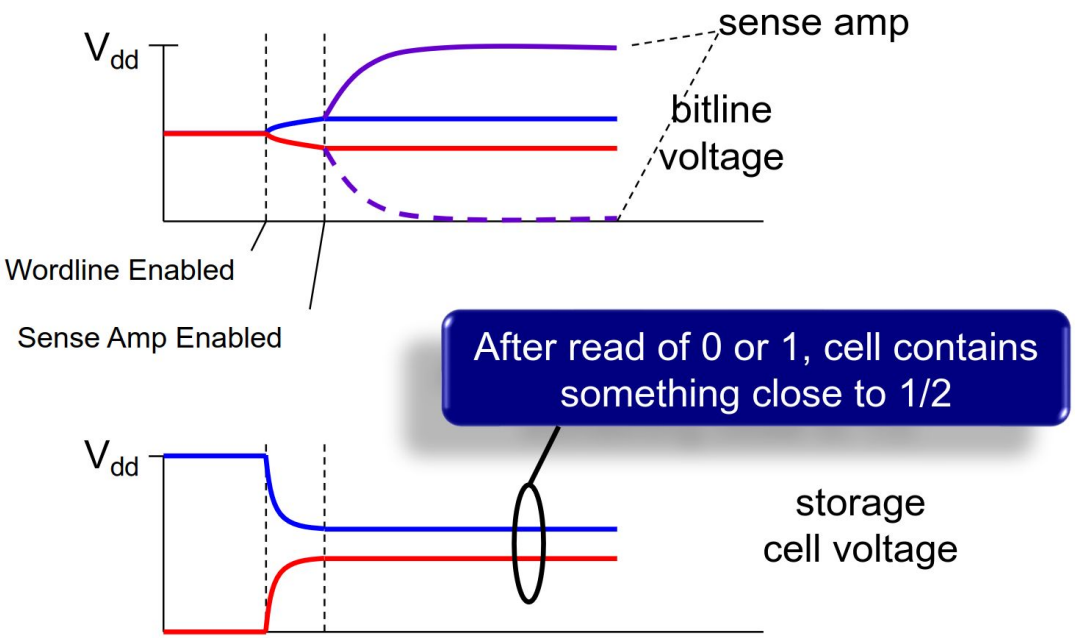
DRAM bit




WL gate
WL
eDRAM trench capacitors
3.30 µm
3.60 µm
3.65 µm
3.55 µr
chipworks

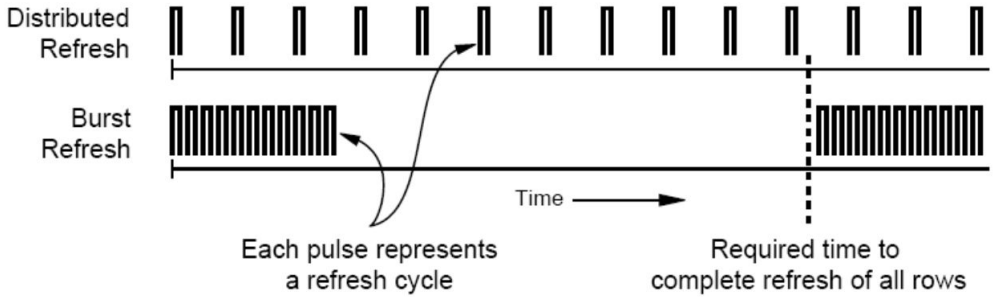
DRAM Read

- Need some amplifier on bitline
  - Cannot fully charge bitline to logic level
- Destructive read
  - Non restoring
  - Limited charge in capacitor
- Need to write back after each read
  - Also called precharge or closing the page



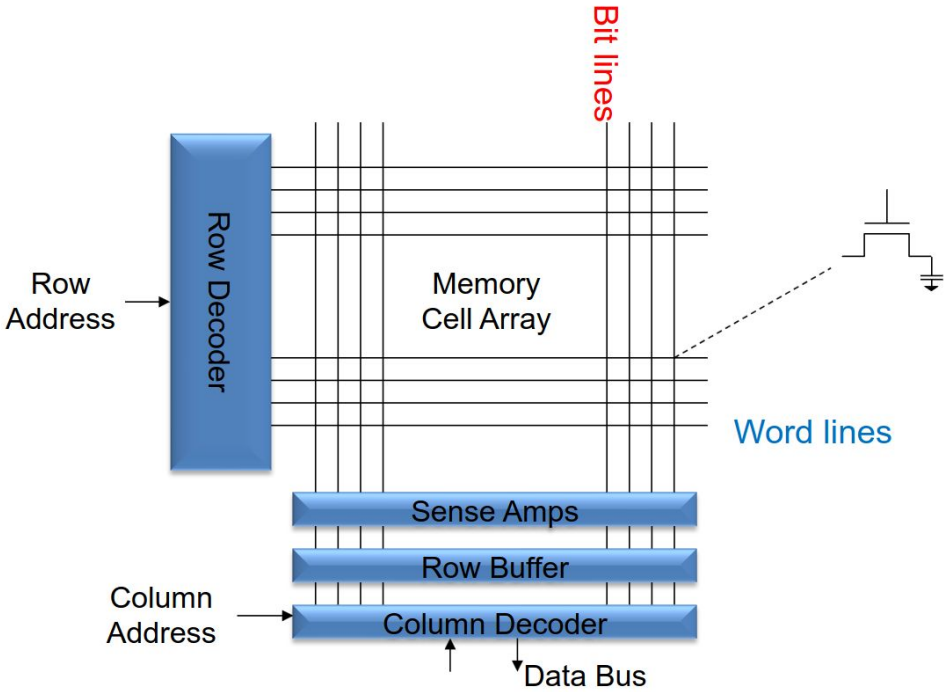
DRAM Refresh

- It is a capacitor
  - Non restoring, compare to SRAM’s inverter
- It is very small
  - Electron do be tunneling
- Need to periodically read and re-write the data back
  - Otherwise the data will be gone in a bit
  - Typically done every ~64ms for every single row
- Hence the name Dynamic RAM



DRAM Array

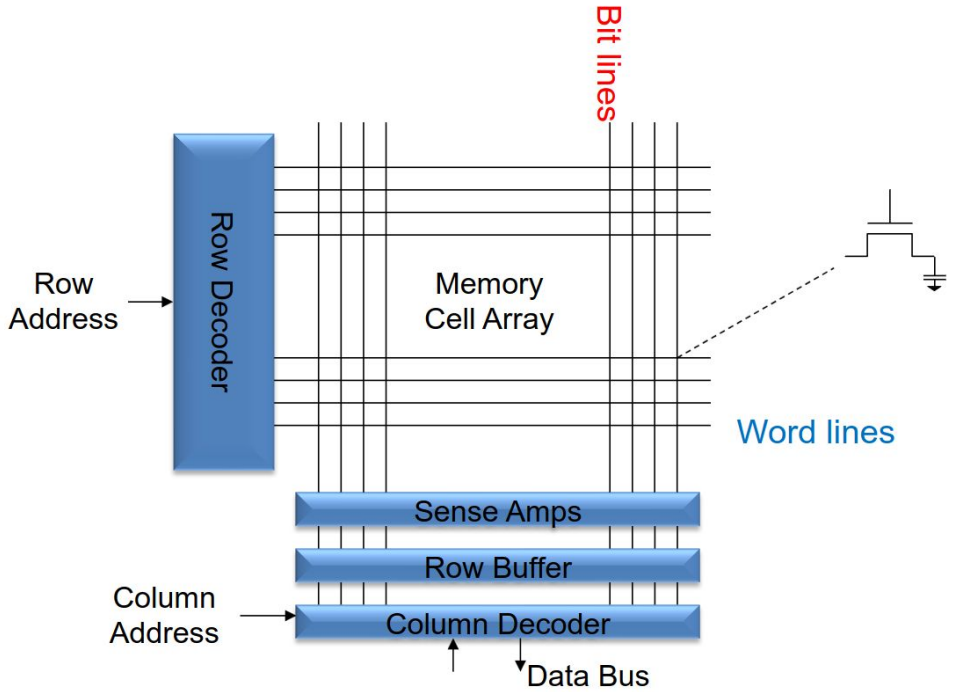
- Row
  - Word lines
  - Also sometimes called a page
  - Not to be confused with virtual memory page
- Row buffer
  - Because of destructive read
  - Implemented using DFF/SRAM
- Column
  - Bit lines
  - A row is very wide
  - Need to further select a subset
- Array is usually a square



DRAM

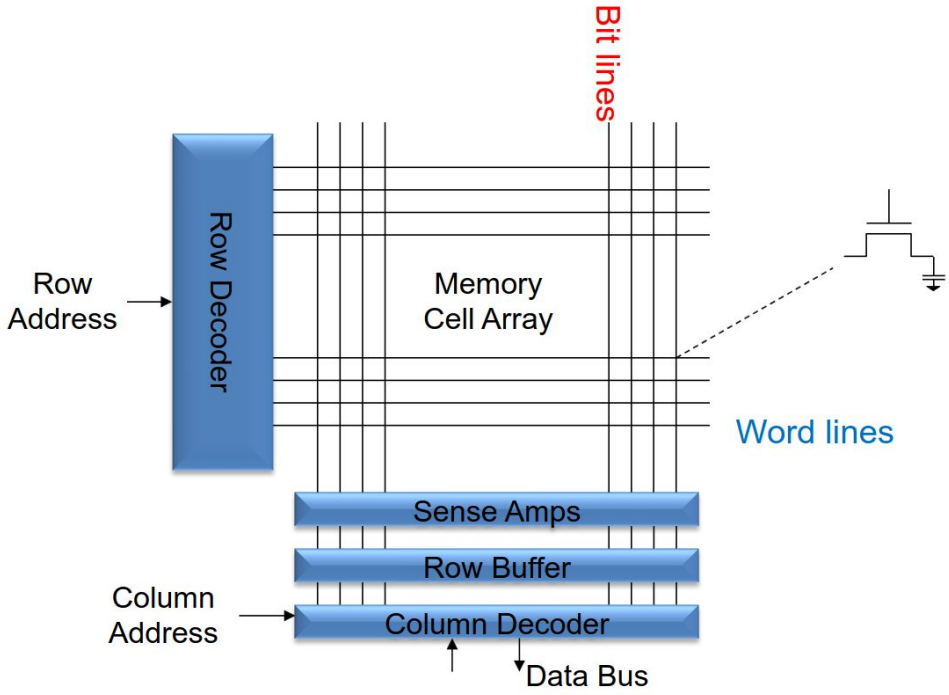
- Slower than SRAM
- Destructive read
- Needs constant refresh
- Needs to use special fabrication technology
  - Cannot be on the same chip as normal logic
- But is more area efficient

Timing


Bit lines
Row Decoder
Row Address
Memory Cell Array
Word lines
Sense Amps
Row Buffer
Column Address
Column Decoder
Data Bus

DRAM Timing

- Row access
  - Also called “active”, “activate a row”
  - smh called tRCD not tRAS
- Column access
  - tCAS / CL
- Precharge
  - tRP
- And more!
  - Active to precharge delay (tRAS)
  - Active to active delay (tRC)
  - Write to precharge delay (tWR)
  - Etc. etc.



SRAM Timing

- Usually boils down to one single value
  - tA
  - Row access time + column access time
  - No other restrictions like DRAM

Gaming

- In the order of CL, tRCD, tRP, and tRAS
- These are written in cycles
  - Cycles of the data bus
- Actually constant real time
  - Not constant cycles
  - So overclocking your RAM doesn't actually reduce access latency..?

Table 1: Key Timing Parameters

Speed Grade	PC4-	Data Rate (MT/s) CL = 24	22	21	20\19	18\17	16\15	14\13	12\11	10\9	tRCD ns	tRP ns	tRC ns
-3G2	3200	3200, 2933	3200, 2933	2933	2666\2666	2400\2400	2133\2133	1866\1866	1600\1600	1333\–	13.75	13.75	45.75
-2G9	2933	–	2933	2933	2666\2666	2400\2400	2133\2133	1866\1866	1600\1600	1333\–	14.32 (13.75)[1]	14.32 (13.75)[1]	46.32 (45.75)[1]
-2G6	2666	–	–	–	2666\2666	2400\2400	2133\2133	1866\1866	1600\1600	1333\–	14.25 (13.75)[1]	14.25 (13.75)[1]	46.25 (45.75)[1]

Details

Capacity	32GB (2 x 16GB)
Type	288-Pin PC RAM
Speed	DDR4 3600 (PC4 28800)
CAS Latency	18
Timing	18-22-22-42
Voltage	1.35V
ECC	No
Buffered/Registered	Unbuffered

DRAM Timing (Real)

CL is about 20 ns for this specific DRAM

Table 12: Electrical Characteristics and Recommended AC Operating Conditions

Notes 1–5 apply to all parameters and conditions

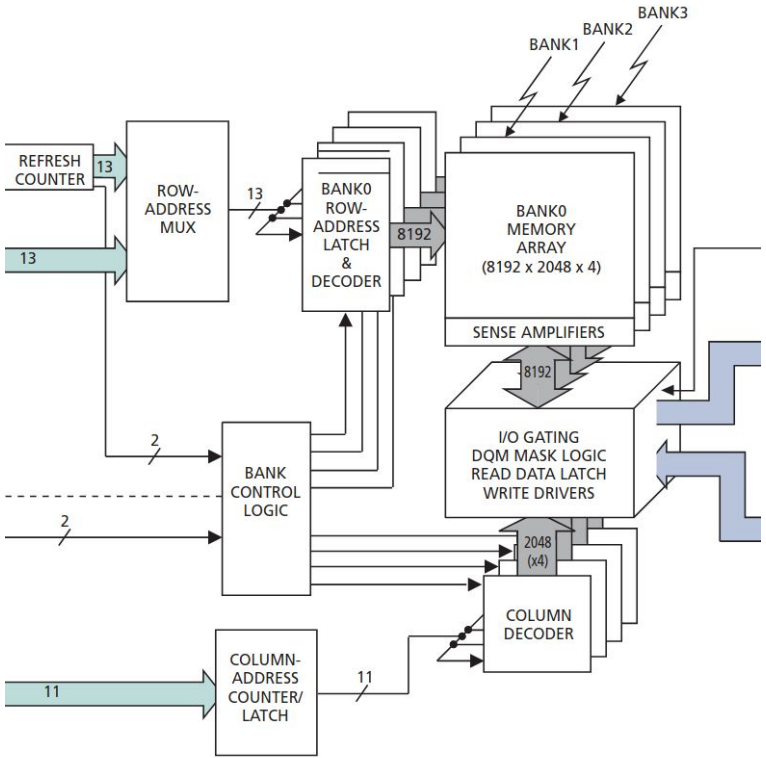
Parameter	Symbol	-6A		-7E		-75		Unit	Notes
		Min	Max	Min	Max	Min	Max		
ACTIVE-to-PRECHARGE command	^{t}RAS	42	120,000	37	120,000	44	120,000	ns	
ACTIVE-to-ACTIVE command period	^{t}RC	60	–	60	–	66	–	ns	11
ACTIVE-to-READ or WRITE delay	^{t}RCD	18	–	15	–	20	–	ns	
Refresh period (8192 rows)	^{t}REF	–	64	–	64	–	64	ms	
Refresh period – automotive (8192 rows)	^{t}REF$_{AT}$	–	16	–	16	–	16	ms	
AUTO REFRESH period	^{t}RFC	60	–	66	–	66	–	ns	
PRECHARGE command period	^{t}RP	18	–	15	–	20	–	ns	
ACTIVE bank *a* to ACTIVE bank *b* command	^{t}RRD	12	–	14	–	15	–	ns	
Transition time	^{t}T	0.3	1.2	0.3	1.2	0.3	1.2	ns	12
WRITE recovery time	^{t}WR	1 CLK + 6ns	–	1 CLK + 7ns	–	1 CLK + 7.5ns	–	ns	13
		12	–	14	–	15	–	ns	14

DRAM Timing (s l o w)

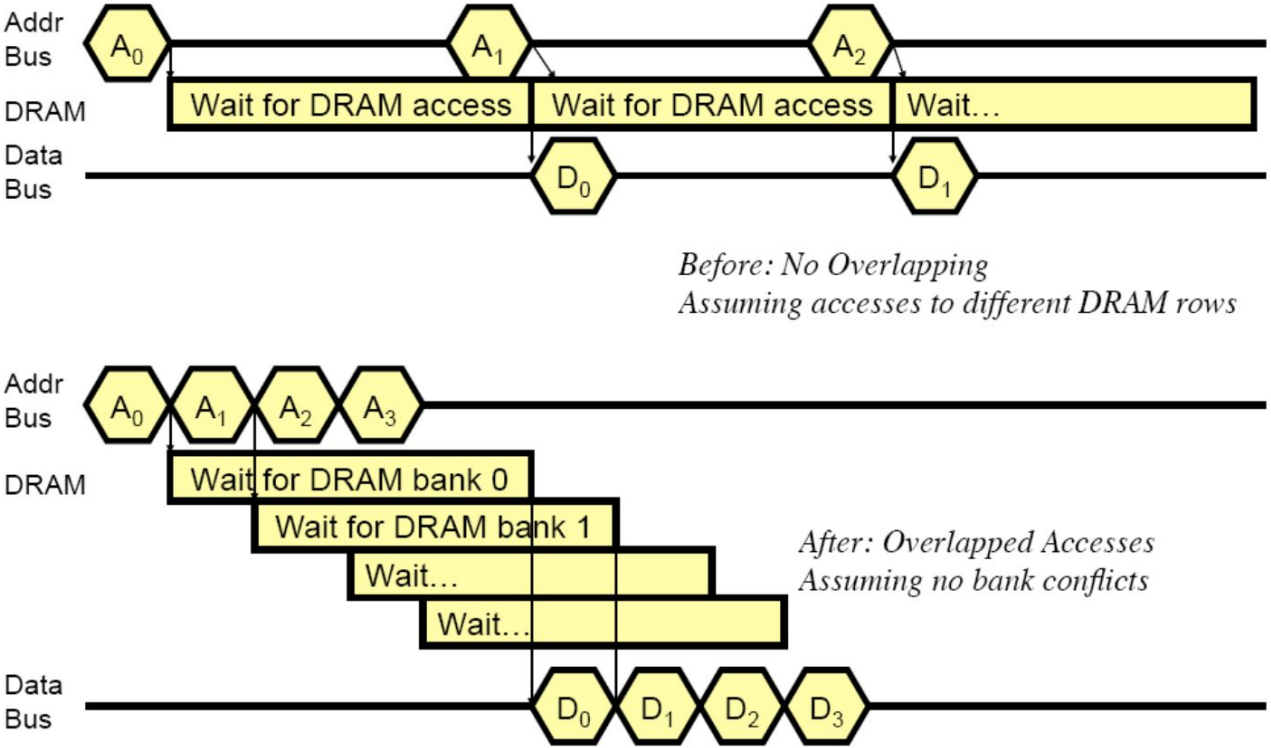
- Closing the current page and opening another page is slow
- Reading from the opened row is not that slow
- Only if we could have more row buffer…

DRAM Banking

- Not to be confused with whatever Wall Street is doing
- Array of arrays
  - More row buffers
  - yay!



DRAM Bank Interleaving



DRAM Bursting

- Pin is limited
  - DRAM chips usually have 4, 8, 16 bit wide versions
  - DRAM stick usually is 64 bit wide
    - Each chip supply 4/8/16 bit of the total 64 bit
- Row buffer is wide
  - Usually ~1kB
- Instead of sending one 64 bit, how about we send 4*64 bit over 4 cycles?
  - LLC will usually have cacheline size to be the same as this burst size (or vice versa)
  - Spatial locality

DRAM Row Buffer Policy

- When to close a page??

Open Page

- Keep the page open until another page is needed
- On page hit:
  - No need to pay precharge time and row access time
  - Only need to pay column access time
- On page miss:
  - Need to pay prechage time first, then row then column access time

Close Page

- Write back page after every access
- There will never be page hit
- On page miss (which is all the time):
  - Only need to pay row and column access time
  - Precharge time is already paid on the last access

Open Page vs Close page

- Open page:
  - Good for access pattern with spatial locality
  - For random access pattern each access will have additional latency
- Close page:
  - Good for random access pattern
  - Never page hit so minimum latency is still high

Queuing

- Imagine having OoO processor with out of order memory capability
  - Or multicore which share a single memory controller
- There could be a lot of outstanding memory request
  - Who should go first?

FCFS / FIFO

- First come first serve / first in first out
- Very fair
- But could it be better?
  - Can we exploit the row buffer speed?

FR-FCFS

- First ready first come first serve
- Those request that will be a hit in the row buffer will be prioritized
  - Very fast to serve access that are in the same row
  - Plain FCFS will need to precharge-row-column-access later which is unnecessary

Actual DRAM Read/Write Timing Diagram

Other DRAM stick stuff

- Ranks
- Channel
- DIMM
- UDIMM
- RDIMM
- LRDIMM
- ECC

Disk stuff

- HDD
- SSD
  - page/block
  - FTL
- RAID