

# Proyecto Final de Diseño Digital Avanzado

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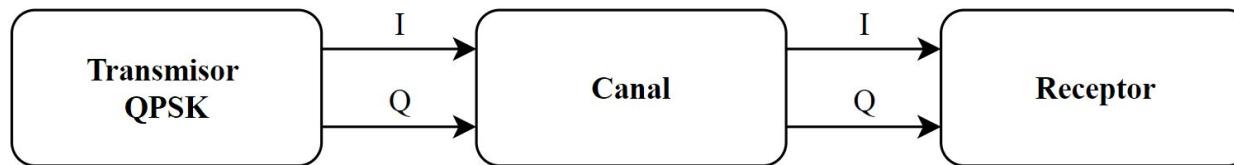
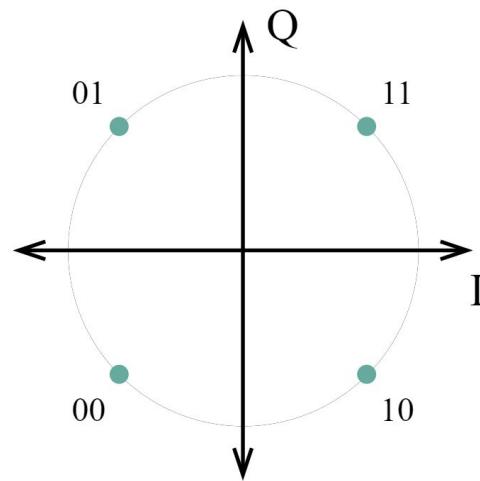
*Ecualizador Fraccionalmente  
Espaciado con Algoritmo LMS en  
el dominio del tiempo*

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<b>Alumno</b>	Ing. FERREYRA, Ramiro Tomás
<b>Profesor</b>	Dr. Ing. POLA, Ariel Luis
<b>Auxiliar</b>	Ing. CAYUELA, Pablo Oscar

# Introducción

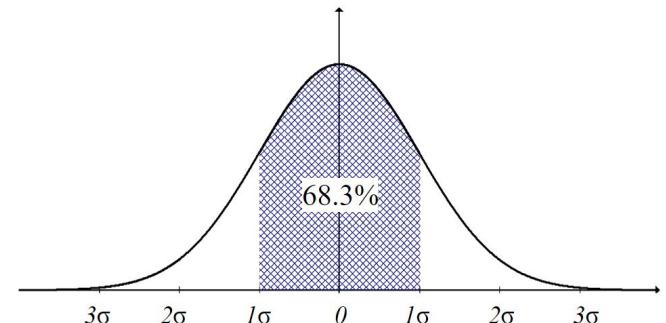
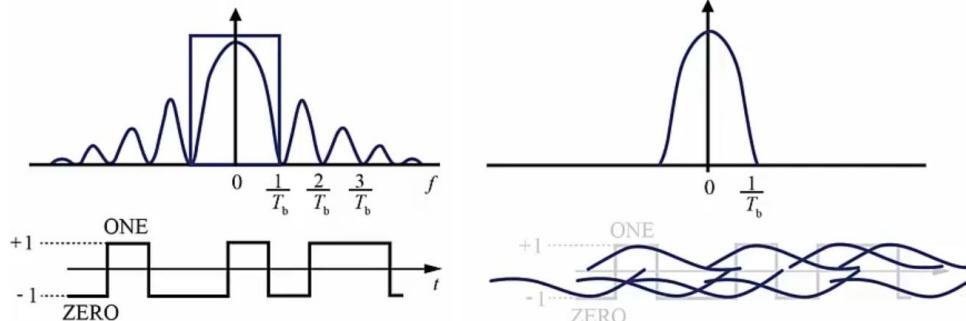
Sistema de comunicaciones



# Introducción

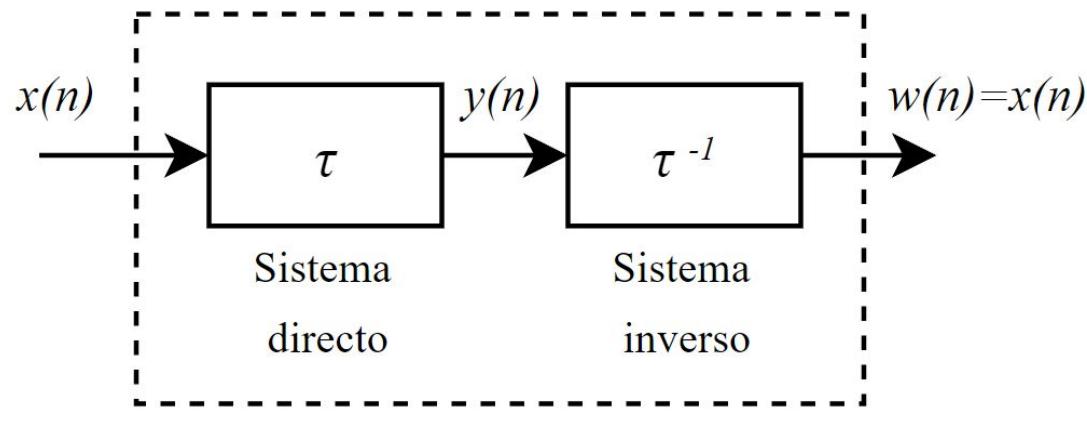
ISI y AWGN

$$r(nT) = a_n g(0) + \sum_{k=-\infty}^{\infty} a_k g((n - k)T) + n(nT)$$



# Introducción

## Ecualizadores



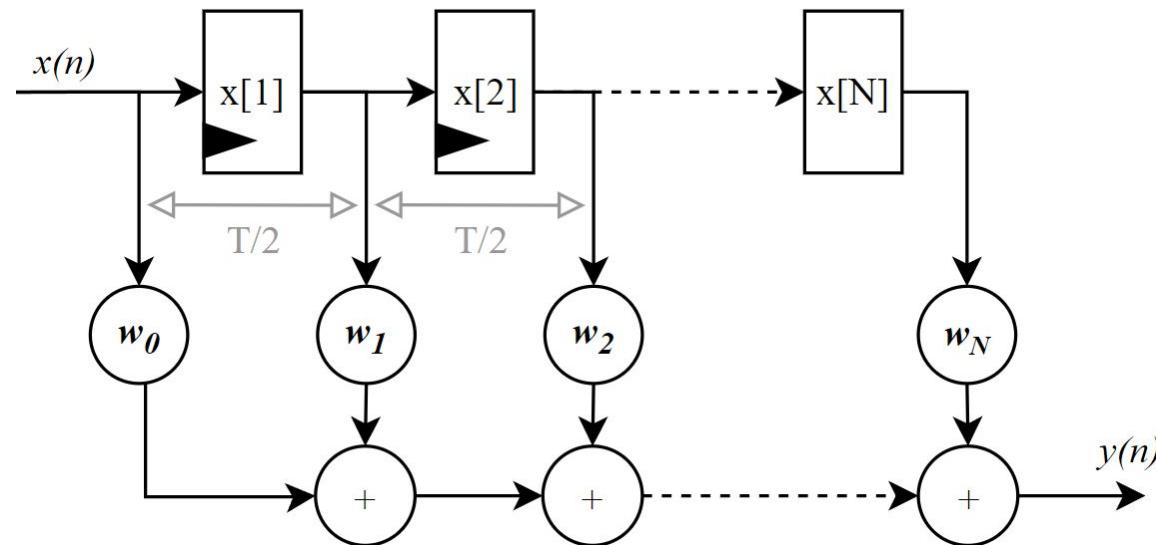
$$w(n) = h_1(n) * h(n) * x(n) = x(n)$$

$$h_1(n) * h(n) = \delta(n)$$

$$H(z)H_1(z) = 1$$

# Introducción

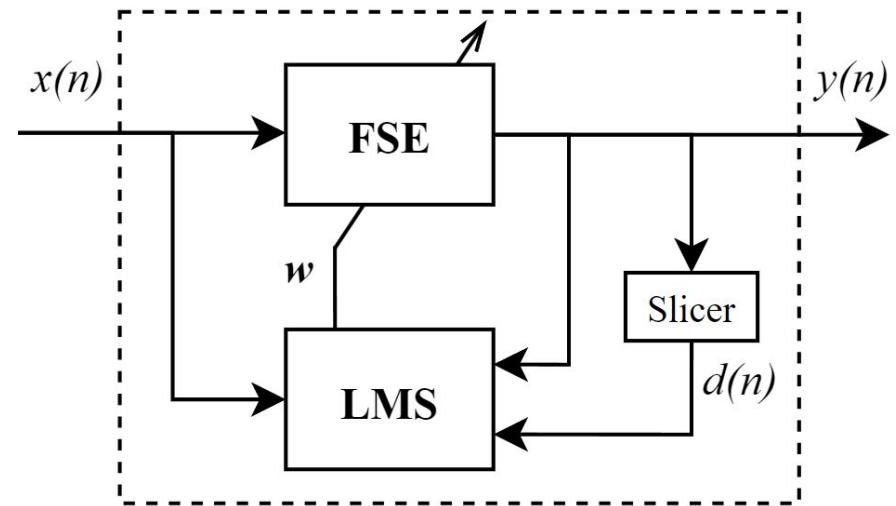
Ecualizador Fraccionalmente Espaciado



# Introducción

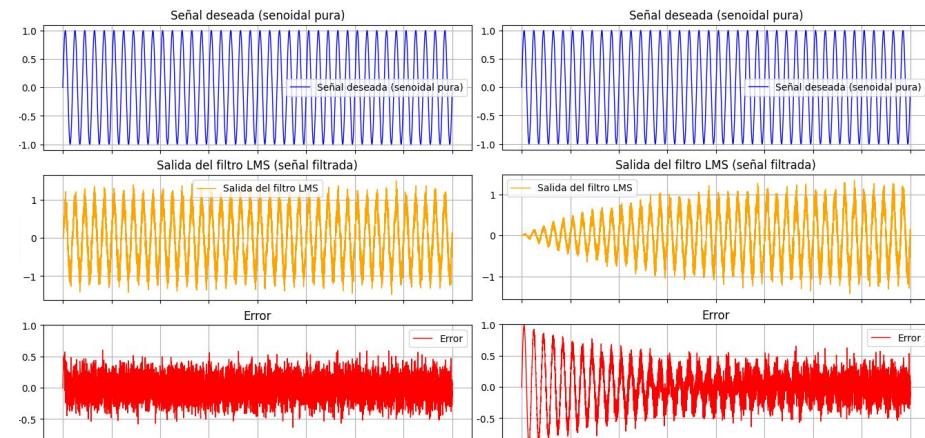
Algoritmo *Least Mean Square*

$$w_{n+1} = w_n + \mu \cdot e_n \cdot x_n$$

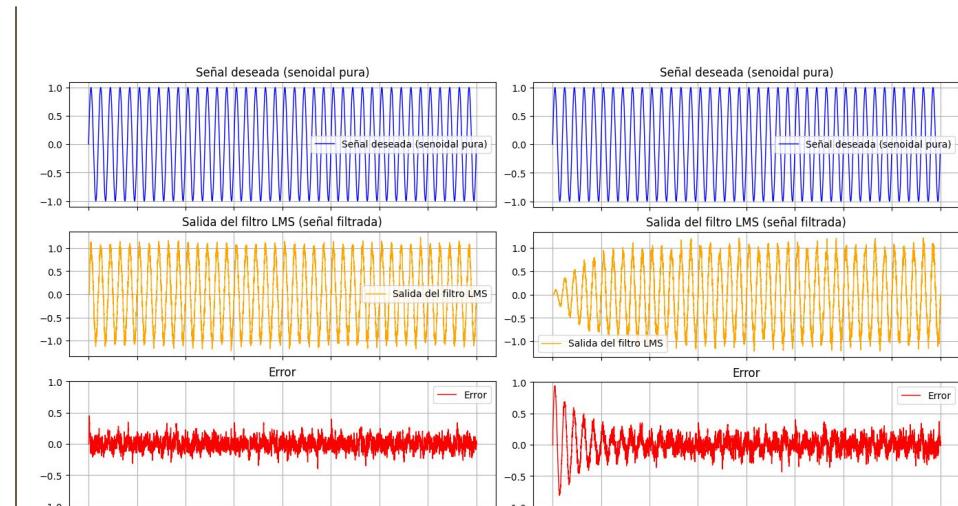


# Simulaciones en alto nivel

## Ecualizador convencional con LMS y señal senoidal



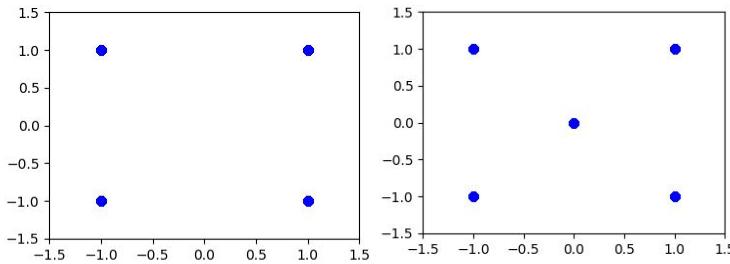
$n=9$ , con  $\mu=0.001$  (izq.) y  $\mu=0.00001$  (der.)



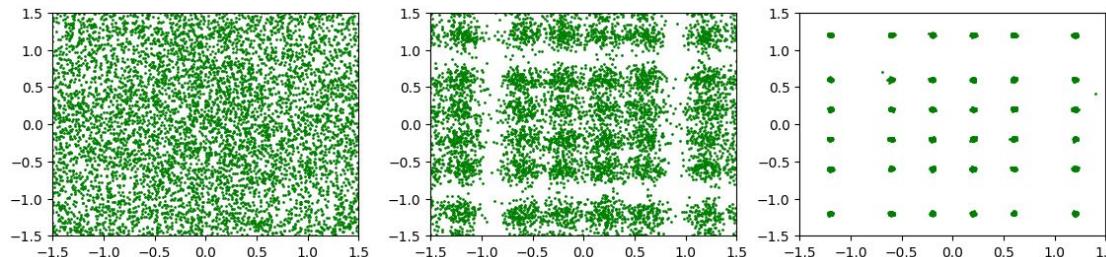
$n=32$ , con  $\mu=0.001$  (izq.) y  $\mu=0.00001$  (der.)

# Simulaciones en alto nivel

FSE con LMS con modulación QPSK sin *pulse shaping* ni decisión



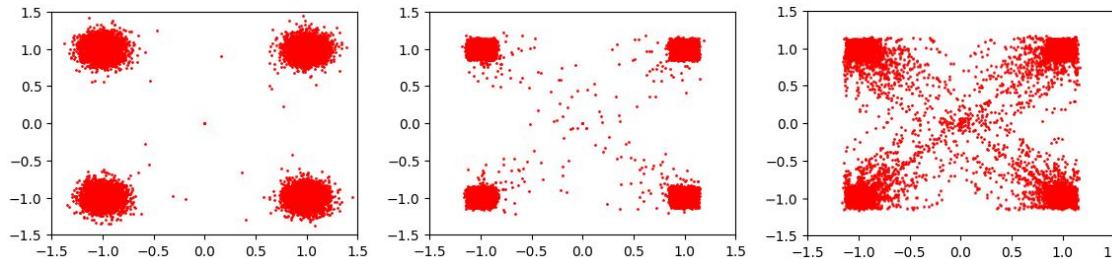
QPSK original sin oversampling (izquierda) y con oversampling (derecha)



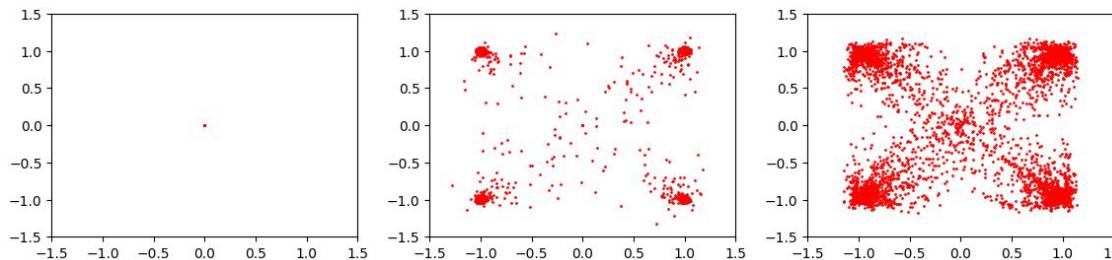
QPSK con ISI y distintas SNR: 10dB (izq.), 20dB(cen.) y 40dB(der.)

# Simulaciones en alto nivel

FSE con LMS con modulación QPSK sin *pulse shaping* ni decisión



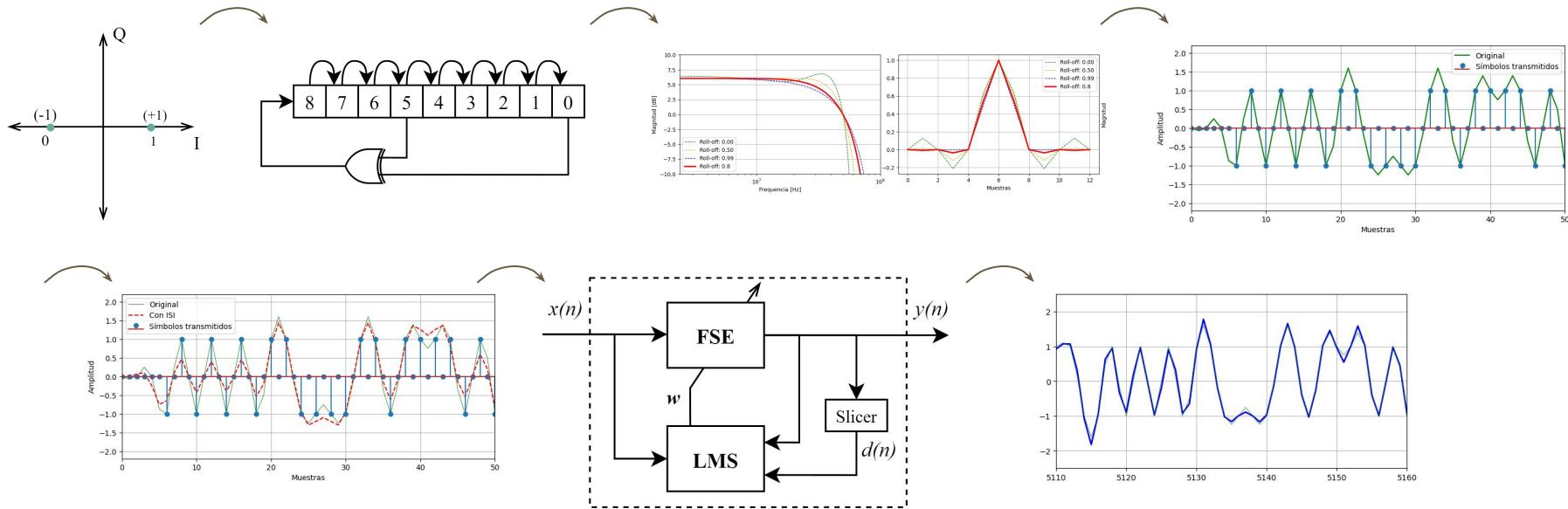
Salida del FSE para  $n=4$ , con  $\mu=0.1$  (izq.),  $\mu=0.01$  (cen.) y  $\mu=0.001$  (der.)



Salida del FSE para  $n=17$ , con  $\mu=0.1$  (izq.),  $\mu=0.01$  (cen.) y  $\mu=0.001$  (der.)

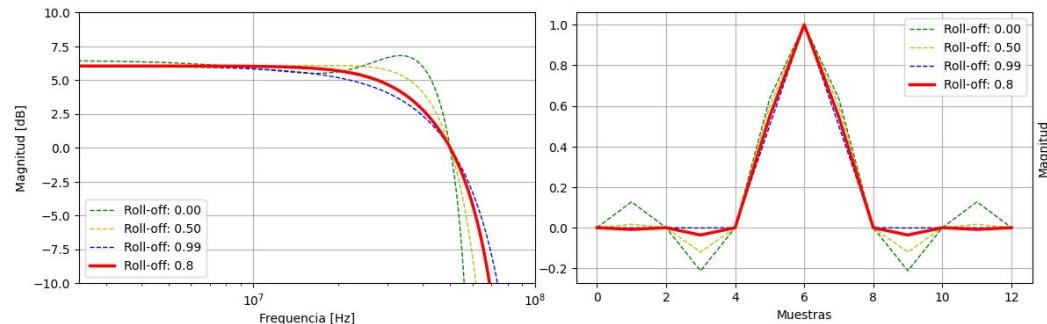
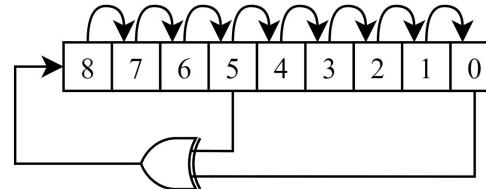
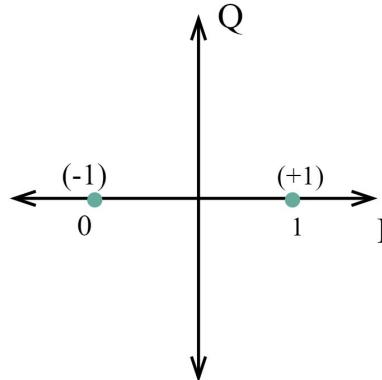
# Simulaciones en alto nivel

Simulación realista de FSE con algoritmo LMS en punto flotante



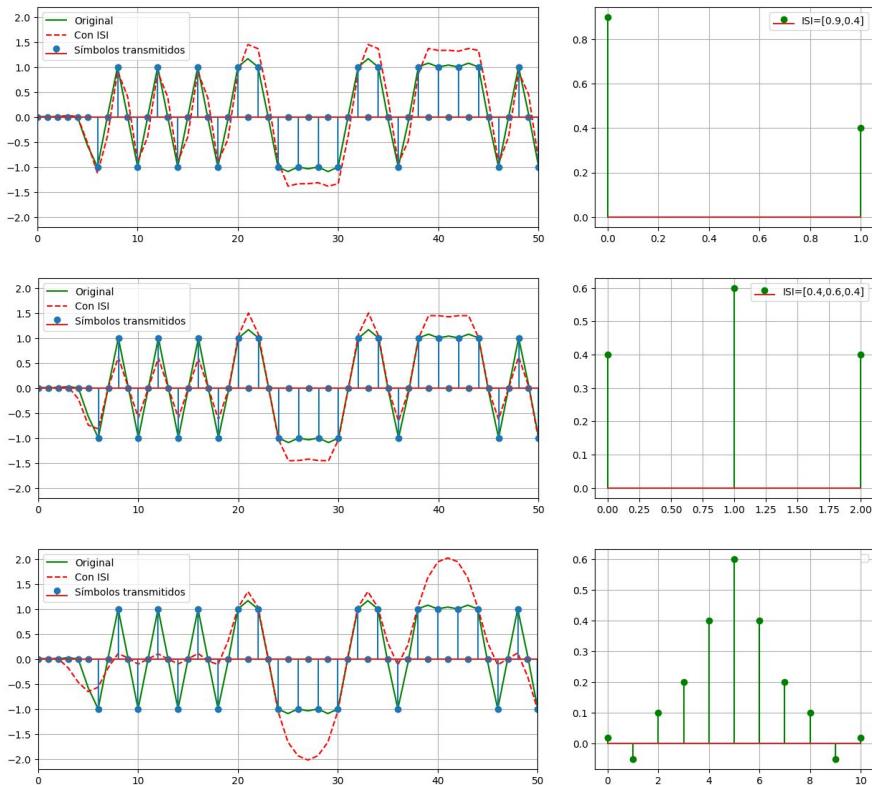
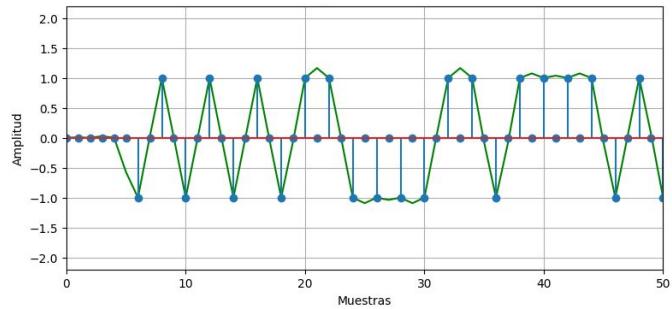
# FSE con LMS en punto flotante

Generación de la señal de entrada



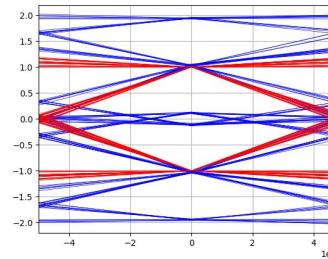
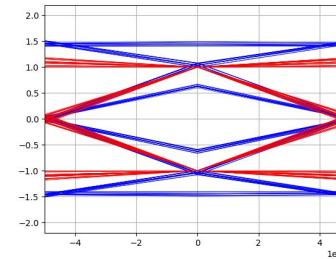
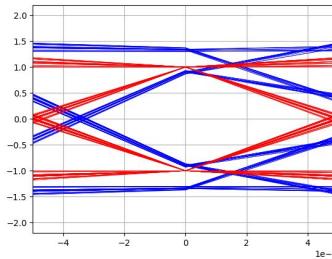
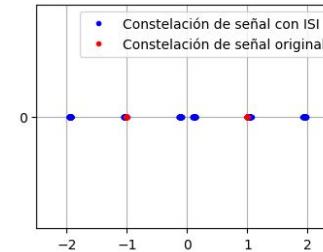
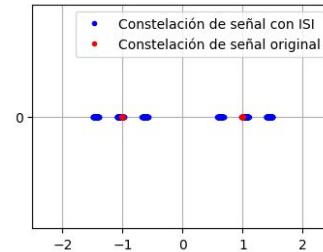
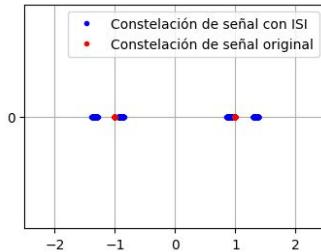
# FSE con LMS en punto flotante

Generación de la señal de entrada



# FSE con LMS en punto flotante

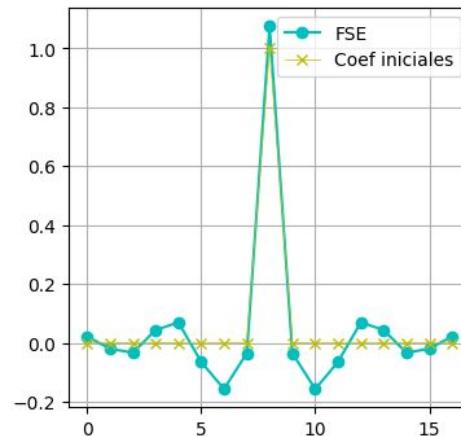
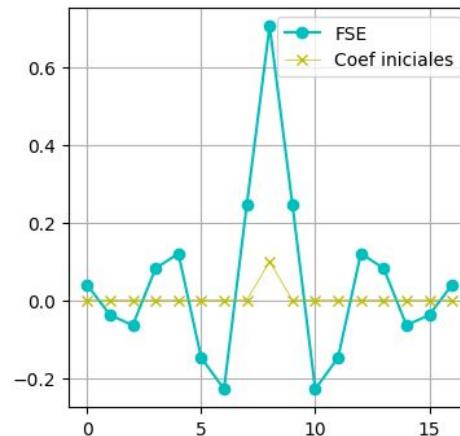
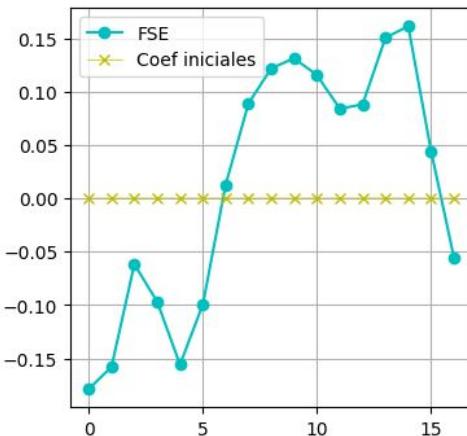
Generación de la señal de entrada



Constelación (arriba) y diagrama de ojo (abajo) de la señal con ISI leve (izq.), moderada (cen.) y severa (der.)

# FSE con LMS en punto flotante

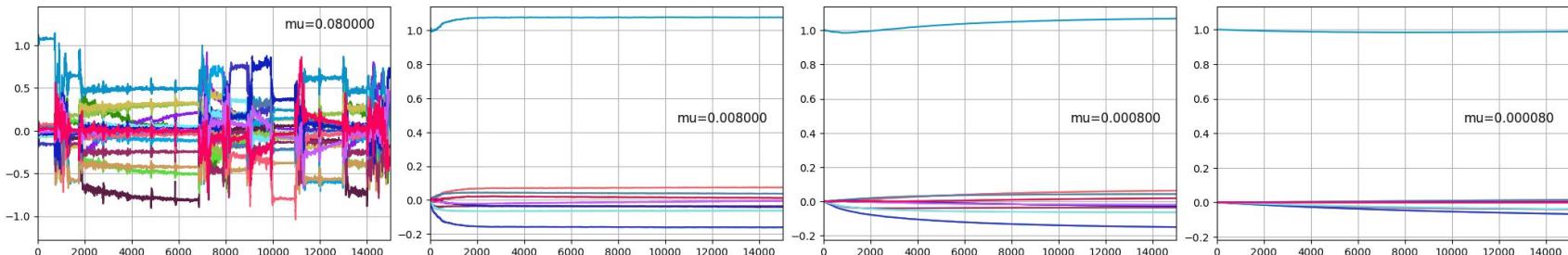
Ecualizador y adaptación de coeficientes: Coeficientes iniciales



*Taps iniciales en 0 (izq.), taps central inicial en 0.1 (cen.) y tap central inicial en 1 (der.)*

# FSE con LMS en punto flotante

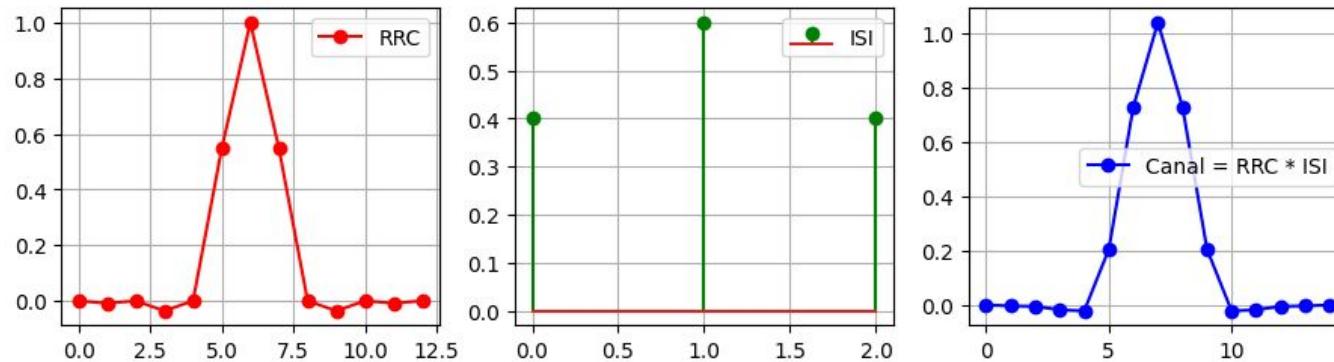
Ecualizador y adaptación de coeficientes: Constante de aprendizaje



*Evolución de los coeficientes para distintos pasos de adaptación ( $\mu$ )*

# FSE con LMS en punto flotante

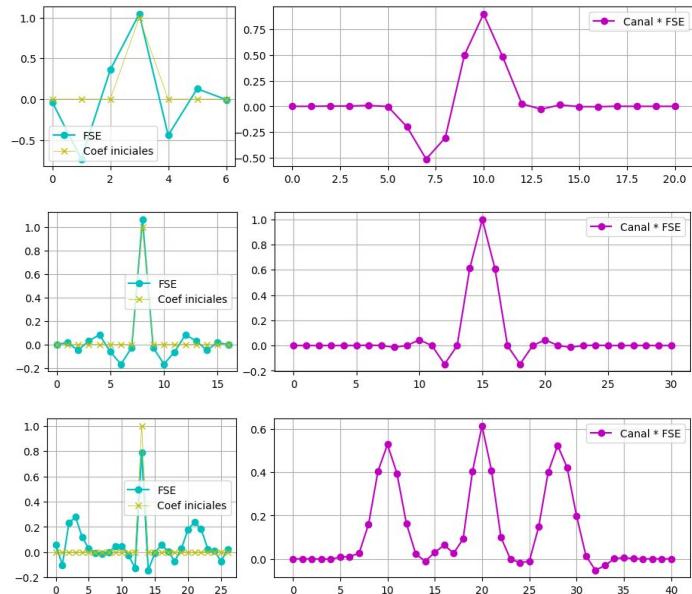
Ecualizador y adaptación de coeficientes: Cantidad de coeficientes



Respuestas al impulso antes del FSE

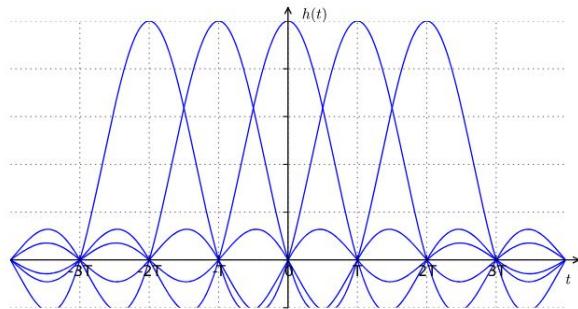
# FSE con LMS en punto flotante

Ecualizador y adaptación de coeficientes: Cantidad de coeficientes



Respuestas al impulso del FSE y total (canal más FSE) para 7 (arriba), 17 (centro) y 27 (abajo) coeficientes

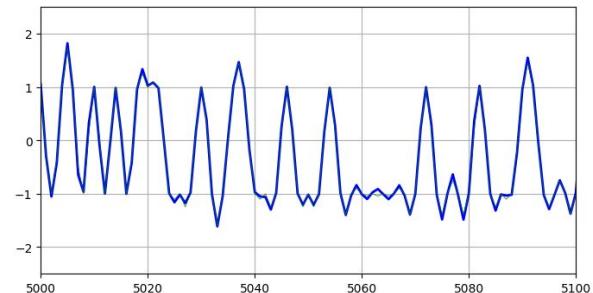
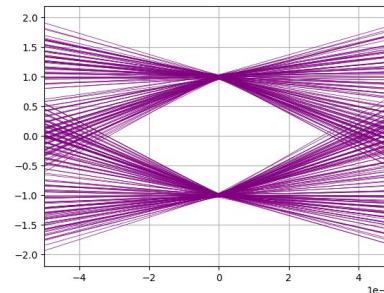
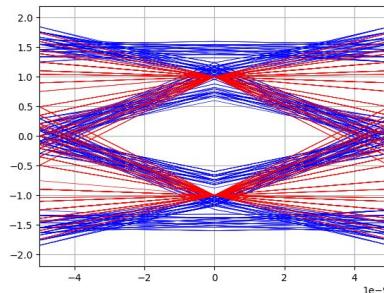
Criterio de Nyquist de cero ISI



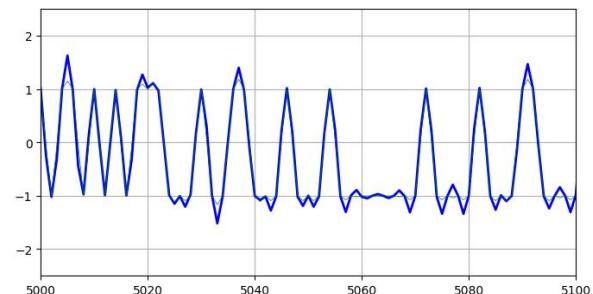
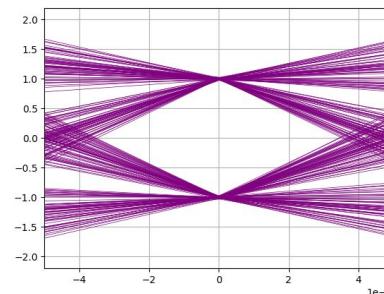
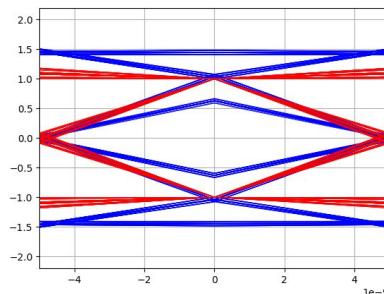
# FSE con LMS en punto flotante

Ecualizador y adaptación de coeficientes

$$\beta=0.3$$



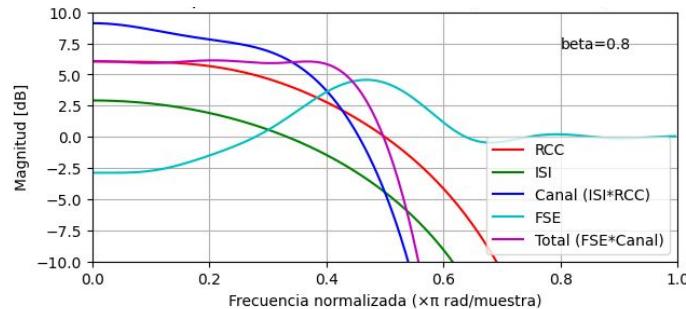
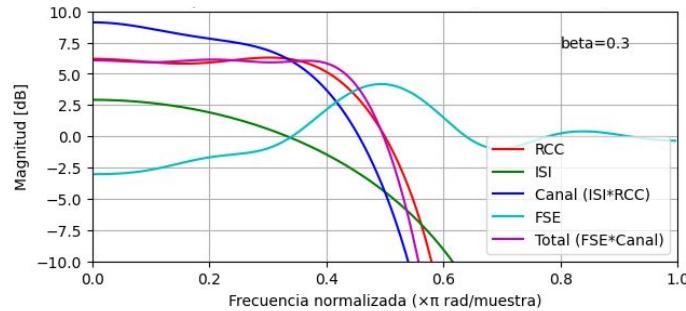
$$\beta=0.8$$



Señal de entrada con y sin ISI (izq.), diagrama de ojo de la salida del FSE (cen.) y salida en el tiempo (der.), para  $\beta=0.3$  (arriba) y  $\beta=0.8$  (abajo)

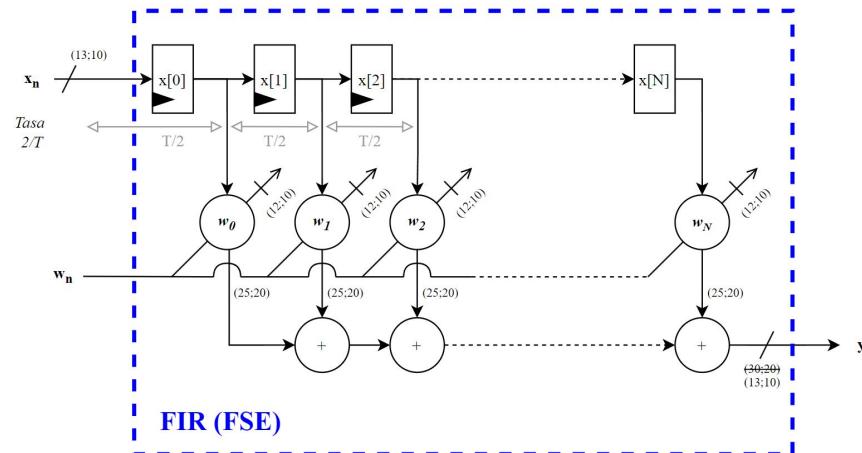
# FSE con LMS en punto flotante

Ecualizador y adaptación de coeficientes: Respuesta en frecuencia



# FSE con LMS en punto fijo

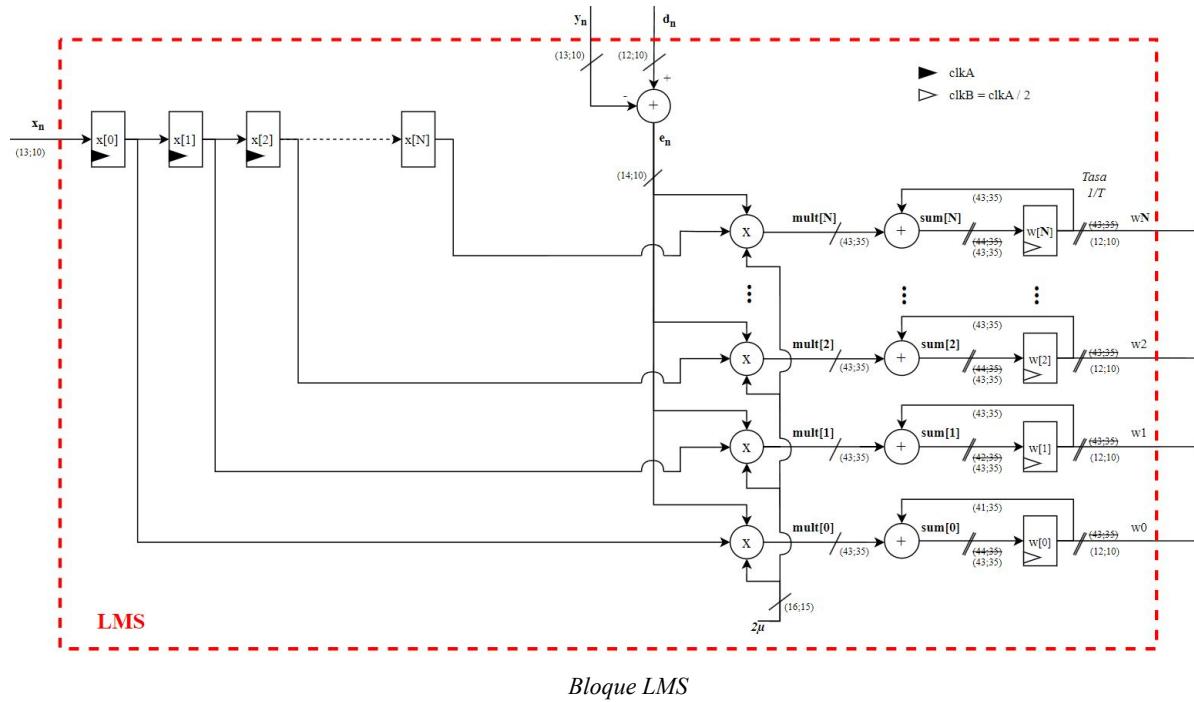
Filtro FIR del ecualizador fraccionalmente espaciado



Bloque FSE

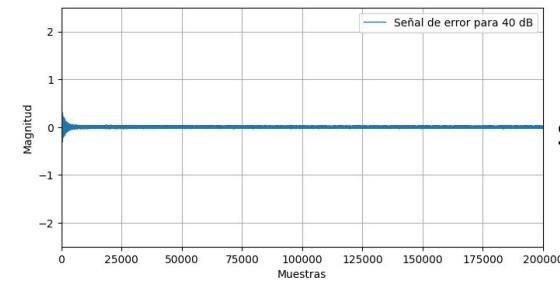
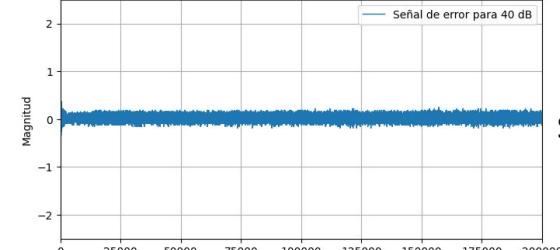
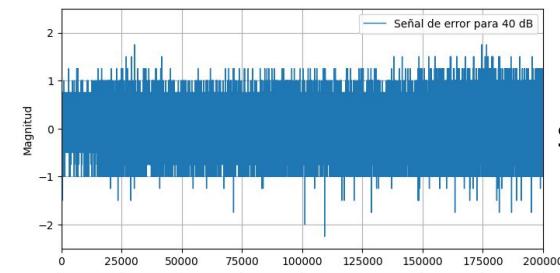
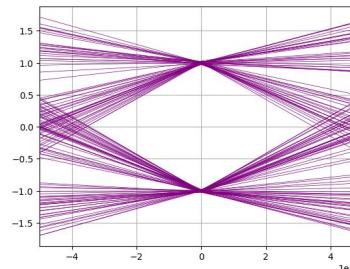
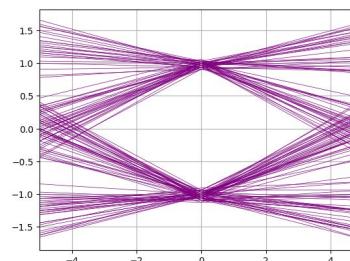
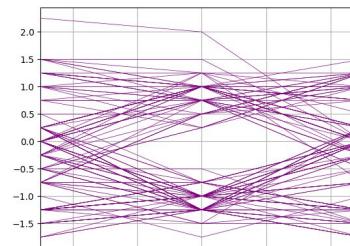
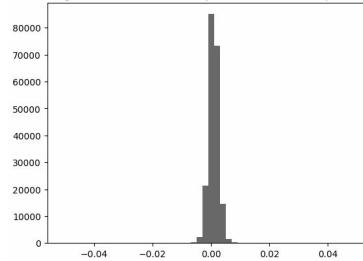
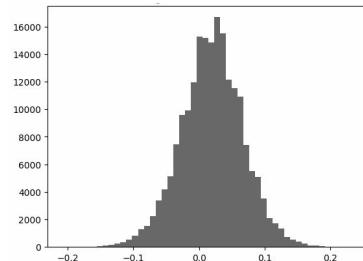
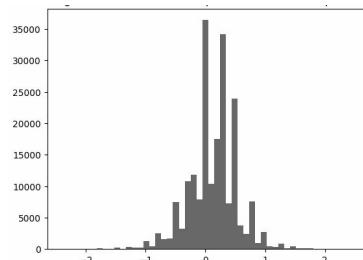
# FSE con LMS en punto fijo

Bloque del algoritmo de adaptación LMS



# FSE con LMS en punto fijo

## Cuantización



$s(5;2)$

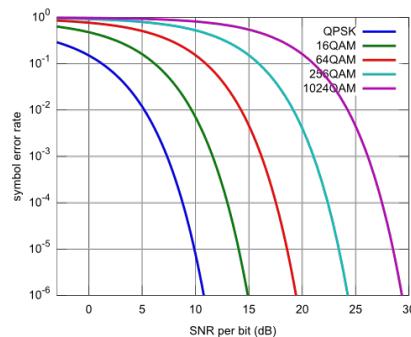
$s(8;5)$

$s(13;10)$

# FSE con LMS en punto fijo

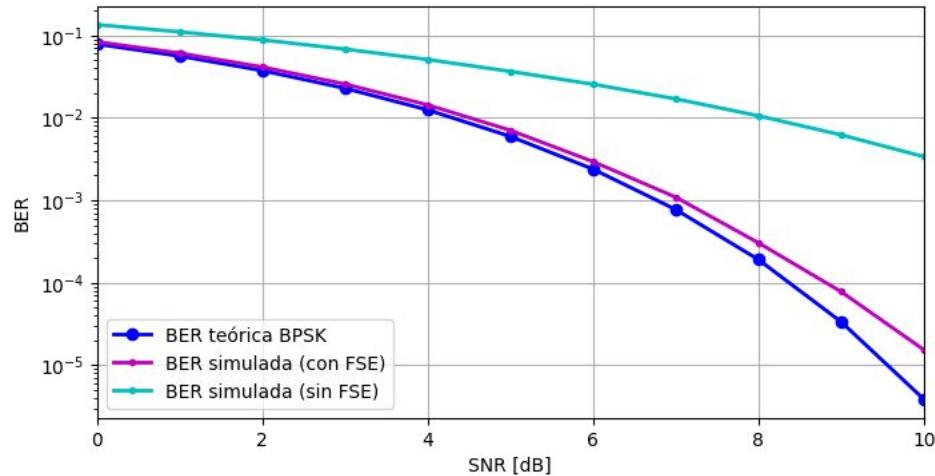
## Tasa de error de bits

- Oversampling de 2 ( $T/2$ )
- 17 coeficientes
- Coeficiente central inicial en 0.5
- Paso de aprendizaje  $\mu \approx 0.004$  para rápida convergencia y  $\mu \approx 0.0001$  para precisión cerca de la convergencia
- Cuantización  $s(13;10)$  para entrada y salida del FSE



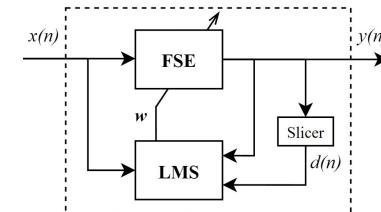
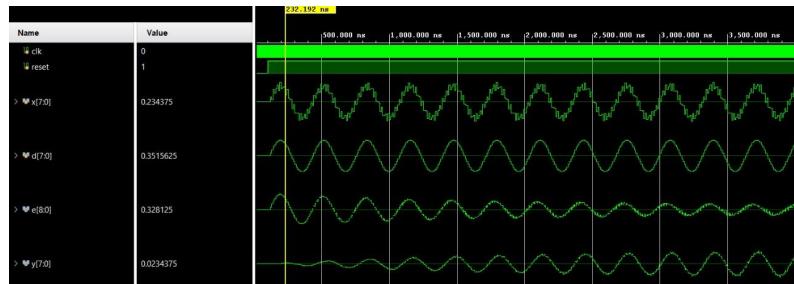
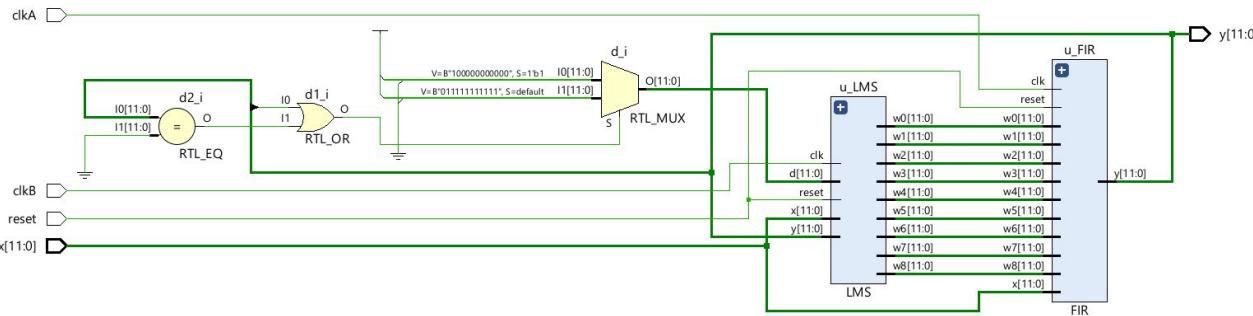
$$BER_{BPSK} = Q\left(\sqrt{2\frac{E_b}{N_0}}\right)$$

$$Q = \frac{1}{2} \operatorname{erfc}\left(\frac{x}{\sqrt{2}}\right)$$



# Descripción de bloques en HDL y análisis RTL

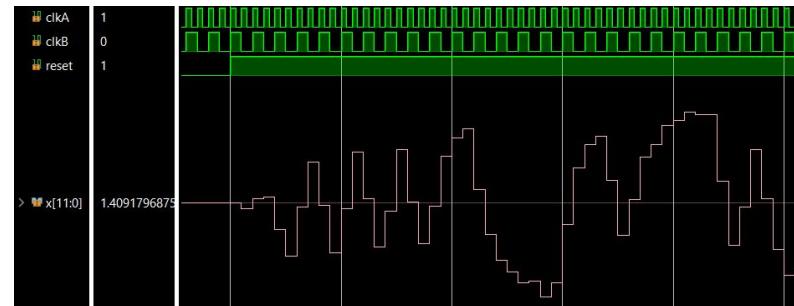
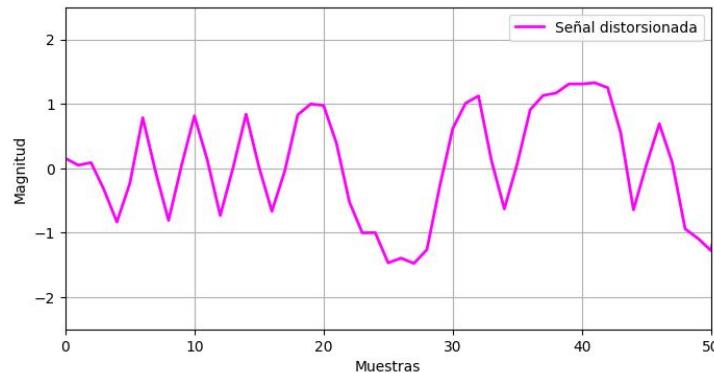
## Bloques básicos y testeos iniciales



# Descripción de bloques en HDL y análisis RTL

Generación de estímulos desde Python y lectura desde el Testbench

```
folder_path = r"C:\VivadoProjects\TrabajoFinalDDA\TrabajoFinalDDA.sim\sim_1\behav\xsim"
os.makedirs(folder_path, exist_ok=True)
filename = os.path.join(folder_path, 'ENTRADA.hex')
```



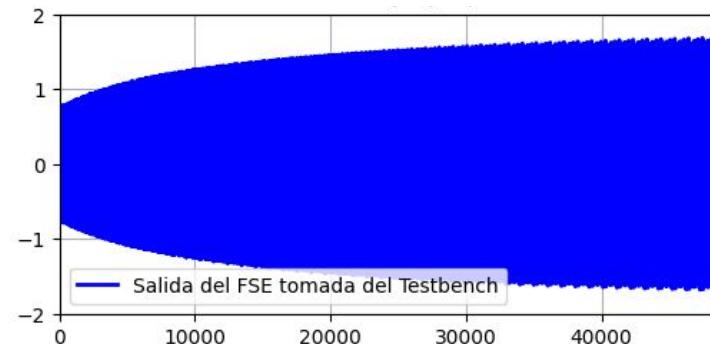
```
$readmemh ("ENTRADA.hex", entrada);

for (j=0; j<(TAM_MEM); j=j+1) begin
    x = entrada[j];
    #10;
end
```

# Descripción de bloques en HDL y análisis RTL

```
file = $fopen ("resultados.txt" , "w");

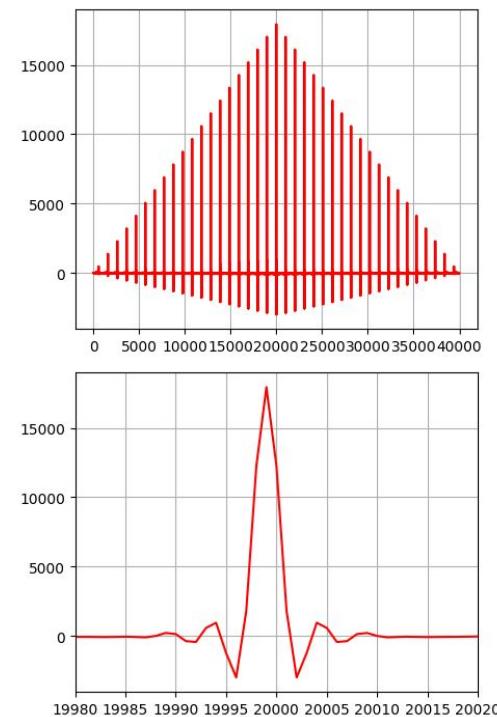
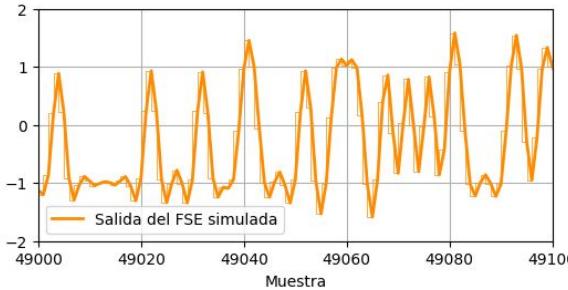
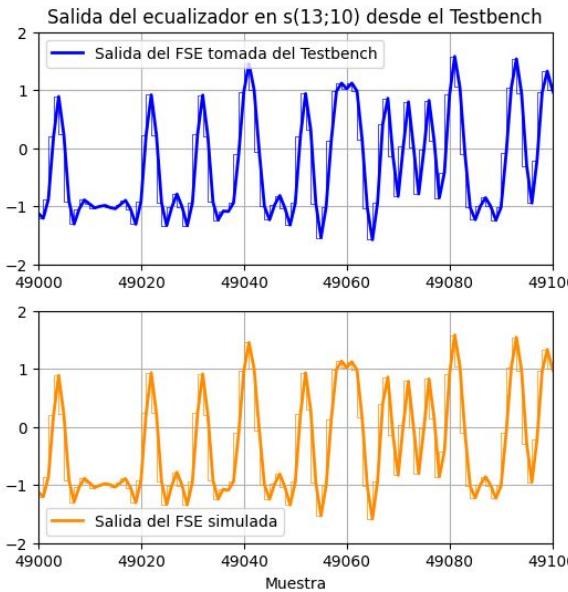
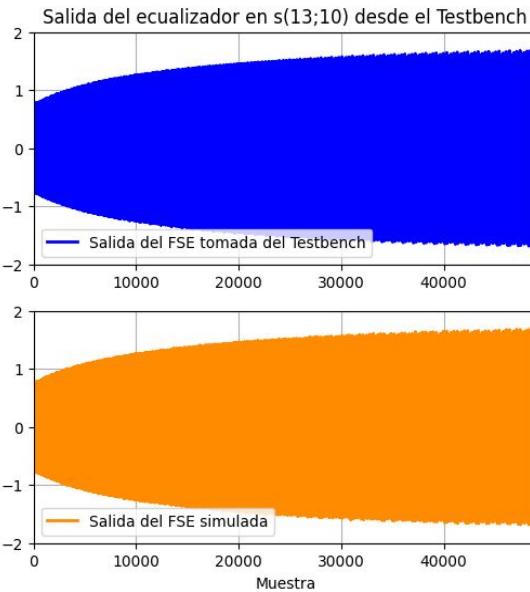
for (j=0; j<(TAM_MEM); j=j+1) begin
    $fwrite (file, "%0h\n", y);
    #10;
end
```



```
with open(r"C:\VivadoProjects\TrabajoFinalDDA\TrabajoFinalDDA.sim\sim_1\behav\xsim\resultados.txt", "r") as f:
    hex_values = [line.strip() for line in f if line.strip()]
```

# Descripción de bloques en HDL y análisis RTL

*Vector Matching* entre simulación de alto nivel y Testbench



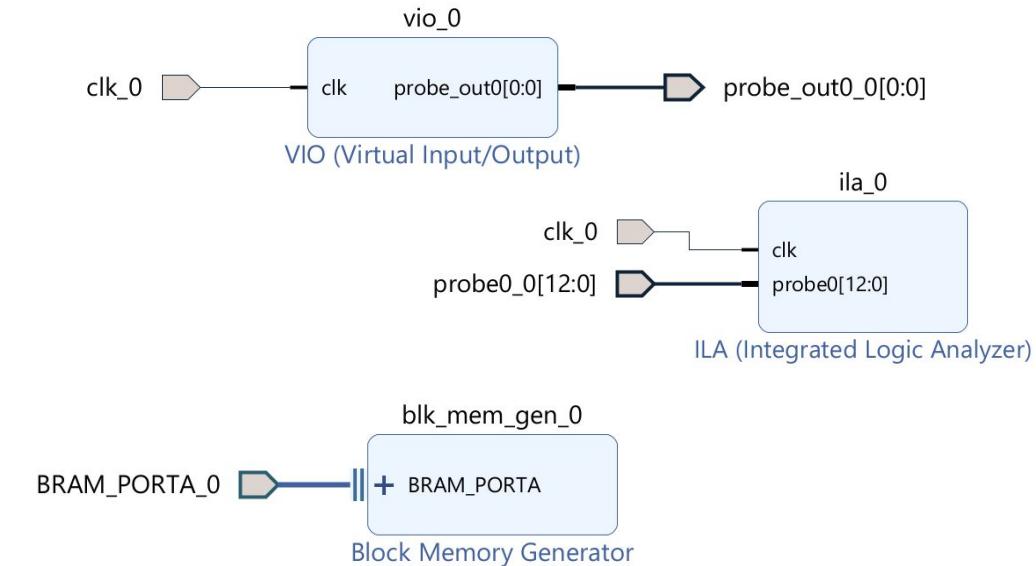
# Descripción de bloques en HDL y análisis RTL

Bloques añadidos para validar el diseño en placa

- ✓ □ Design Sources (4)
  - ✓ □ Verilog Header (1)
    - include.v
  - ✓ ● □ top (top.v) (5)
    - > ▲ □ u\_vio : vio (vio.bd) (1)
    - > ▲ □ u\_ilab : ila (ila.bd) (1)
    - ✓ ● ROMsignal\_inst : ROMsignal (ROMsignal.v) (1)
      - > ▲ □ u\_ROM\_bmg : ROM\_bmg (ROM\_bmg.bd) (1)
    - u\_FIR : FIR\_t (FIR\_t.v)
    - u\_LMS : LMS (LMS.v)

- ✓ □ Constraints (1)

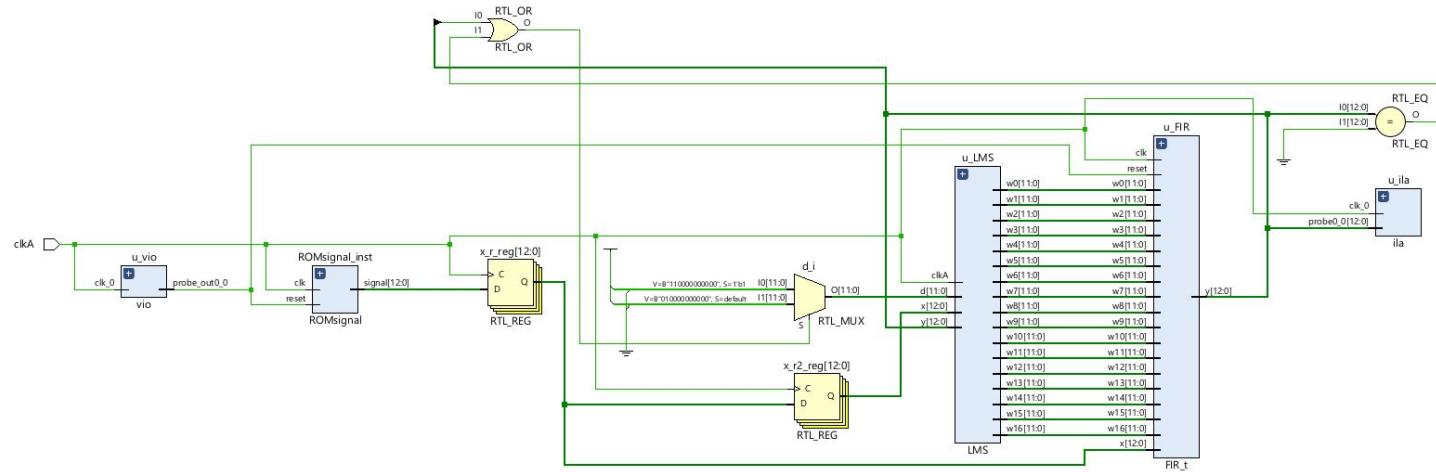
- ✓ □ constrs\_1 (1)
  - Constraint.xdc



*IP Cores utilizados*

# Descripción de bloques en HDL y análisis RTL

Bloques añadidos para validar el diseño en placa

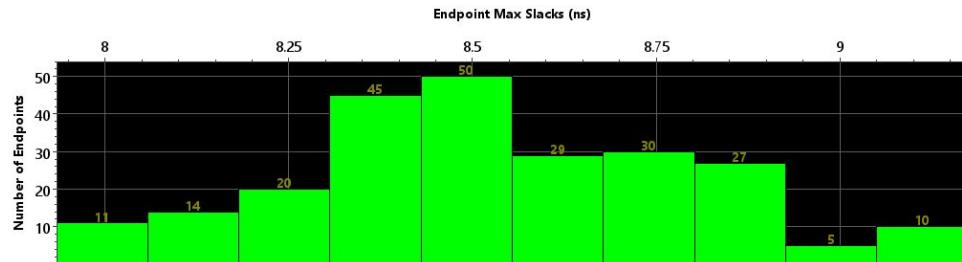


Esquemático completo pre-síntesis

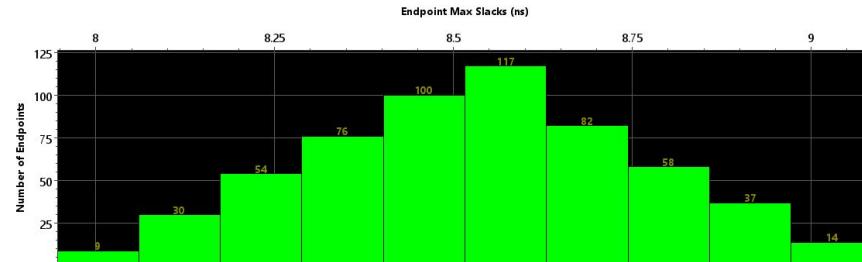
# Síntesis e Implementación

Comparación de implementación con 9 y 17 coeficientes (sin ROM, VIO e ILA)

Worst Negative Slack (WNS):	7.934 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	241



Worst Negative Slack (WNS):	7.946 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	577

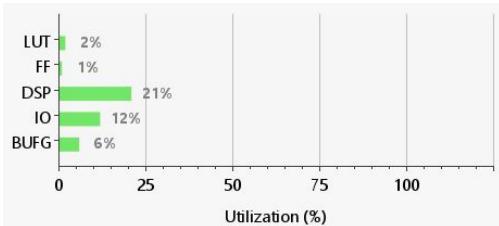


Comparación de resultados de timing para 9 y 17 taps

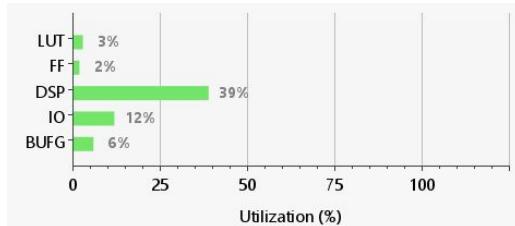
# Síntesis e Implementación

Comparación de implementación con 9 y 17 coeficientes (sin ROM, VIO e ILA)

Resource	Utilization	Available	Utilization %
LUT	369	20800	1.77
FF	359	41600	0.86
DSP	19	90	21.11
IO	26	210	12.38
BUFG	2	32	6.25



Resource	Utilization	Available	Utilization %
LUT	658	20800	3.16
FF	679	41600	1.63
DSP	35	90	38.89
IO	26	210	12.38
BUFG	2	32	6.25

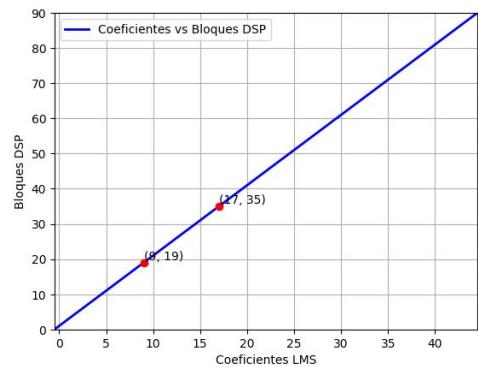


Comparación de reporte de utilización para 9 (izq.) y 17 (der.) taps

9 coeficientes → 19 bloques DSP (21,11%)

17 coeficientes → 35 bloques DSP (38,89%)}

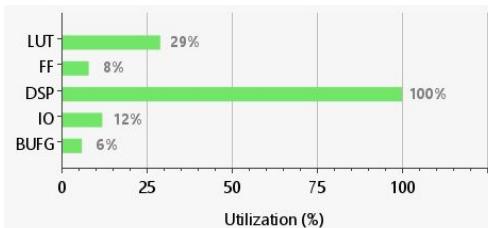
Se estiman unos 45 coeficientes para ocupar el 100% de DSPs



# Síntesis e Implementación

Implementación con 45 coeficientes (sin ROM, VIO e ILA)

Resource	Utilization	Available	Utilization %
LUT	5962	20800	28.66
FF	3418	41600	8.22
DSP	90	90	100.00
IO	26	210	12.38
BUFG	2	32	6.25



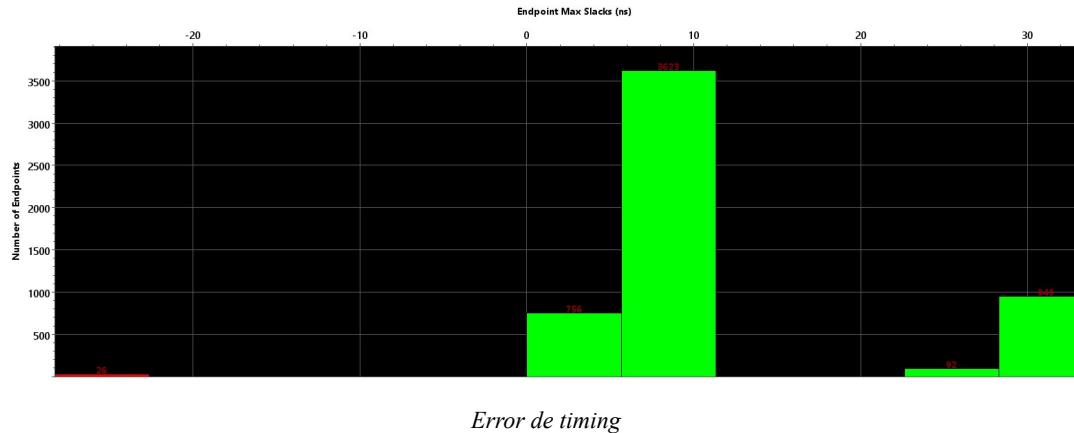
Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	LUT	FF	DSP	BRAM	URAM
✓ synth_1	constrs_1	Synthesis Out-of-date									547	359	19	0	0
✓ impl_1	constrs_1	Implementation Out-of-date	7.934	0.000	0.166	0.000		0.000	0.107	0	369	359	19	0	0
✓ synth_2	constrs_1	Synthesis Out-of-date									987	679	35	0	0
✓ impl_2	constrs_1	Implementation Out-of-date	7.946	0.000	0.158	0.000		0.000	0.139	0	658	679	35	0	0
✓ synth_3 (active)	constrs_1	<b>synth_design Complete!</b>									6027	3418	90	0	0
✓ impl_3 (active)	constrs_1	<b>route_design Complete!</b>	7.515	0.000	0.052	0.000		0.000	0.323	0	5962	3418	90	0	0

# Síntesis e Implementación

Implementación de diseño completo (ROM, VIO e ILA incluídos)

```
set_property -dict { PACKAGE_PIN E3 IO_STANDARD LVCMOS18 } [get_ports clkA]
create_clock -period 10.000 -name sys_clk_pin -waveform {0.000 5.000} -add [get_ports clkA]
```

synth_4 (active)	constrs_1	Synthesis Out-of-date									1390	1146	52	0.5	0
impl_4 (active)	constrs_1	Implementation Out-of-date	-24.602	-935.365	0.041	0.000	8.853	0.000	0.172	0	2517	3297	52	1	0



# Síntesis e Implementación

Implementación de diseño completo (ROM, VIO e ILA incluidos)

**Constraints**

Constraints: constrs\_1 (active)

**Report Settings**

Strategy: Vivado Synthesis Default Reports (Vivado Synthesis 2023)

**Settings**

Incremental synthesis: Automatically selected checkpoint

Strategy: Vivado Synthesis Defaults\* (Vivado Synthesis 2023)

Description: Vivado Synthesis Defaults

**Synth Design (vivado)**

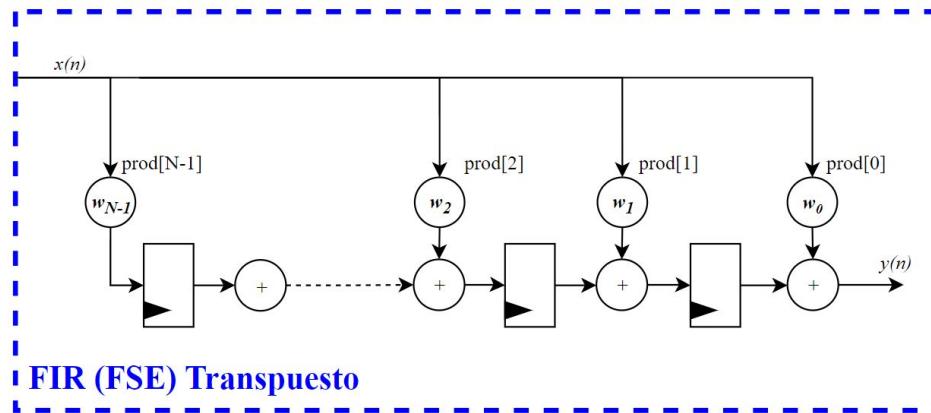
tcl.pre	rebuilt
tcl.post	off
-flatten_hierarchy	rebuilt
-gated_clock_conversion	off
-bufg	12
-directive	Default
<b>-retiming</b>	<input checked="" type="checkbox"/>
-no_retimining	<input type="checkbox"/>
-fsm_extraction	auto

**-retiming**  
Seeks to improve circuit performance for intra-clock sequential paths by automatically moving registers (register balancing) across combinatorial gates or LUTs. It maintains the original behavior and latency of the circuit and does not require changes to the RTL sources.

*Retiming automático*

# Síntesis e Implementación

Implementación de diseño completo (ROM, VIO e ILA incluídos)



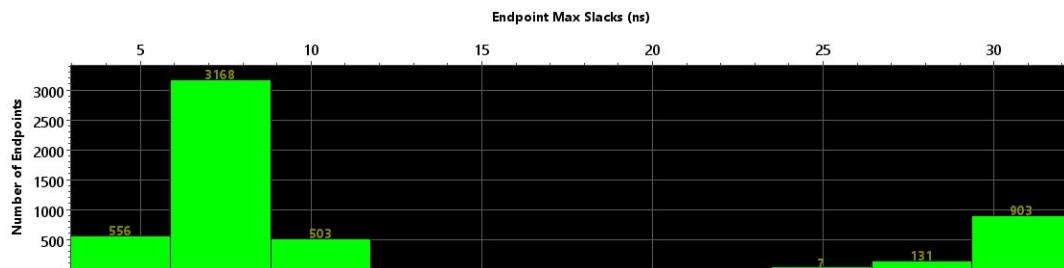
*FIR de estructura transpuesta*

# Síntesis e Implementación

Implementación de diseño completo (ROM, VIO e ILA incluidos)

Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	LUT	FF	DSP	BRAM	URAM
✓ synth_4 (active)	constrs_1	Synthesis Out-of-date									1764	1003	52	0.5	0
✓ impl_4 (active)	constrs_1	Implementation Out-of-date	2.944	0.000	0.038	0.000	9.140	0.000	0.080	0	1227	2108	17	1	0

Worst Negative Slack (WNS): 2.944 ns  
Total Negative Slack (TNS): 0 ns  
Number of Failing Endpoints: 0  
Total Number of Endpoints: 5268



Pasa timing

Summary	
Name	Path 21
Slack	2.944ns
Source	u_vio/vio_0/inst/PROBE_OUT_ALL_INST/G_PROBE_OUT[0].PROBE_OUT0_INST/Probe_out_reg[0]/C
Destination	u_FIR/sum_reg[16]/RSTB (rising edge-triggered cell DSP48E1 clocked by sys_clk_pin {rise@0.000}
Path Group	sys_clk_pin
Path Type	Setup (Max at Slow Process Corner)
Requirement	10.000ns (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
Data Path Delay	6.466ns (logic 0.580ns (8.970%) route 5.886ns (91.030%))
Logic Levels	1 (LUT1=1)
Clock Path Skew	-0.011ns
Clock U.tainty	0.035ns

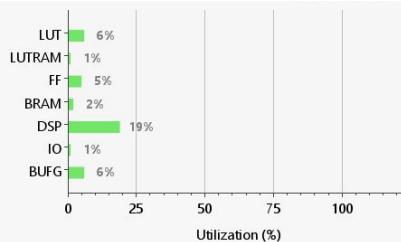
Slack Equation	
Required Time - Arrival Time	
Required Time	14.009ns
Arrival Time	11.065ns

# Síntesis e Implementación

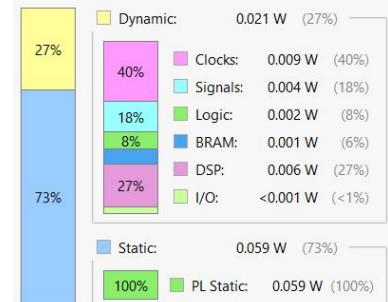
Implementación de diseño completo (ROM, VIO e ILA incluidos)

Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	LUT	FF	DSP	BRAM	URAM
synth_4 (active)	constrs_1	Synthesis Out-of-date									1764	1003	52	0.5	0
impl_4 (active)	constrs_1	Implementation Out-of-date	2.944	0.000	0.038	0.000	9.140	0.000	0.080	0	1227	2108	17	1	0

Resource	Utilization	Available	Utilization %
LUT	1227	20800	5.90
LUTRAM	96	9600	1.00
FF	2108	41600	5.07
BRAM	1	50	2.00
DSP	17	90	18.89
IO	1	210	0.48
BUFG	2	32	6.25



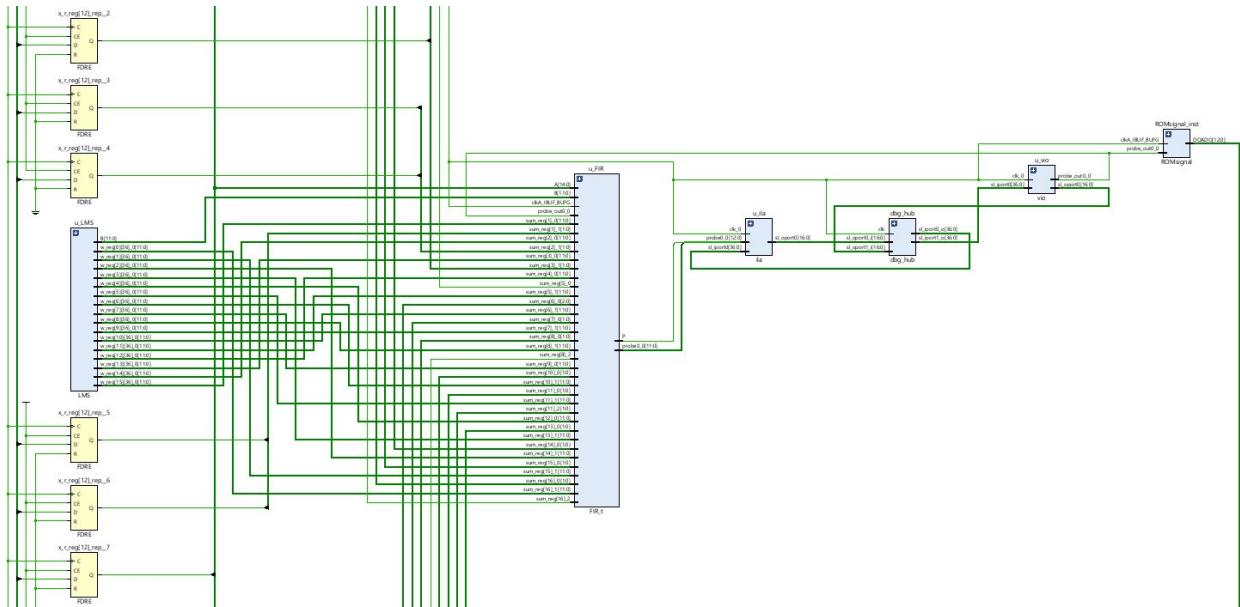
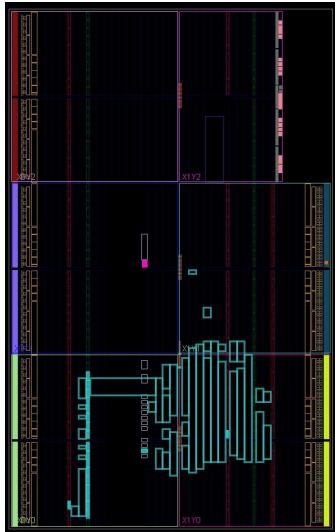
**Total On-Chip Power:** 0.08 W  
**Junction Temperature:** 25.4 °C  
Thermal Margin: 74.6 °C (15.5 W)  
Effective θJA: 4.8 °C/W  
Power supplied to off-chip devices: 0 W  
Confidence level: Medium



Resultados de área y potencia

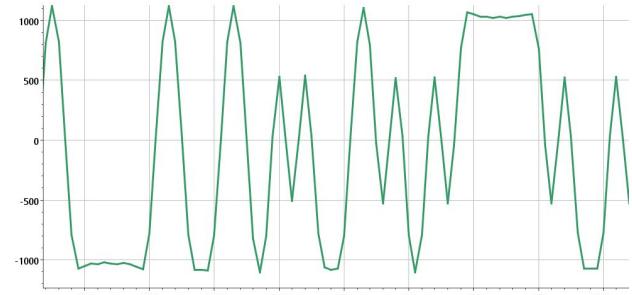
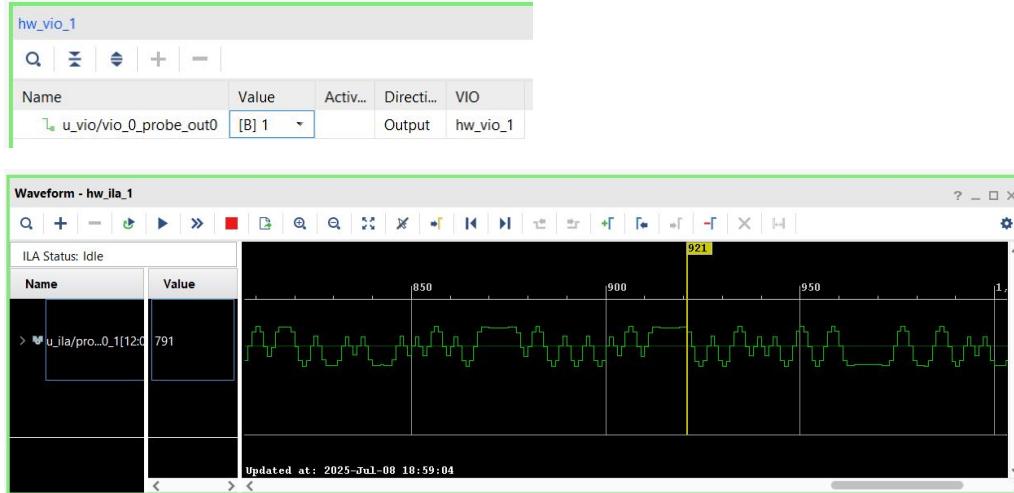
# Síntesis e Implementación

Implementación de diseño completo (ROM, VIO e ILA incluídos)



Dispositivo post-síntesis y esquemático de implementación

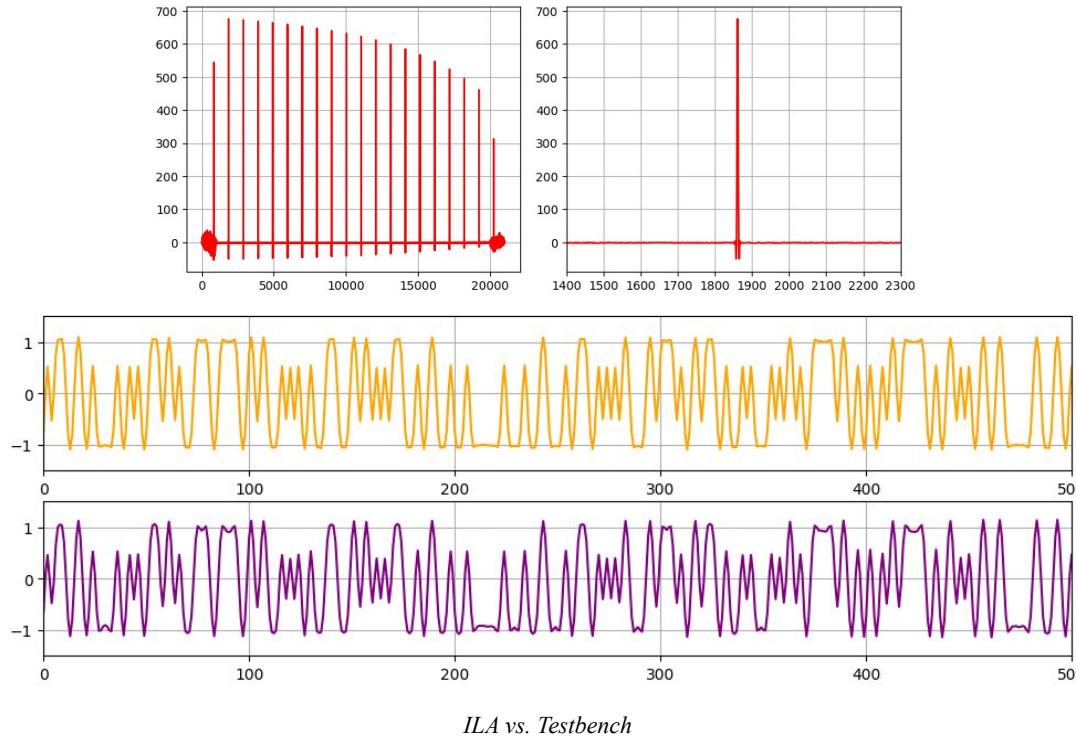
# Generación de bitstream e implementación en FPGA



```
Sample in Buffer, Sample in Window, TRIGGER, u_ilia/probe0_0_1[12:0]
Radix - UNSIGNED, UNSIGNED, UNSIGNED, SIGNED
0,0,0,-781
1,1,0,36
2,2,0,527
3,3,0,1
4,4,0,-542
5,5,0,-32
6,6,0,773
7,7,0,1063
8,8,0,1074
9,9,0,1083
10,10,0,784
11,11,0,-9
12,12,0,-824
13,13,0,-1120
```

VIO e ILA

# Generación de bitstream e implementación en FPGA



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# Muchas gracias

Ramiro

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