# UNIC-CASS Project

## Polyphase Transmission Filter

Fundación FULGOR

IEEE CIRCUITS AND SYSTEMS SOCIETY

# Project Design

- Design Title:
  - Polyphase transmission filter for QPSK modulation
- Design Acronym:
  - Tx-PPF

# Team Composition

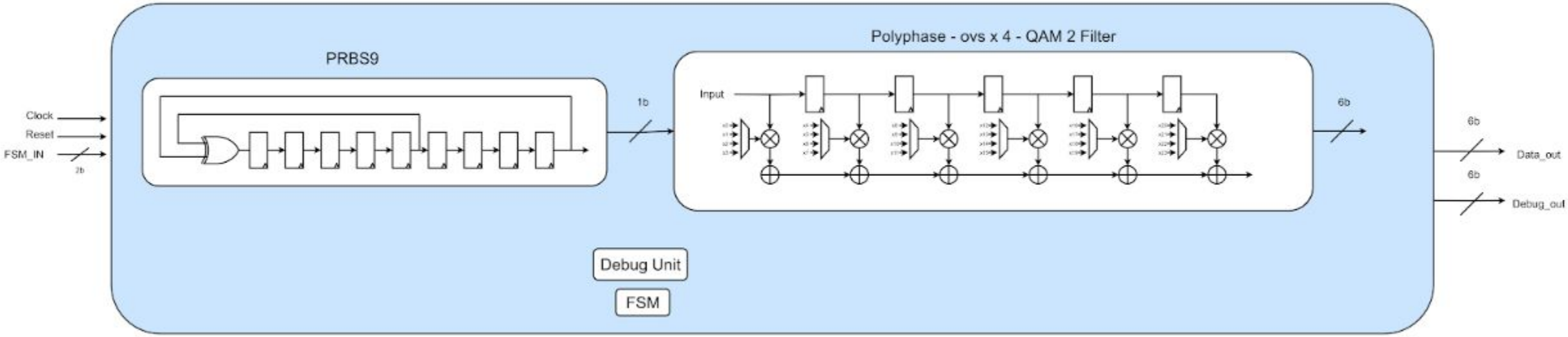
- Mariano Cárcamo
- Leslie Barrios Michel
- Ignacio Gatti
- Gabriel Iván Garcés

Design Team Composition

| | First Name | Middle Name | Last Name | Email | IEEE Membership Number | University Name | Expected Graduation Date (*1) |
|---|---|---|---|---|---|---|---|
| Member 1 | Mariano | Gabriel | Cárcamo | mgcarcamo@gmail.com | 101674818 | Univeridad Nacional del Sur - Argentina | 2026/12 - Master degree - Digital Design |
| Member 2 | Gabriel | Iván | Garcés | gabrielgarces.bariloche@gmail.com | 101682867 | Universidad Nacional del Sur - Argentina | 2026/12 - Master degree - Digital Design |
| Member 3 | Ignacio | Ezequiel | Gatti | Ignaciogatti3102@gmail.com | - | Universidad Tecnológica Nacional - Argentina | 2025/12 - Electronic engineering |
| Member 4 | Leslie | Elisa | Barrios Michel | leselisabm@gmail.com | 99038240 | Universidad Mayor de San Andrés | 2025/12/12 - Bachelor Degree - Electronic engineering |
| Member 5 | | | | | | | |
| Mentor 1 | Ariel | Luis | Pola | | 91235587 | Universidad Nacional del Sur - Argentina | Graduated Ph.D. |

*1: For example "2020/03/31" in the format of 20YY/MM/DD.

# Diagram for main blocks



# Design Details

- ## Description of the idea:

This project presents the design of a **Polyphase Transmit Filter** for generating an upsampled baseband signal for **QAM-2 modulation**. The filter performs **×4 upsampling** using **24 taps** on the input signal. In addition, a **Finite State Machine (FSM)** and a **Debug Unit** are included for control and diagnostic purposes.

The architecture comprises the following key digital blocks:

- **PRBS9 Generator**: Produces a pseudo-random bit sequence as the input stream for verification, enabling realistic stimulus while validating spectral shaping and upsampling performance.
- **Polyphase FIR Filter**: Implemented with four phases of six taps each, it processes 1-bit input samples to generate oversampled QAM-2 outputs efficiently.
- **Output Stage**: Performs rounding and saturation to ensure 6-bit I/Q outputs suitable for DAC interfacing.
- **FSM**: Controls the system using two-bit inputs, enabling the transmit filter and the debug unit as required.
- **Debug Unit**: Outputs the PRBS stream, the current polyphase filter phase, and the FSM state for monitoring and debugging.

Unlike conventional zero-insertion upsampling, the polyphase filter interpolates efficiently while preserving spectral quality and minimizing hardware cost. With carefully designed and quantized coefficients, this architecture offers a **compact, scalable solution for high-speed transmitters**.

# Design Details

- Input Pins:
  - Clock:  1 pin
  - Reset:  1 pin
  - FSM_in:  2 pin
  - VCD + GND: 2 pin
- Output Pins:
  - data_out:  6 pins
  - debug_unit_out: 6 pins

**Estimated Number of Pins:***

Input: * 6

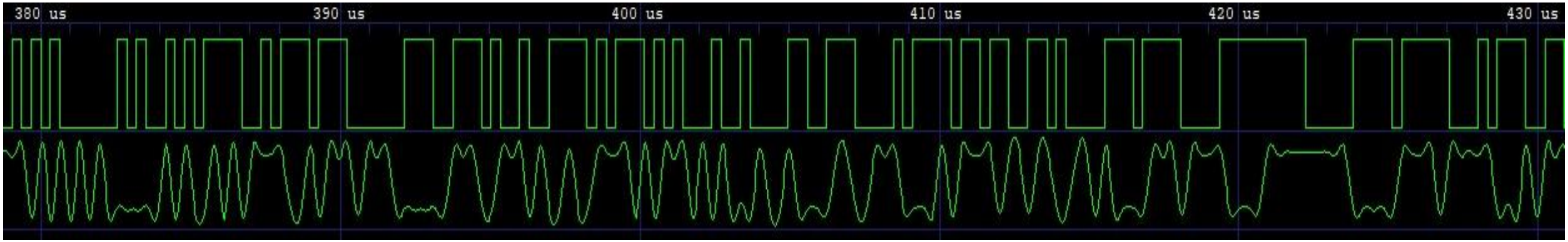
Output: * 12

Bidirectional: * 0

ihp 130 nm

# RTL Simulations:

## Polyphase SRRC filter input and output respectively:




## Polyphase SRRC filter impulse response: