Design of a High-performance amplifier with a bandwidth of 500 MHz

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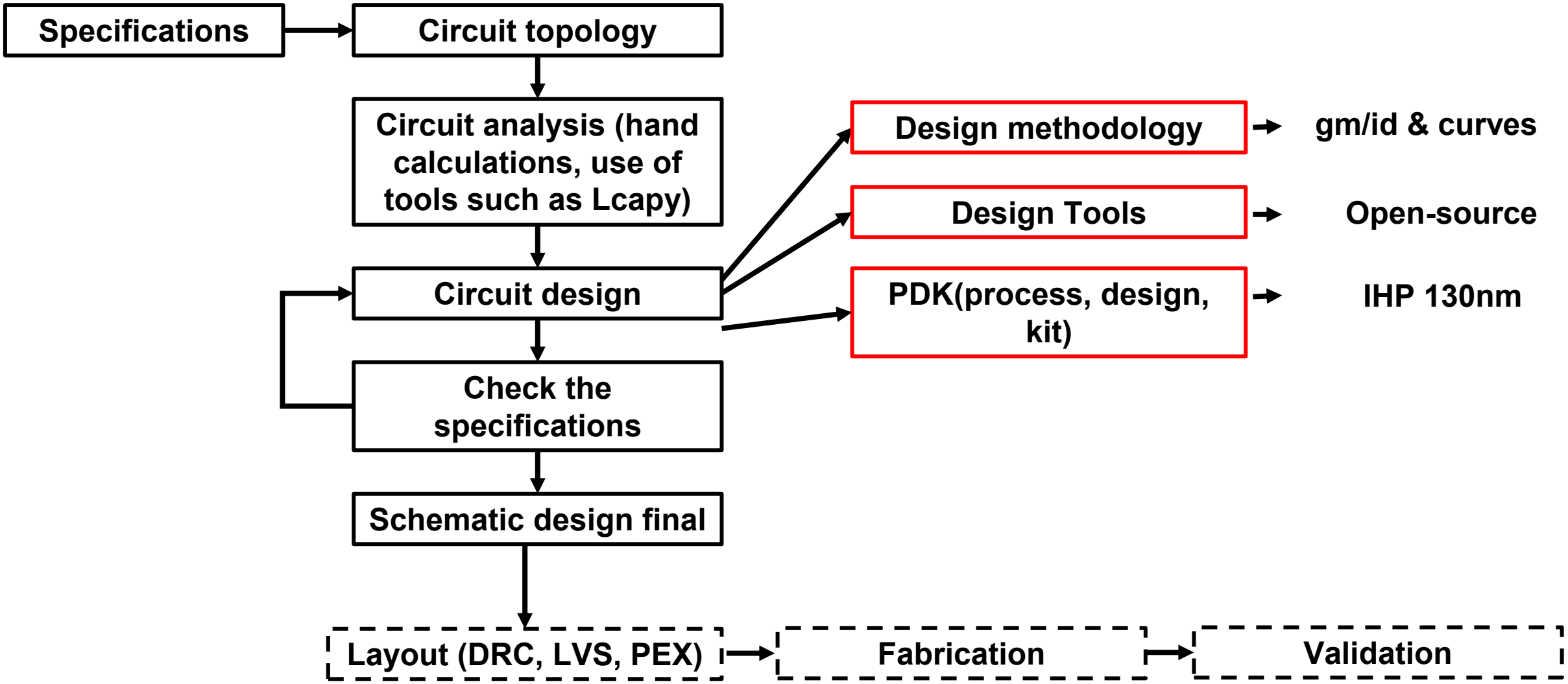
Outline

- Design Flow
- Specifications and requirements
- Topology of HPA
- Circuit Implementation
- Measurements Open Loop HPA
- Measurements Close Loop HPA

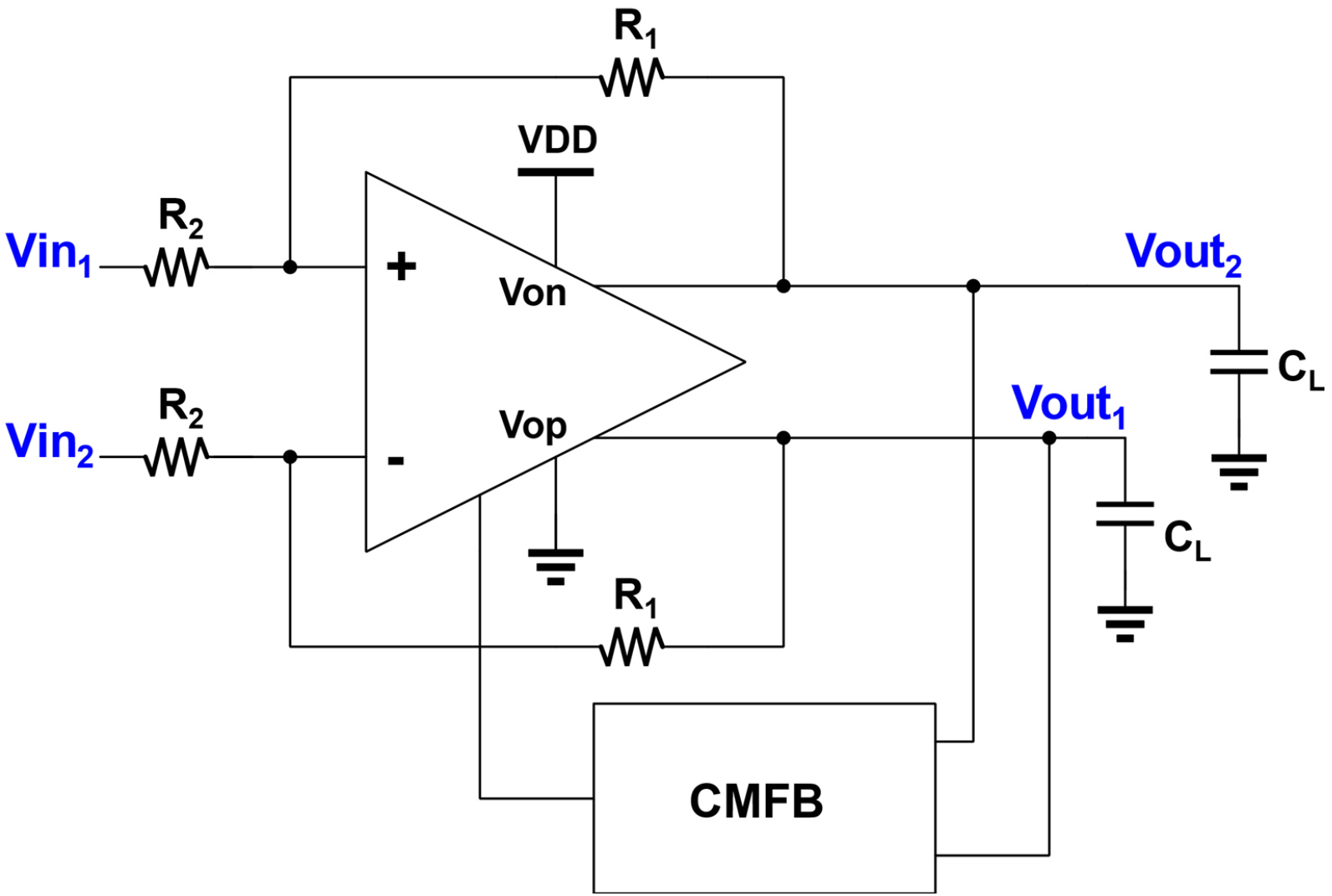
Design flow


Specifications
Circuit topology
Circuit analysis (hand calculations, use of tools such as Lcapy)
Circuit design
Check the specifications
Schematic design final
Layout (DRC, LVS, PEX)
Fabrication
Validation
Design methodology
gm/id & curves
Design Tools
Open-source
PDK(process, design, kit)
IHP 130nm

Specifications and requirements

HPA Specifications	
Boundary Conditions	**Requirement**
Techn.	CMOS
Node	130 nm
Supply Voltage	1.8 ± 10% V
Temperature	[0, 65, 125] °C
CL	0.5 pF
Bias current	100 ± 5% uA
Output Type	Fully Differential
Specifications	**Value**
Close loop bandwidth ($f_{c\text{-}3dB}$)	≥500 MHz
Close loop gain (A_{vCL})	7 ± 0.1 dB
Output Swing	500 mVpp
ENOB @ 100 MHz	≥ 9 bits
ENOB @ 400 MHz	≥ 7.5 bits

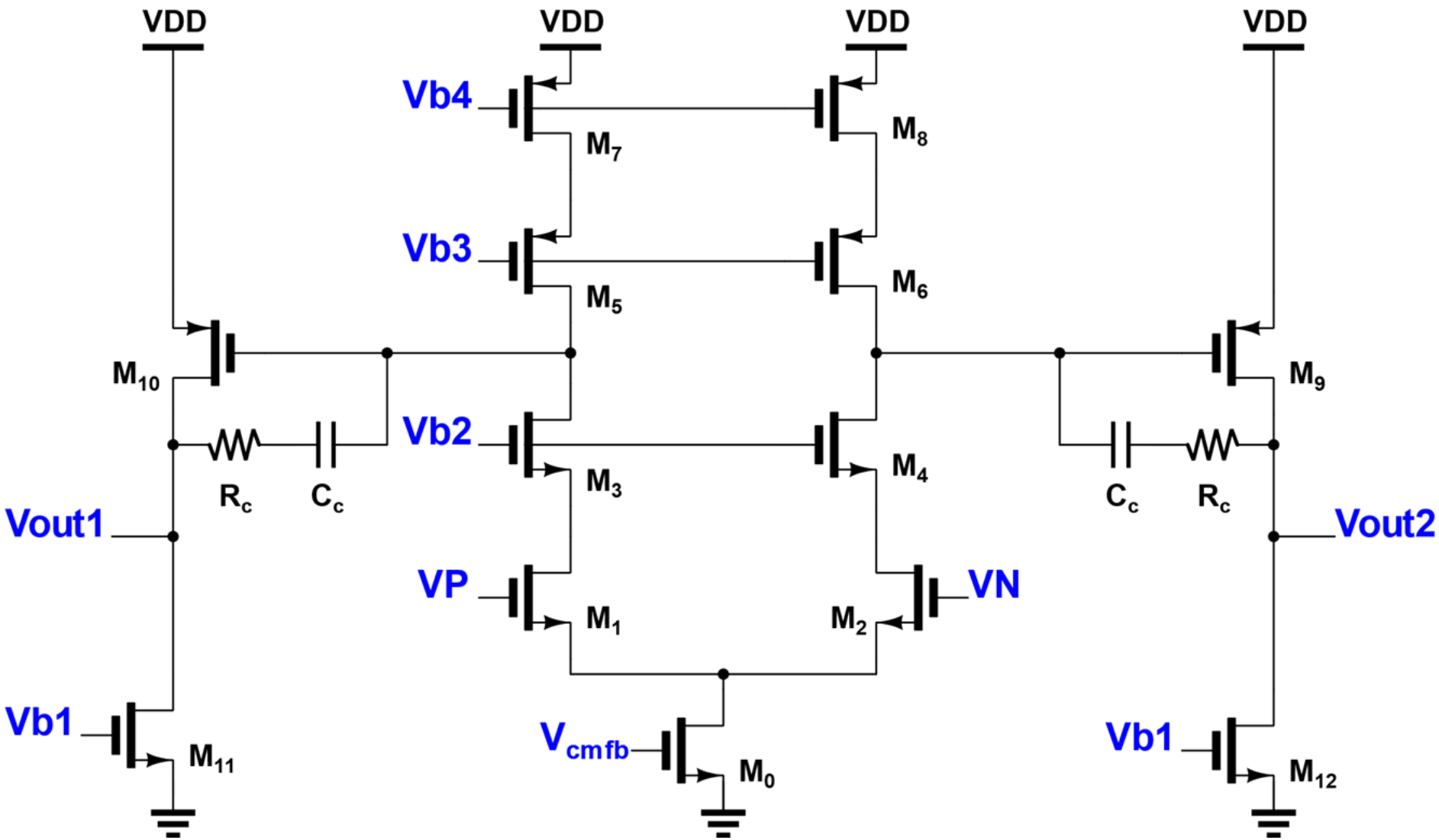
HPA feedback loop configuration



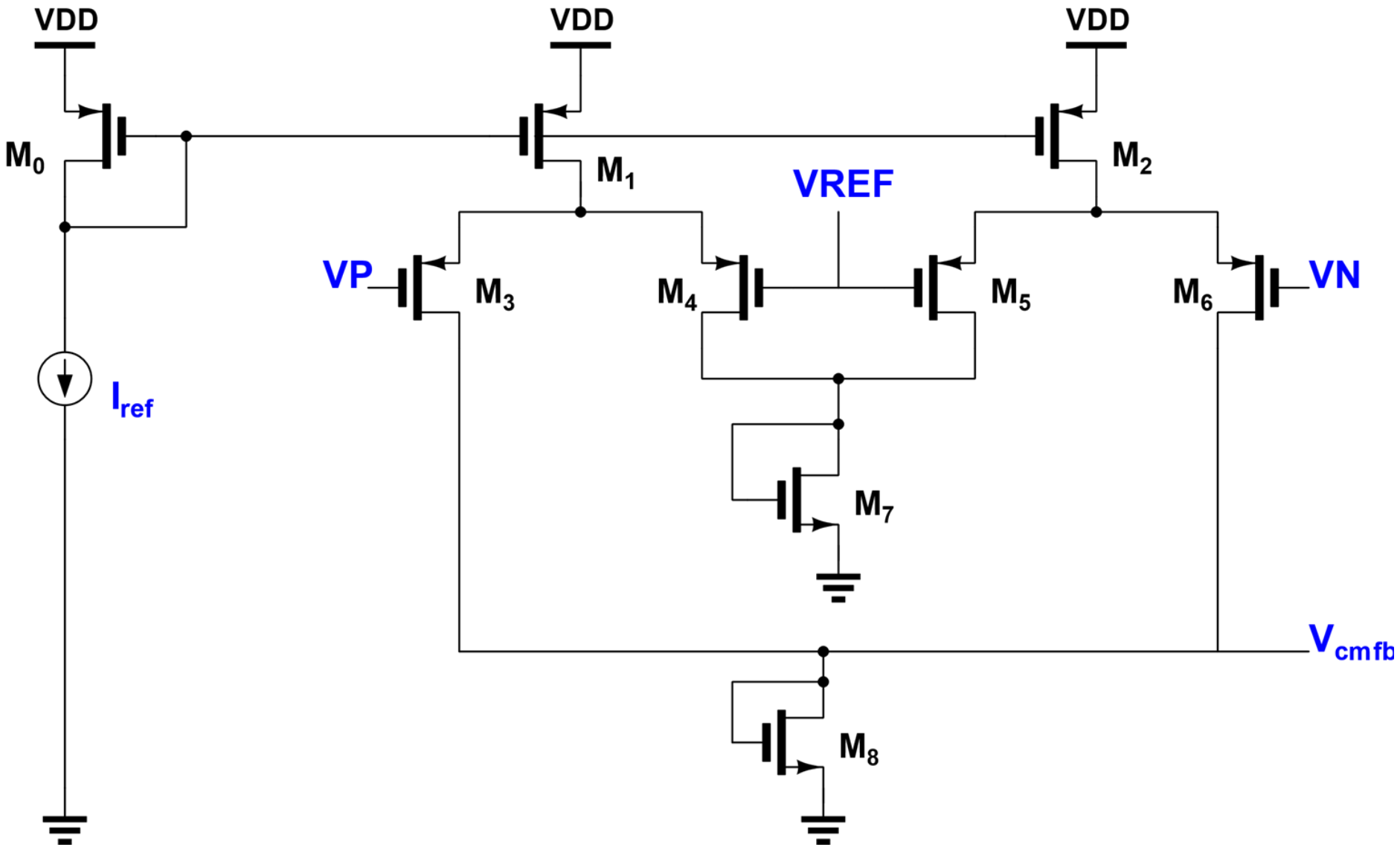
$$A_{vCL} = \frac{R_1}{R_2}$$

$$C_L = 0.5\ pF$$

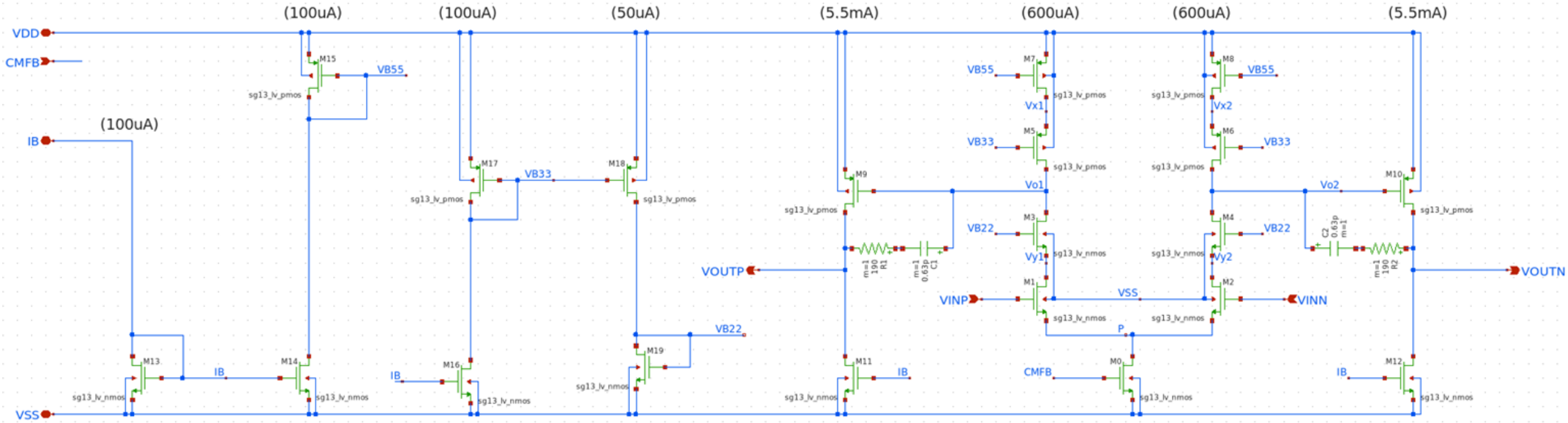
Topology of HPA



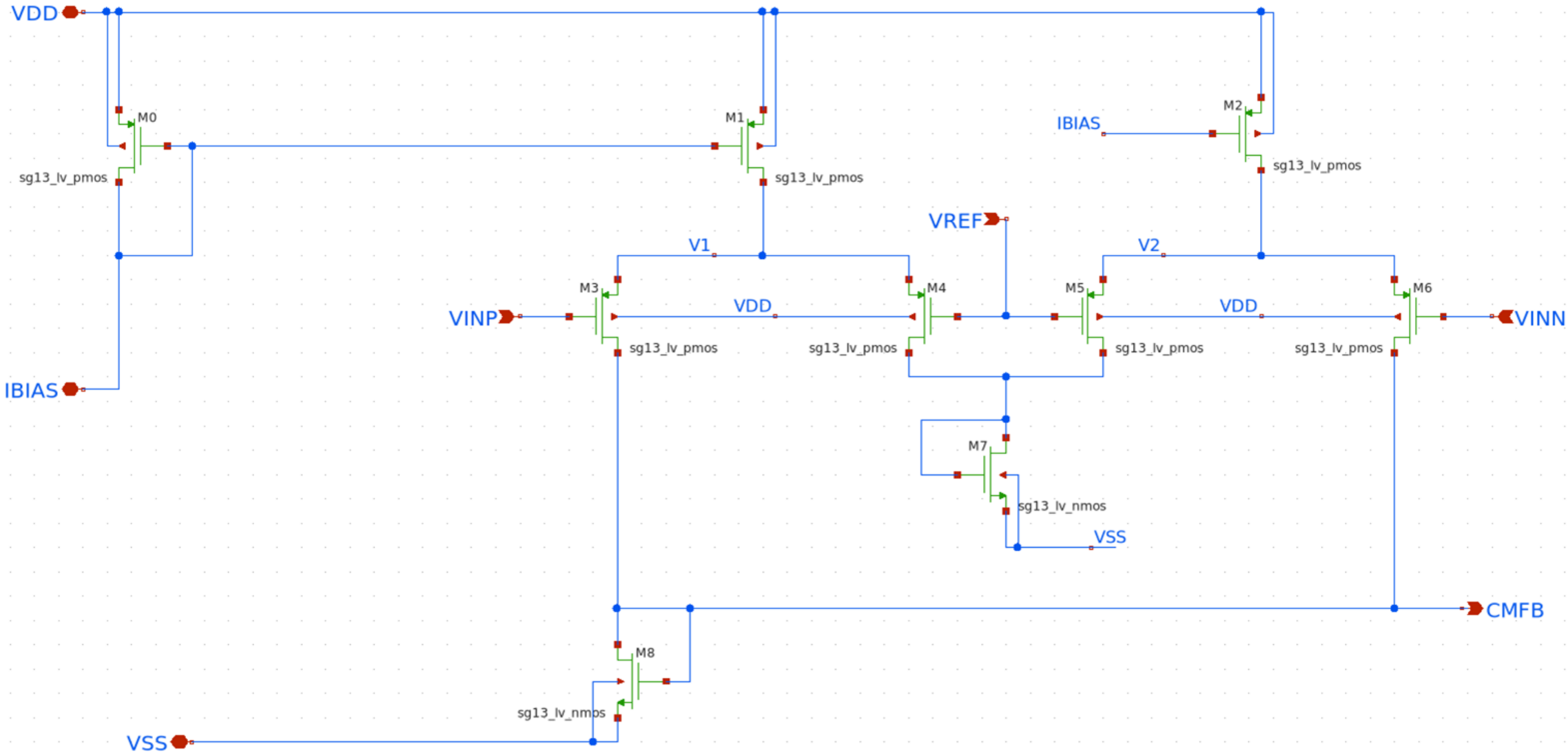
Topology of HPA



Circuit Implementation



Circuit Implementation

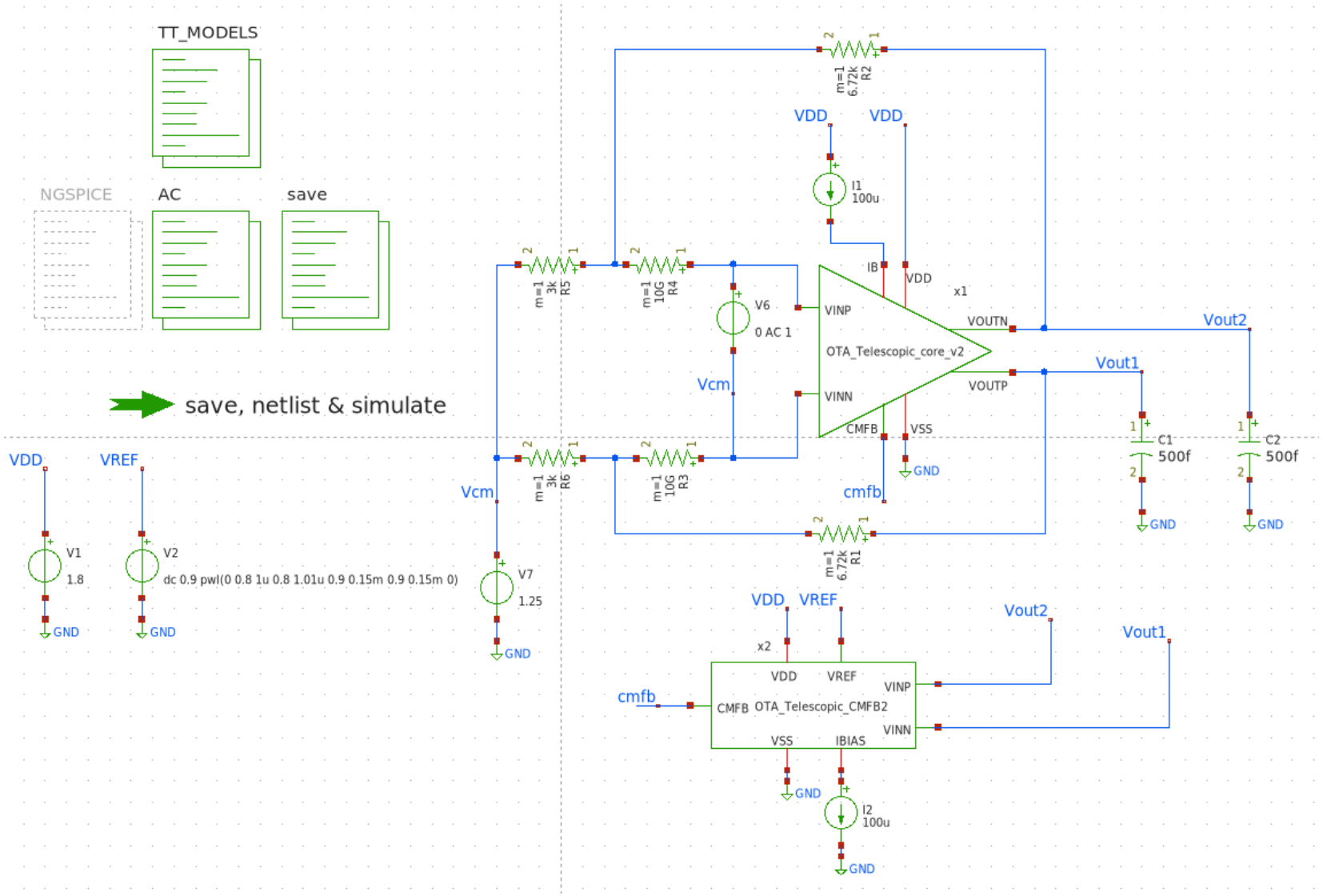


Corners

- PVT(Process, Voltage, Temperature) variations:

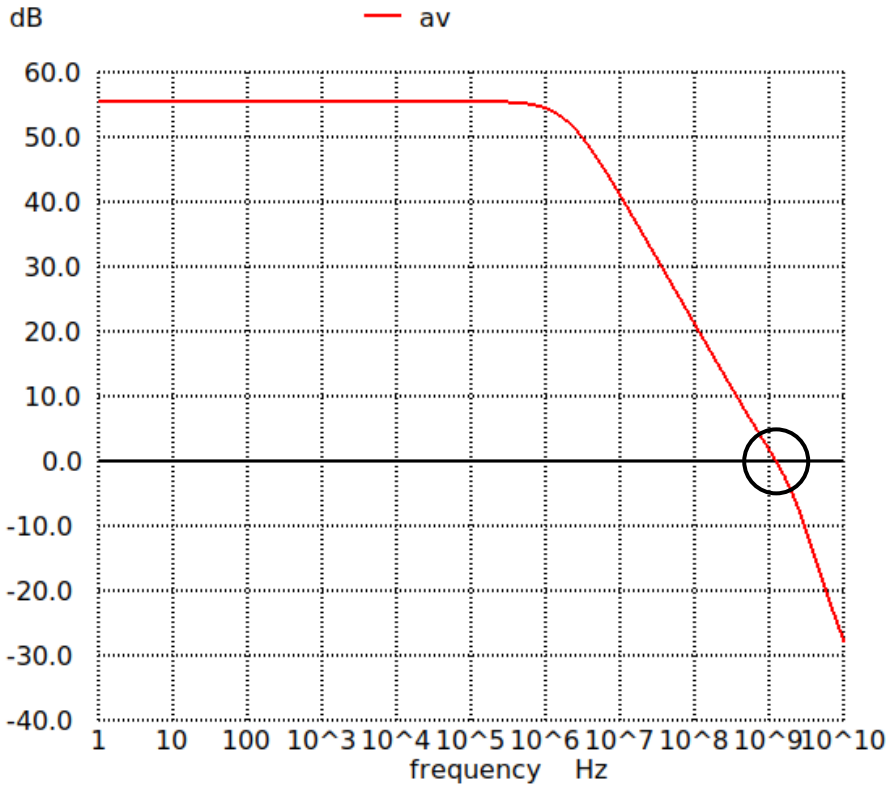
Corner	Temperature [°C]	VDD [V]	Iref [uA]
SS: Slow	125	1.62	95
TT: Typical	65	1.8	100
FF: Fast	0	1.98	105

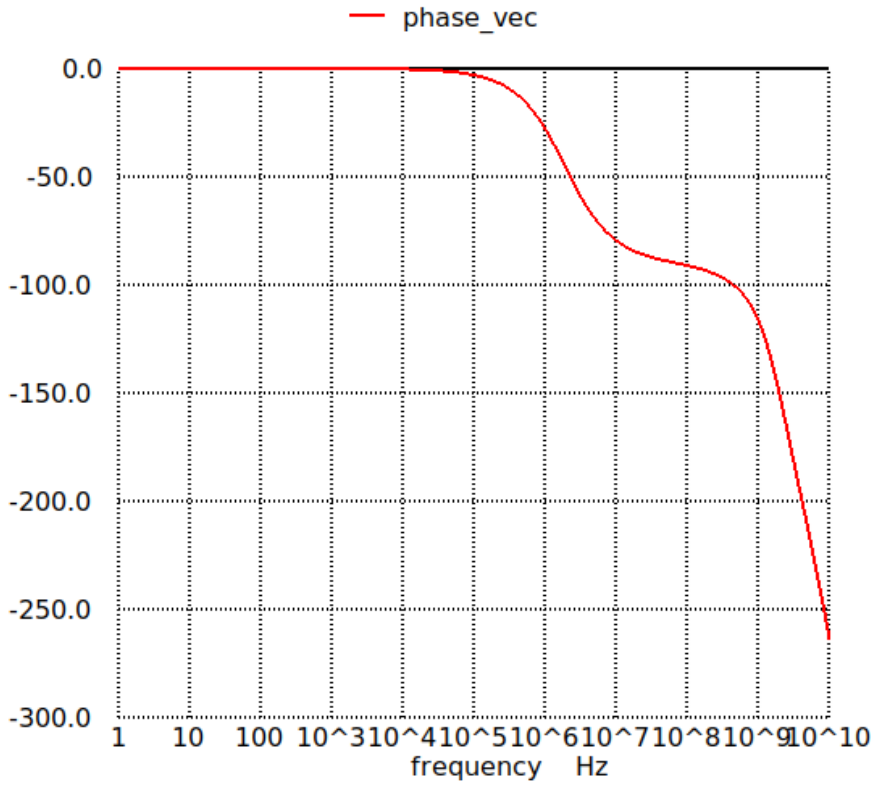
Open loop HPA



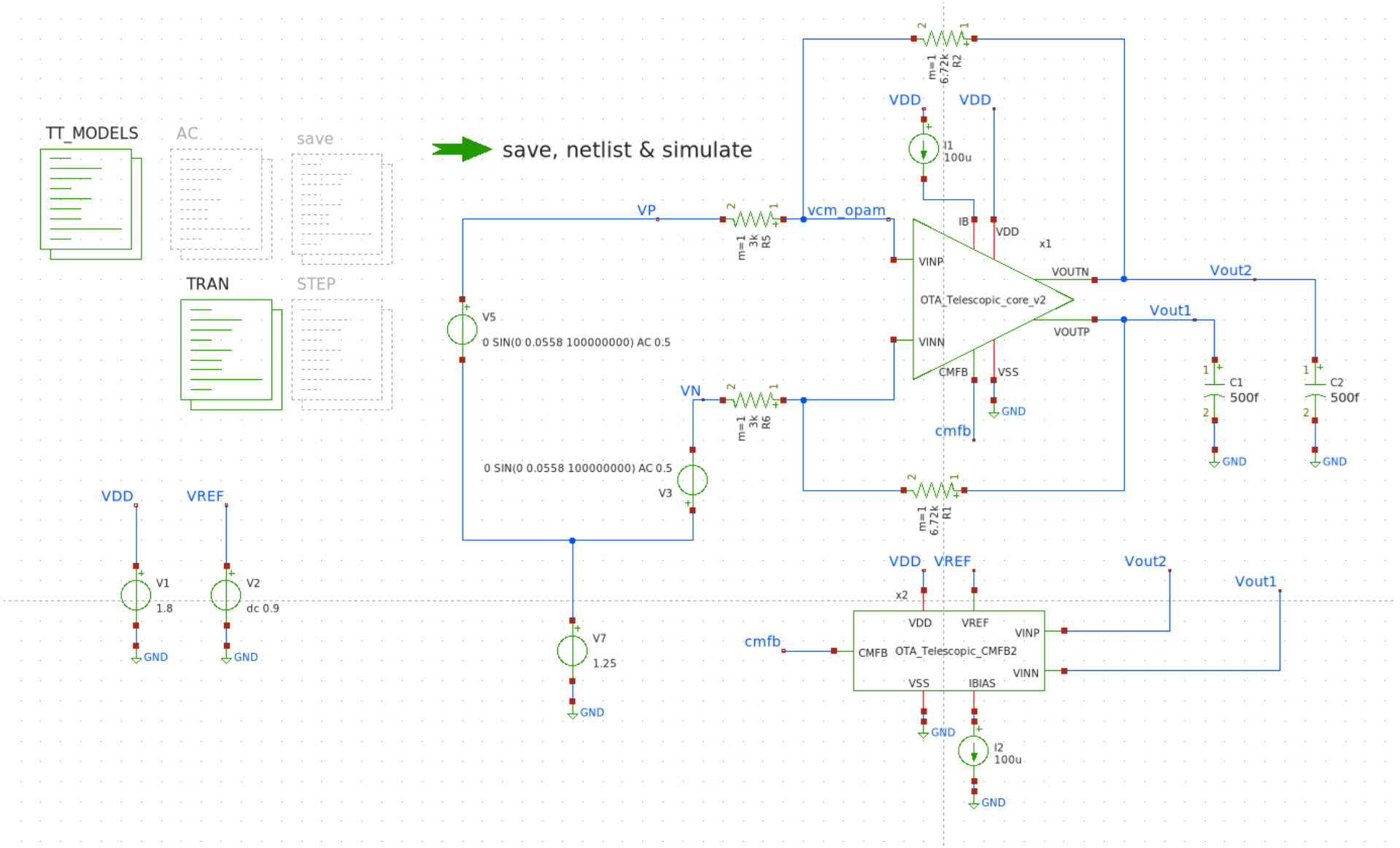
Measurements Open Loop HPA

Spec	Target	Slow	Typical	Fast
Open loop gain (A_{VCL})	≥ 44.35 dB	To do	55.5 dB	To do
Phase Margin	≥ 60 °	To do	56.2 °	To do
Unity Gain Bandwidth (UGB)	≥ 795 MHz	To do	1240 MHz	To do



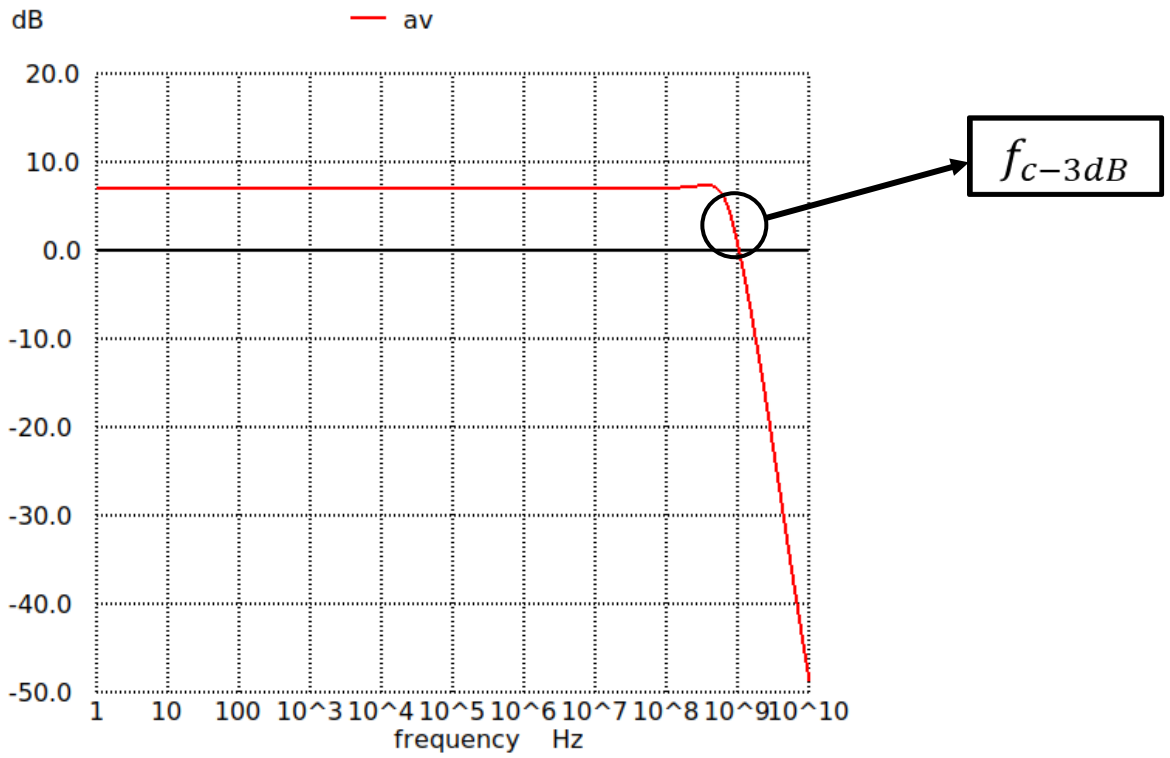


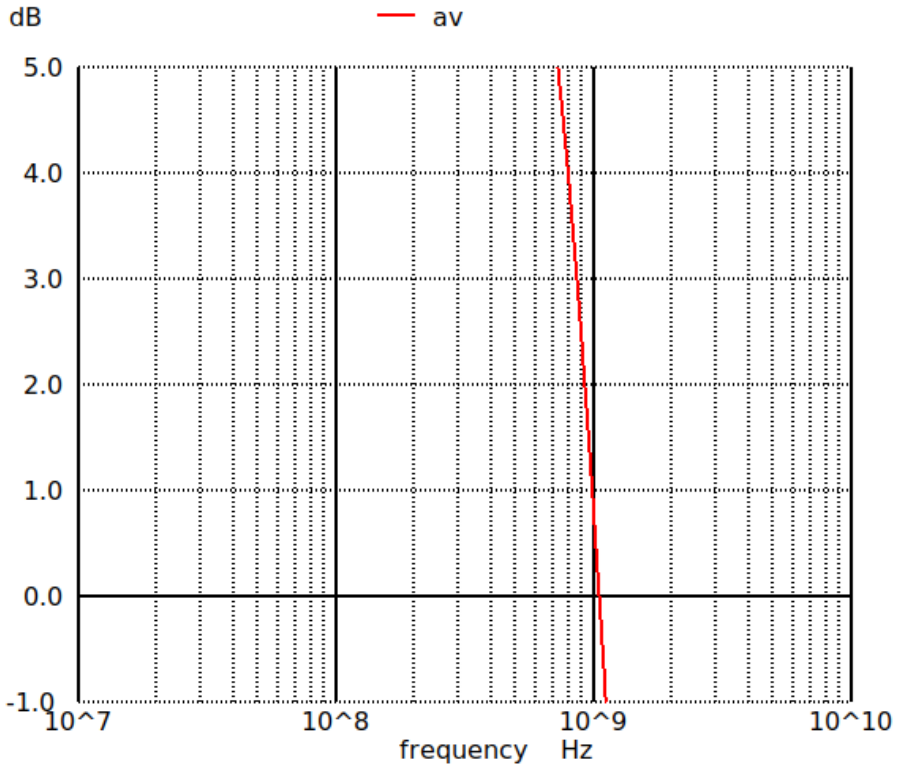
Close Loop HPA



Measurements Close Loop HPA

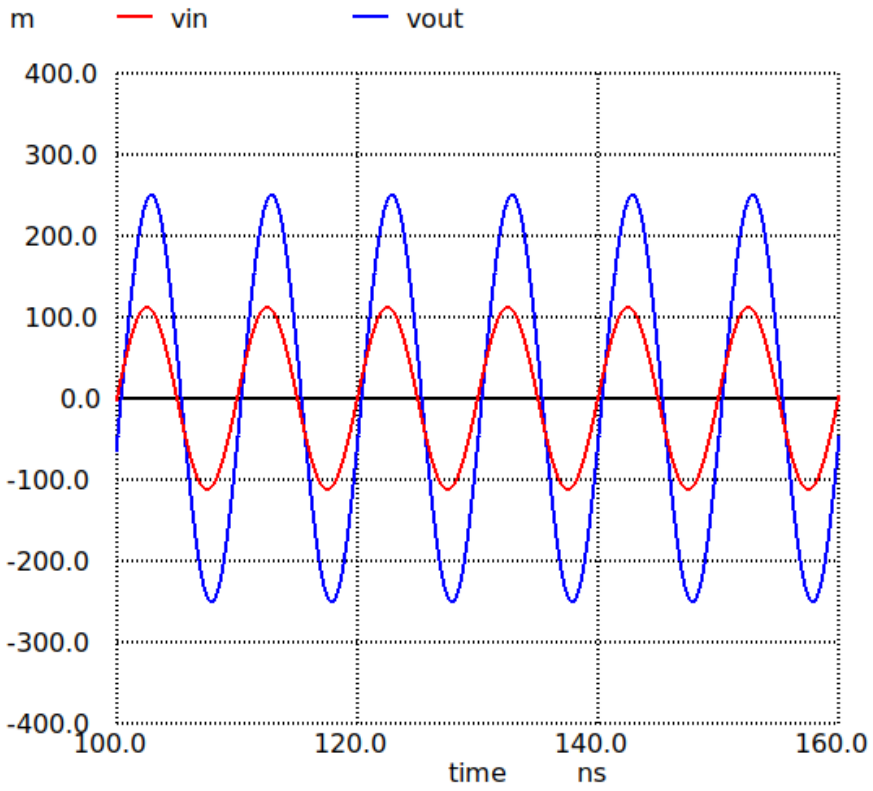
Spec	Target	Slow	Typical	Fast
Close loop bandwidth ($f_{c\text{-}3dB}$)	≥500 MHz	To do	796 MHz	To do
Close loop gain (A_{vCL})	7 ± 0.1 dB	To do	6.98 dB	To do

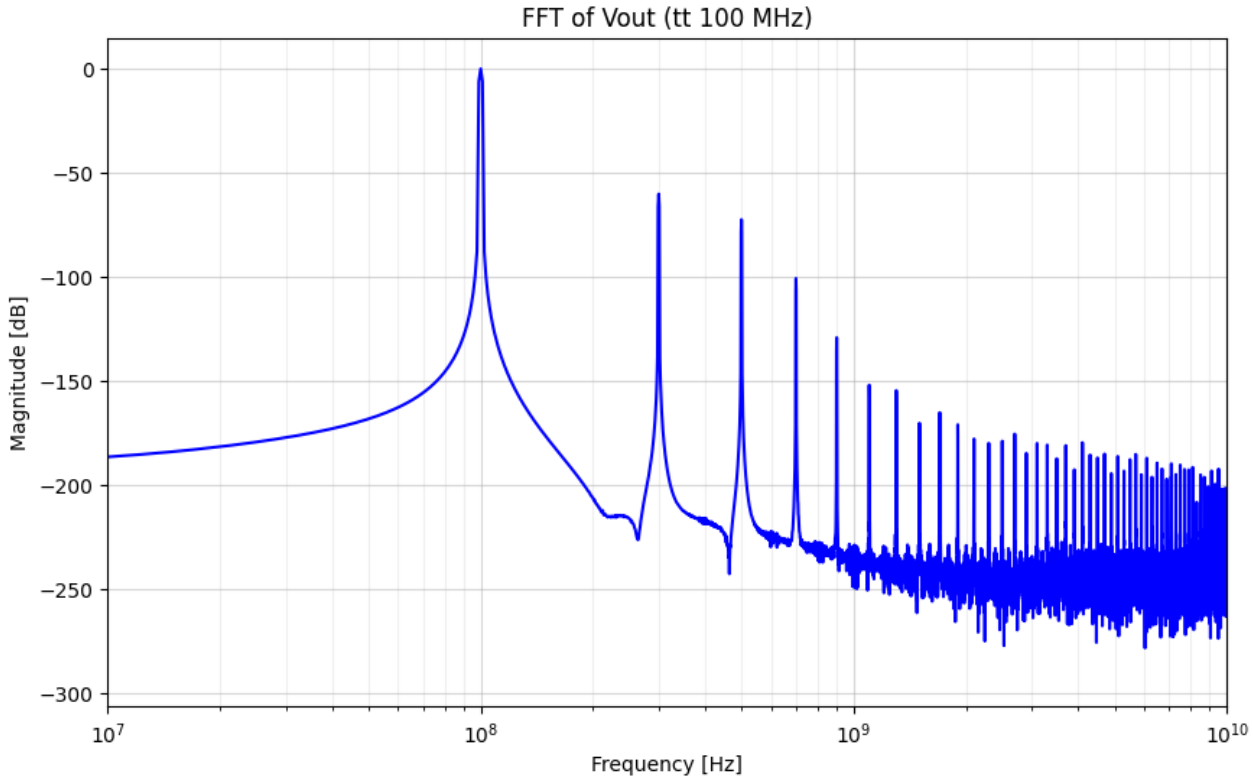




Measurements Close Loop HPA

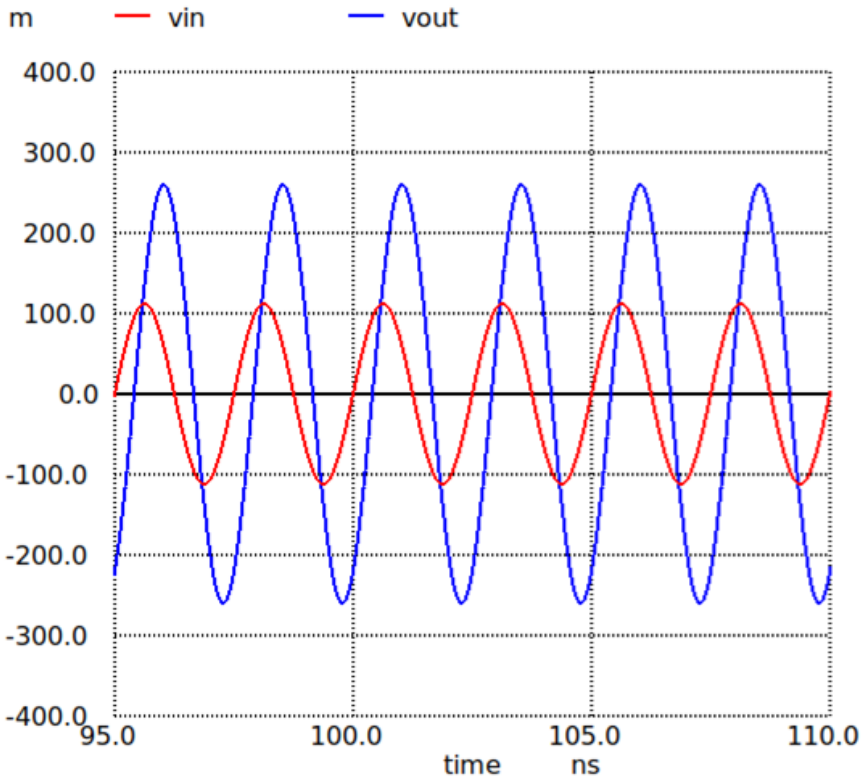
Spec	Target	Slow	Typical	Fast
SNDR @ 100 MHz	≥ 55.94 dB	To do	60.11 dB	To do
ENOB @ 100 MHz	≥ 9 bits	To do	9.69 bits	To do

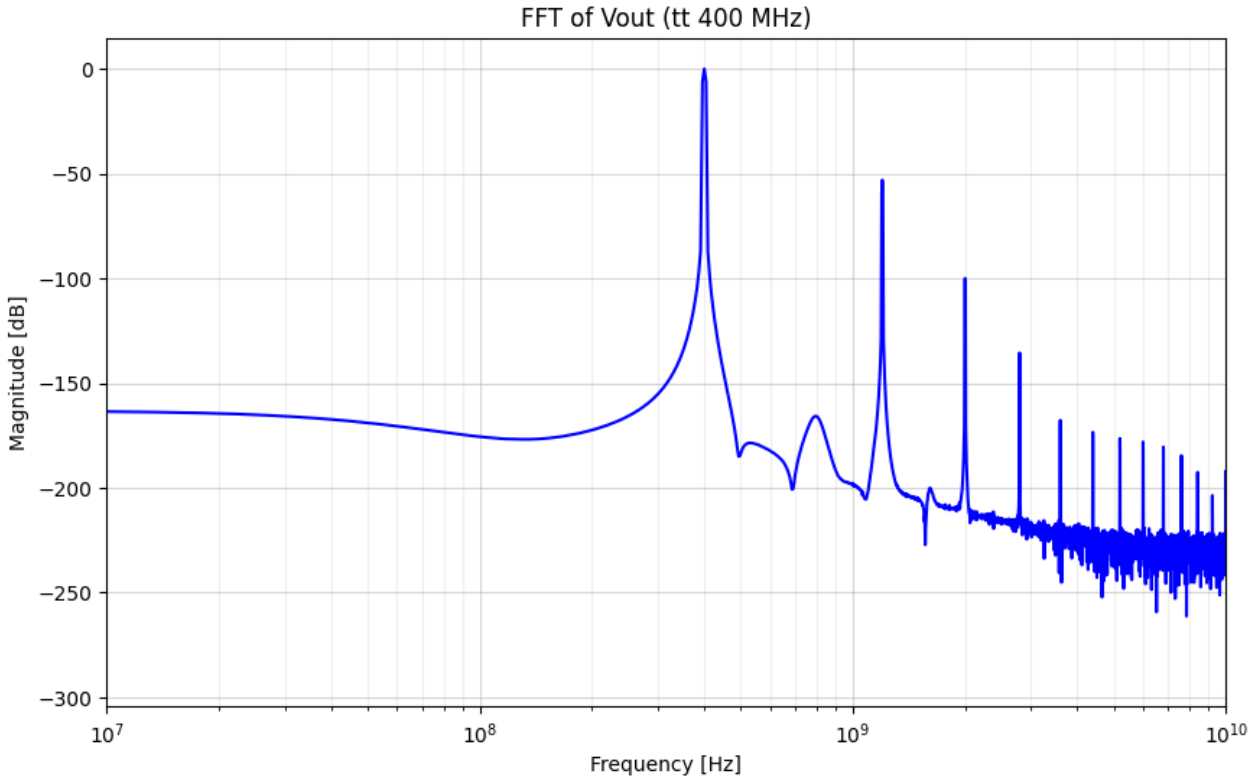




Measurements Close Loop HPA

Spec	Target	Slow	Typical	Fast
SNDR @ 400 MHz	≥ 46.91 dB	To do	53.09 dB	To do
ENOB @ 400 MHz	≥ 7.5 bits	To do	8.53 bits	To do





References

- [1] F. Tolosa, E. Dri, Á. F. Bocco and B. T. Reyes, "High Performance Amplifier in 130nm CMOS Technology using an Open Source Design Flow for 10Gbase-T Ethernet Transceivers," 2023 Argentine Conference on Electronics (CAE), Cordoba, Argentina, 2023, pp. 75-80, doi: 10.1109/CAE56623.2023.10087008.
- [2] B. Razavi, Design Of Analog Cmos Integrated Circuit , 2Nd Edition, Mc Graw Hill India, 2017
- [3] P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design, 3rd ed. New York, NY: Oxford University Press, 2011.

Thank you!!!

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