UNIC-CASS Project

Quadrature Delay Locked Loop

Project Details

Martín Doric - Argentina section

Leonardo Vazquez - Argentina section

Fundación FULGOR

CAS IEEE CIRCUITS AND SYSTEMS SOCIETY

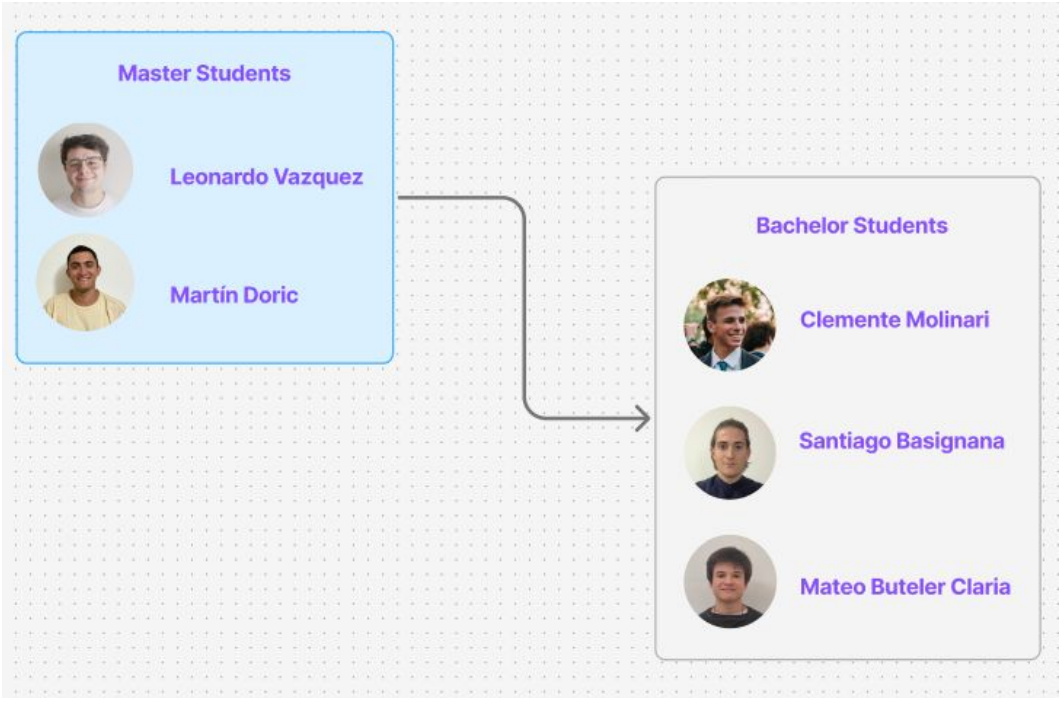
Project Design

- Design Title:
  - Quadrature Delay Locked Loop for 500 MHz Clock-Data-Recovery
- Design Acronym:
  - QDLL

Team Composition

IEEE CIRCUITS AND SYSTEMS SOCIETY

	First Name	Middle Nam	Last Name	Email	IEEE Membership Number	University Name	Expected Graduation Date (*1)
Member 1	Leonardo	David	Vazquez	vazquezleonardodavid@outlook.com	98930480	Universidad Nacional del Sur - Argentina	2026/12 - Master degree - Microelectronics
Member 2	Martín	Ivan	Doric	martin.doric97@gmail.com	101333183	Universidad Nacional del Sur - Argentina	2026/12 - Master degree - Microelectronics
Member 3	Mateo	José	Buteler	mateojosebuteler@gmail.com	101320612	Universidad Nacional de Córdoba - Argentina	2030/12 - Bachelor degree - electronic engineering
Member 4	Santiago		Basignana	basignana.santiago@gmail.com	101322282	versidad Tecnológica Nacional - Córdoba Argent	2027/12 - Bachelor degree - electronic engineering
Member 5	Clemente		Molinari		101322327	versidad Tecnológica Nacional - Córdoba Argent	2027/12 - Bachelor degree - electronic engineering
Mentor 1	Agustín	Carlos	Galetto	agaletto@fundacionfulgor.org.ar	95581281	Universidad Nacional del Sur - Argentina	2025 - Doctor of Philosophy



Design Details

Description of the idea:

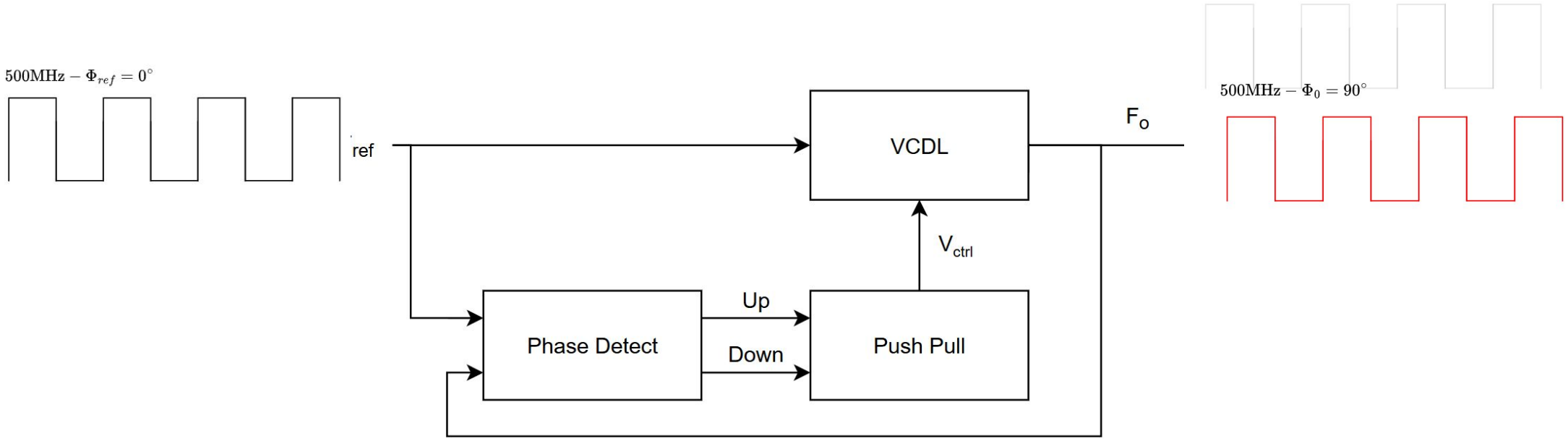
This project presents the design of a **Quadrature-Delay-Locked Loop (QDLL)** in CMOS technology, targeting the generation of a clock signal with a **fixed 90° phase shift** relative to a 500 MHz input reference. Such quadrature clock generation is essential in systems such as IQ modulators/demodulators, frequency synthesizers, and time-interleaved ADCs.

The architecture includes three key blocks:

- **Voltage-Controlled Delay Line (VCDL, Mixed-Signal):** already designed and implemented. It dynamically adjusts the propagation delay so that the output clock achieves a stable quarter-period (90°) displacement. The design was verified at the schematic level.
- **Phase Detector (Digital):** currently under development. Its role is to compare the reference and the delayed clock, generating *Up* and *Down* signals that indicate whether the output leads or lags the desired 90° phase shift.
- **Charge Pump (Analog):** also in progress. It will convert the digital Up/Down signals into a continuous control voltage that tunes the VCDL. Special care is being taken to minimize mismatch and noise contributions.

Unlike PLL-based solutions, the QDLL locks directly to the reference clock, avoiding frequency drift and ensuring that the 90° phase relation remains stable. With the VCDL completed and the other blocks in development, this design forms a compact and scalable solution for quadrature clock generation in mixed-signal integrated systems.

Block Diagram



Design Details

- ## Expected Outcome

The expected outcome of this project is a CMOS Delay-Locked Loop (DLL) capable of generating a stable **90° phase-shifted clock signal** with respect to the reference input. The design is expected to:

- Demonstrate **robust locking behavior** across process, voltage, and temperature (PVT) variations.
- Achieve **low jitter and stable quadrature phase relation** suitable for high-speed communication and signal processing systems.
- Provide a **validated VCDL block**, with the Phase Detector and Charge Pump under development, leading to a complete integrated DLL solution.

Design Details

- Number of Pins
  - VDD+VSS: Bi-direcctional
  - PD: 2 inputs
  - Charge pump: 1 output
  - VCDL: Vout 1 output + Vcontrol: 1 input
- Design type: Analog

Design Type:* *

Analog

Estimated Number of Pins:*

Input: *

3

Output: *

2

Bidirectional: *

2

ihp 130 nm

UNIC-CASS Project

Quadrature Delay Locked Loop

Technical Details

Martín Doric - Argentina section

Leonardo Vazquez - argentina section

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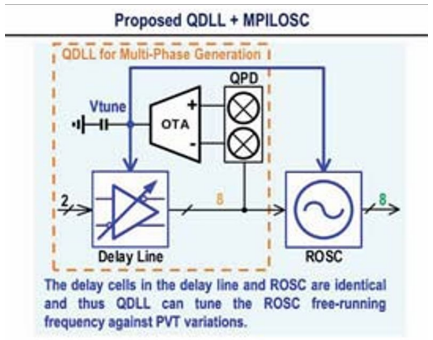
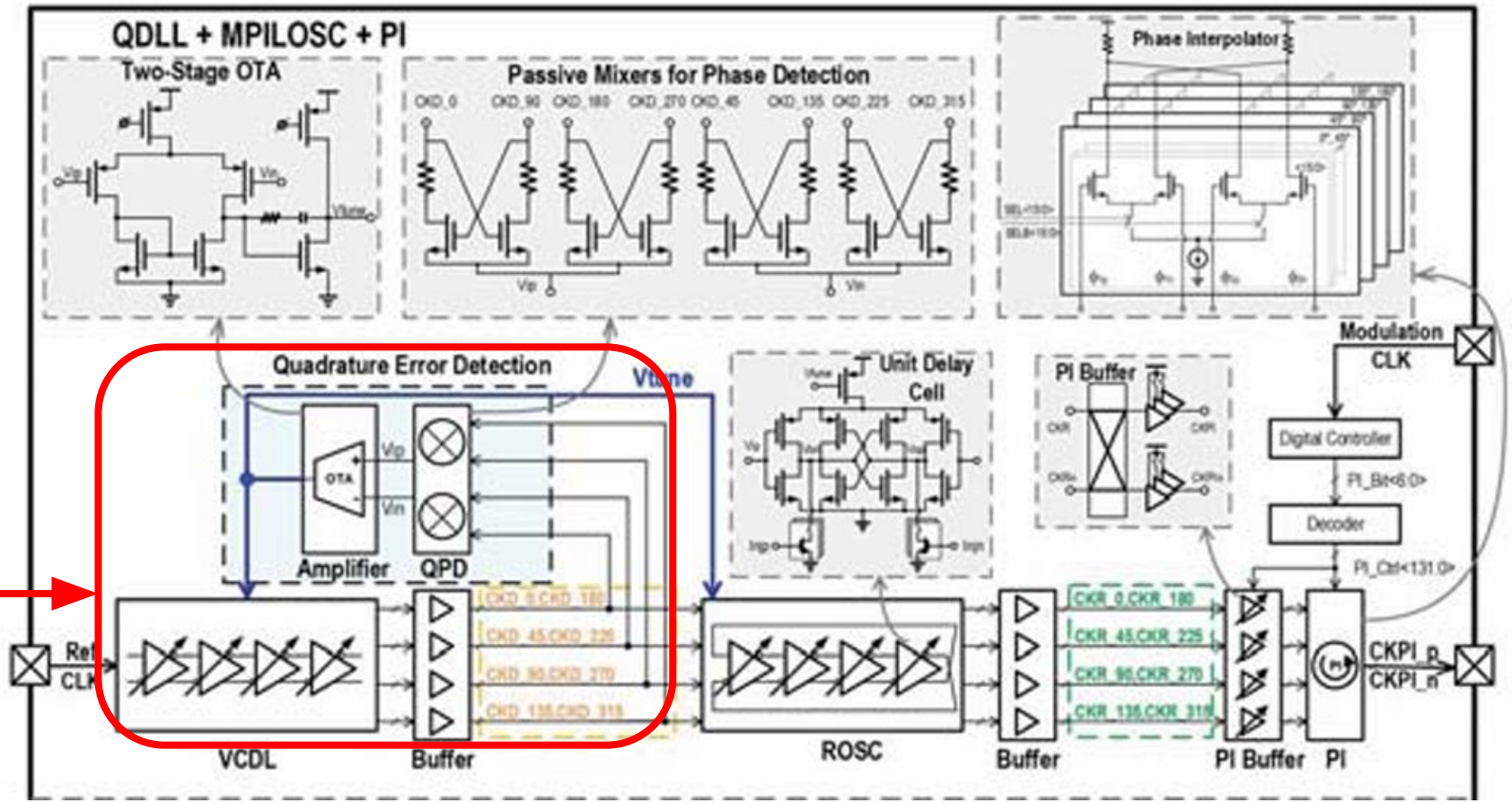
WorkFlow

- Analog Design (This work)
  - State of the art ✅
  - Schematics levels design (XSCHEM) ✅
  - Simulation & W/L iteration (NGSPICE) in progress
- Layout Design (Future Work)
  - Layout implementation (KLayout)
  - DRC + LVS Verification

Multiphase Clock Generator: CDR for 7 GHz



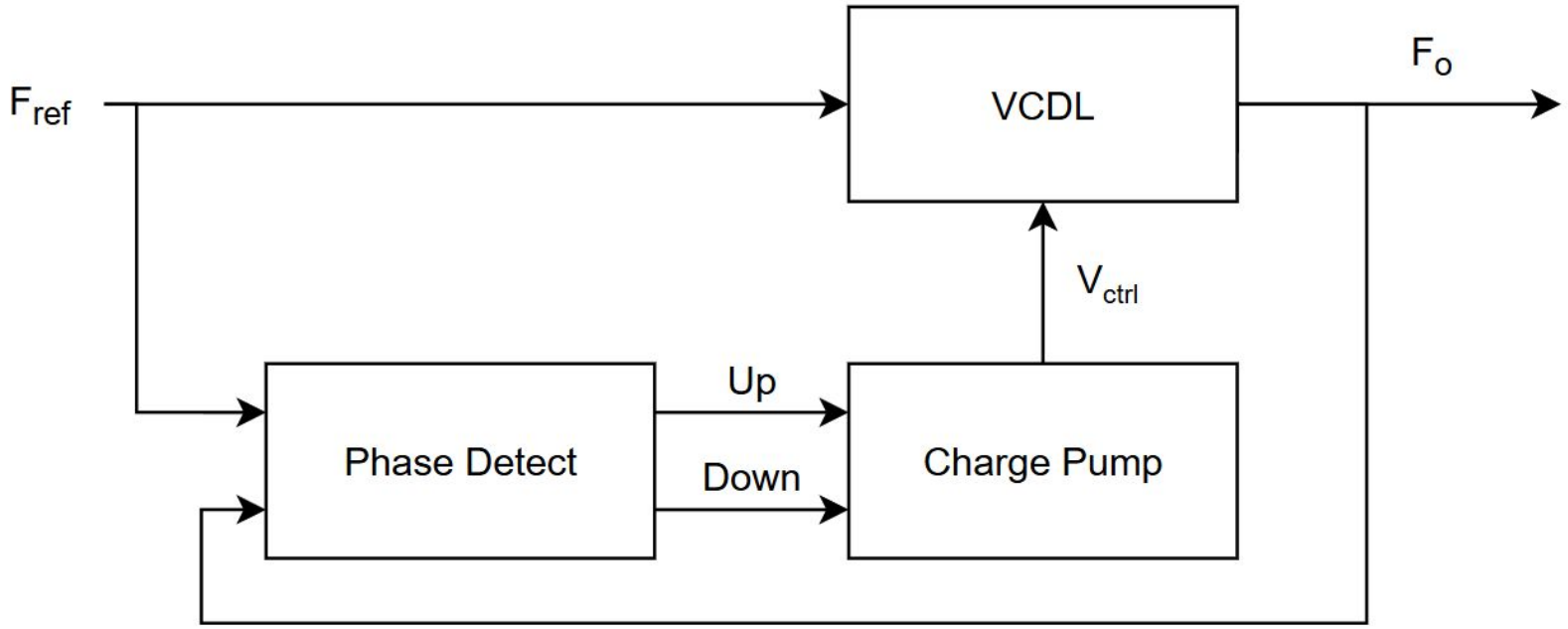
DLL!!!!



Source: A highAccuracy Multi-Phase Injection-Locked 8-Phase 7GHz Clock Generator in 65nm with 7bits Phase Interpolators for High-Speed Data Links

Proposed DLL

- Block Diagram

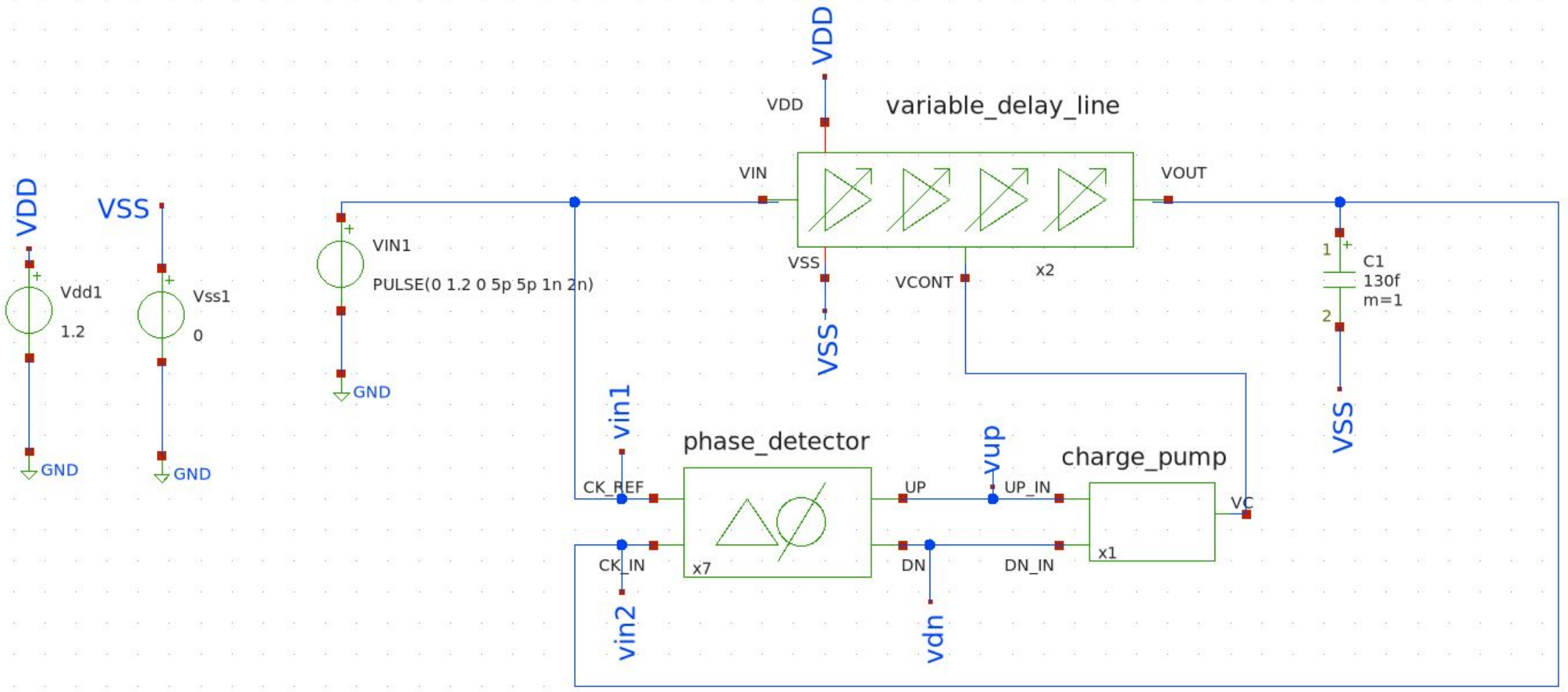


Proposed DLL

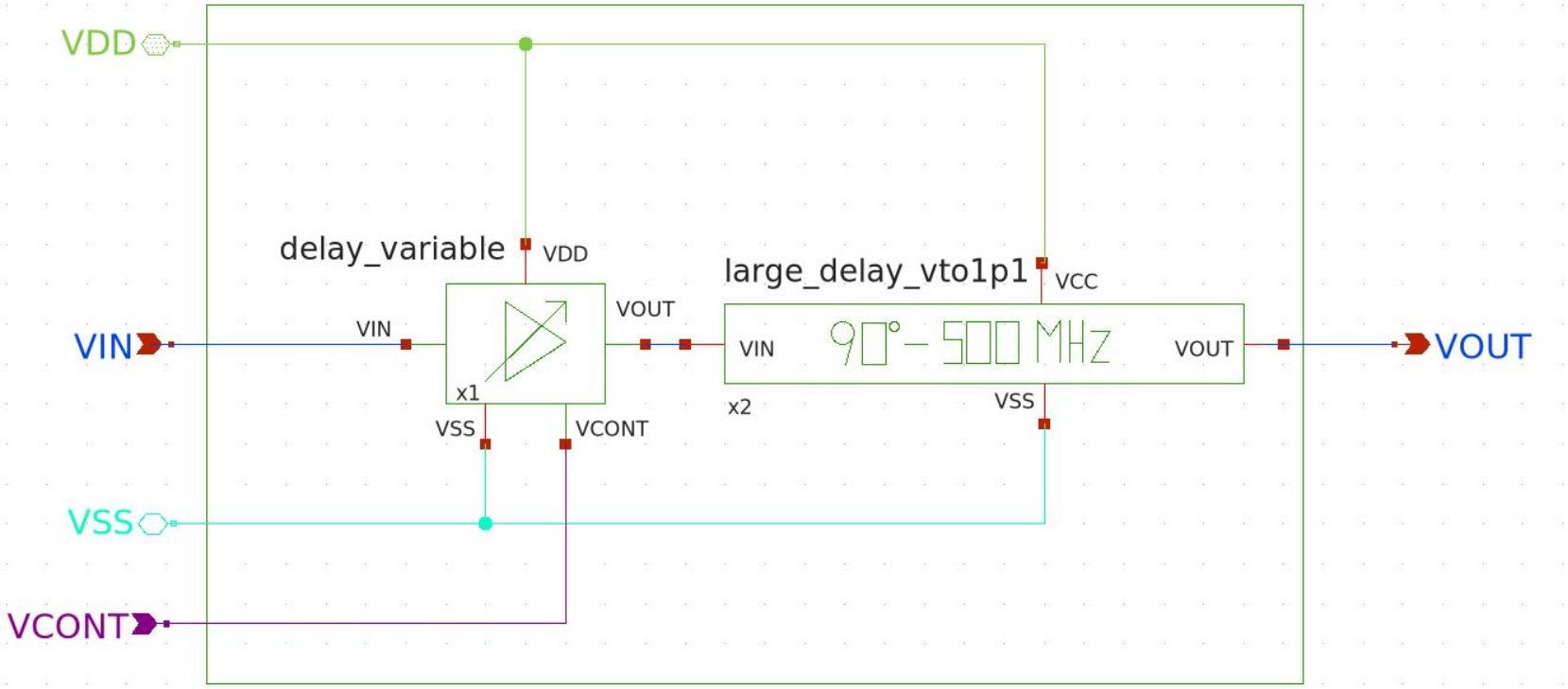
- Main Expected Characteristics

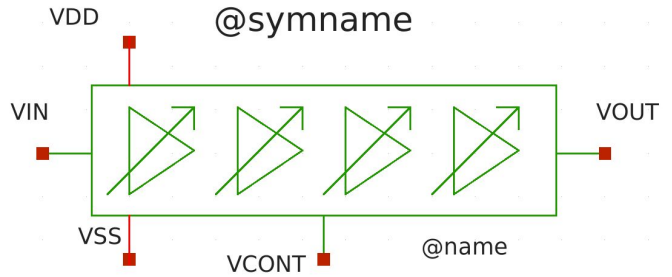
	Value	Unit
Tech.	130	nm
Supply Voltage	1.2 ± 10 %	V
Temperature	[0, 65, 125]	°C
Vcont	[0 , 1.2]	V
Vinput/ Voutput	[0 - 1.2] (rail-to-rail)	V
t_rise/t_fall	< 0.25	ps
Phase shift	90 ± 5	degrees
Frequency	500±10	MHz
Period	2	ns
Charge	80-150	fF

Proposed DLL: Top Level

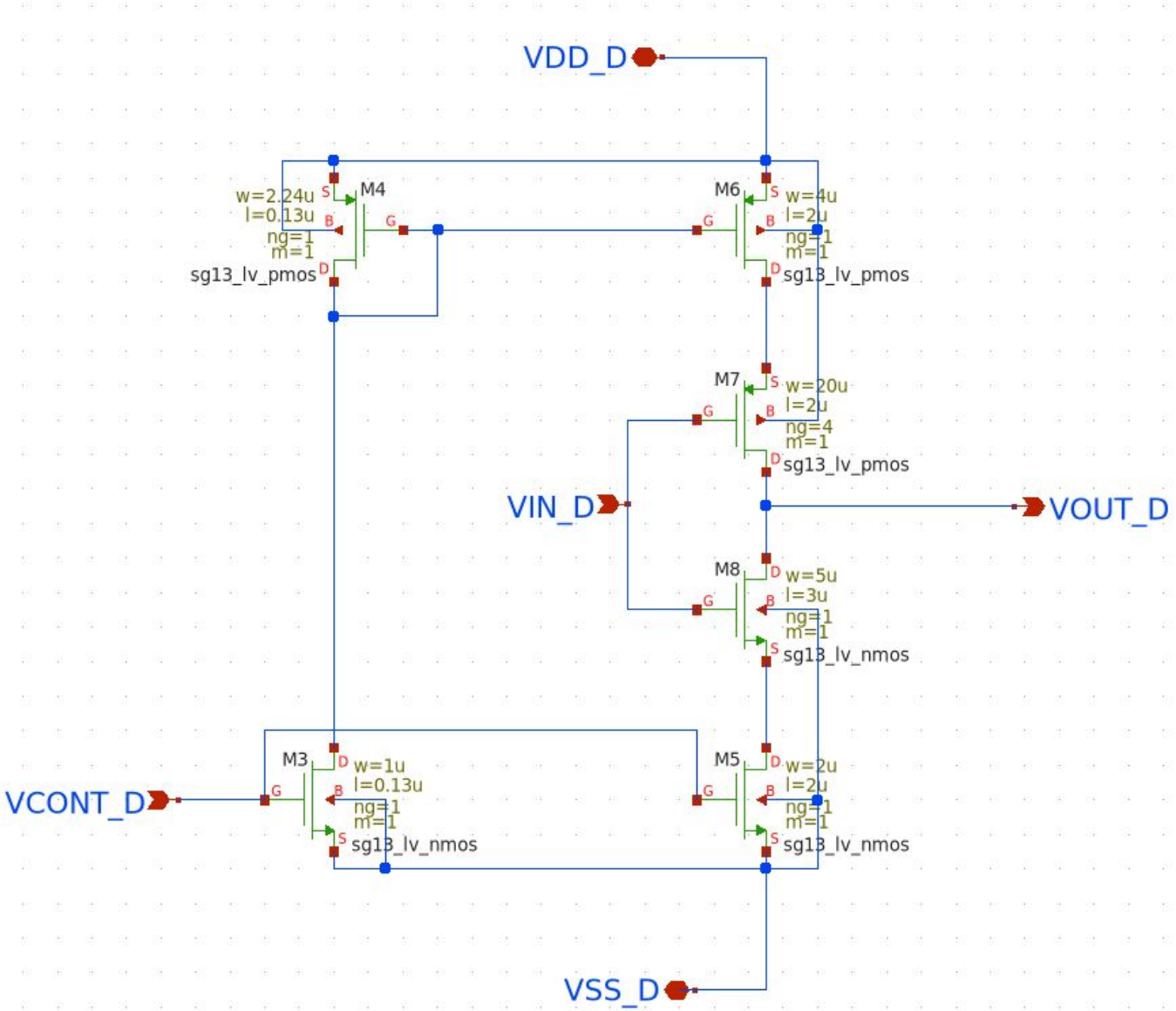


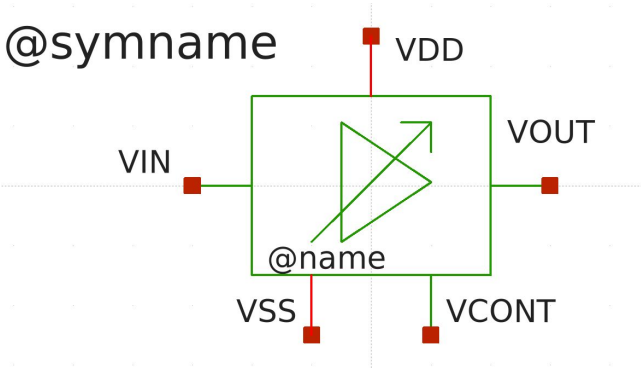
Schematics: Variable Delay Line



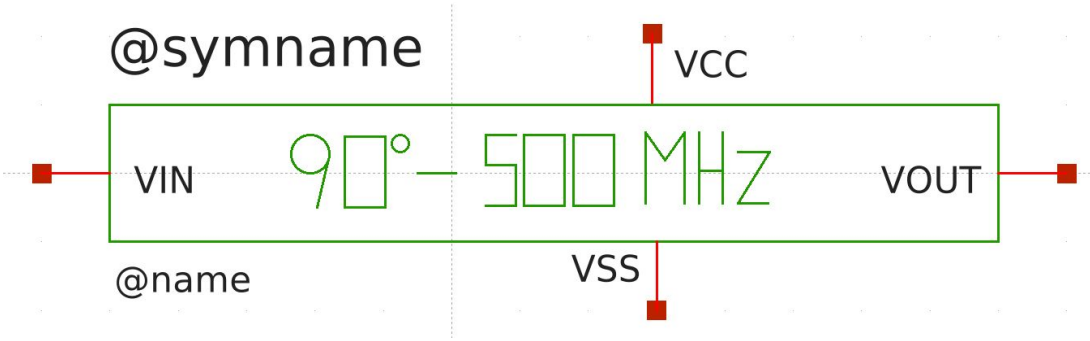


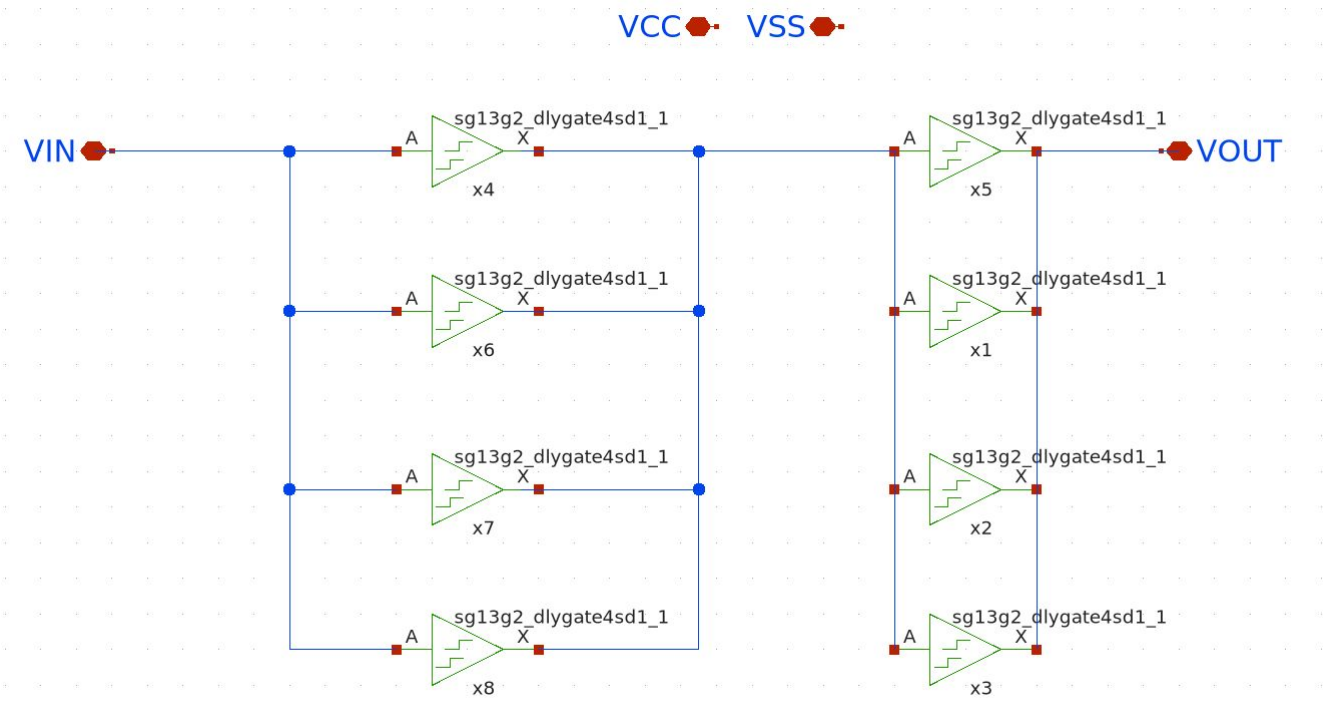
Schematic: Variable Delay



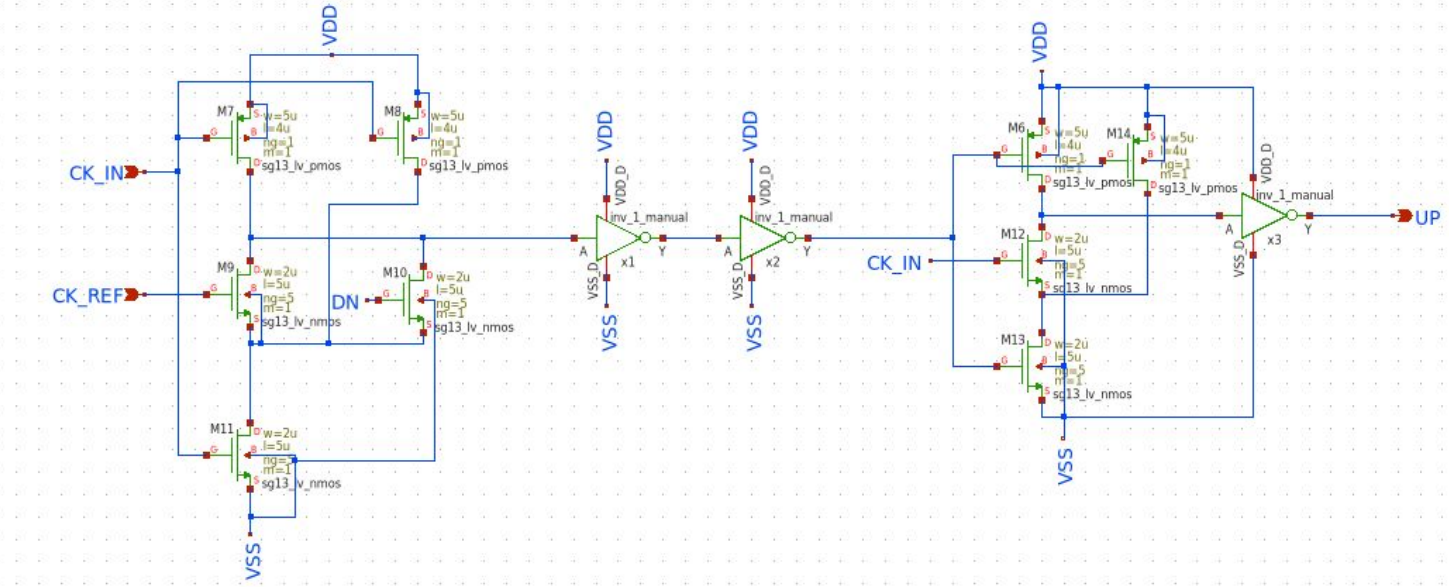


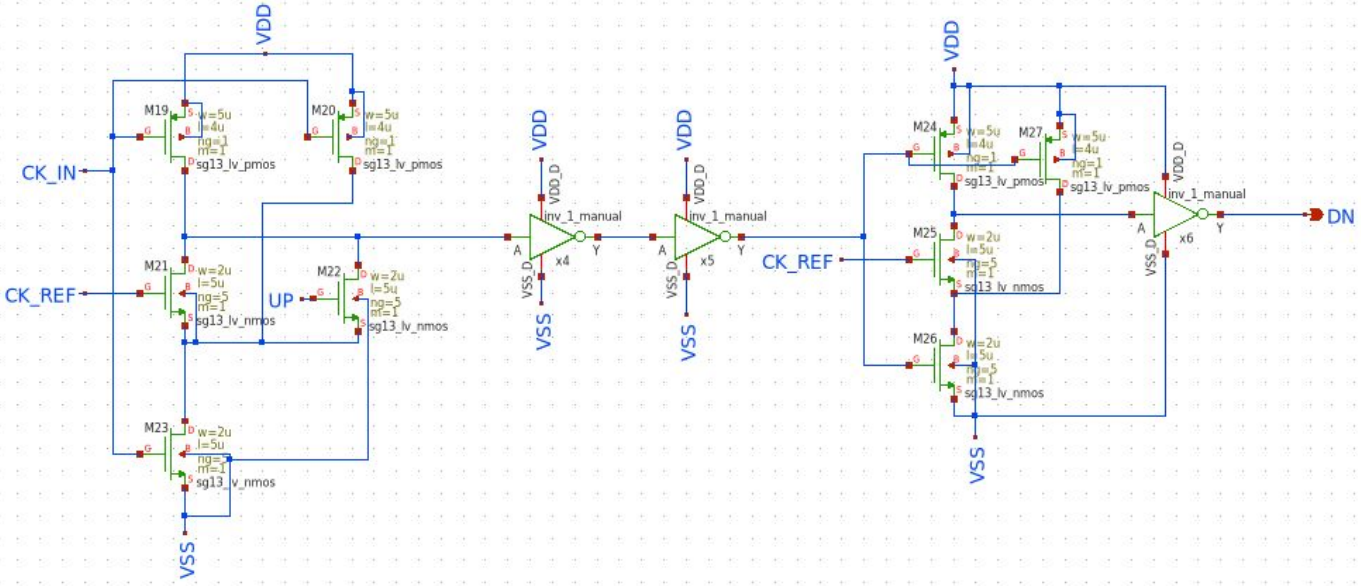
Schematic: Large Delay

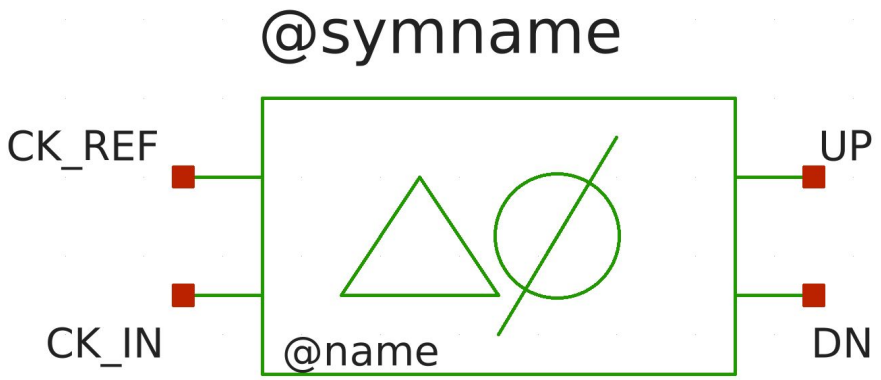




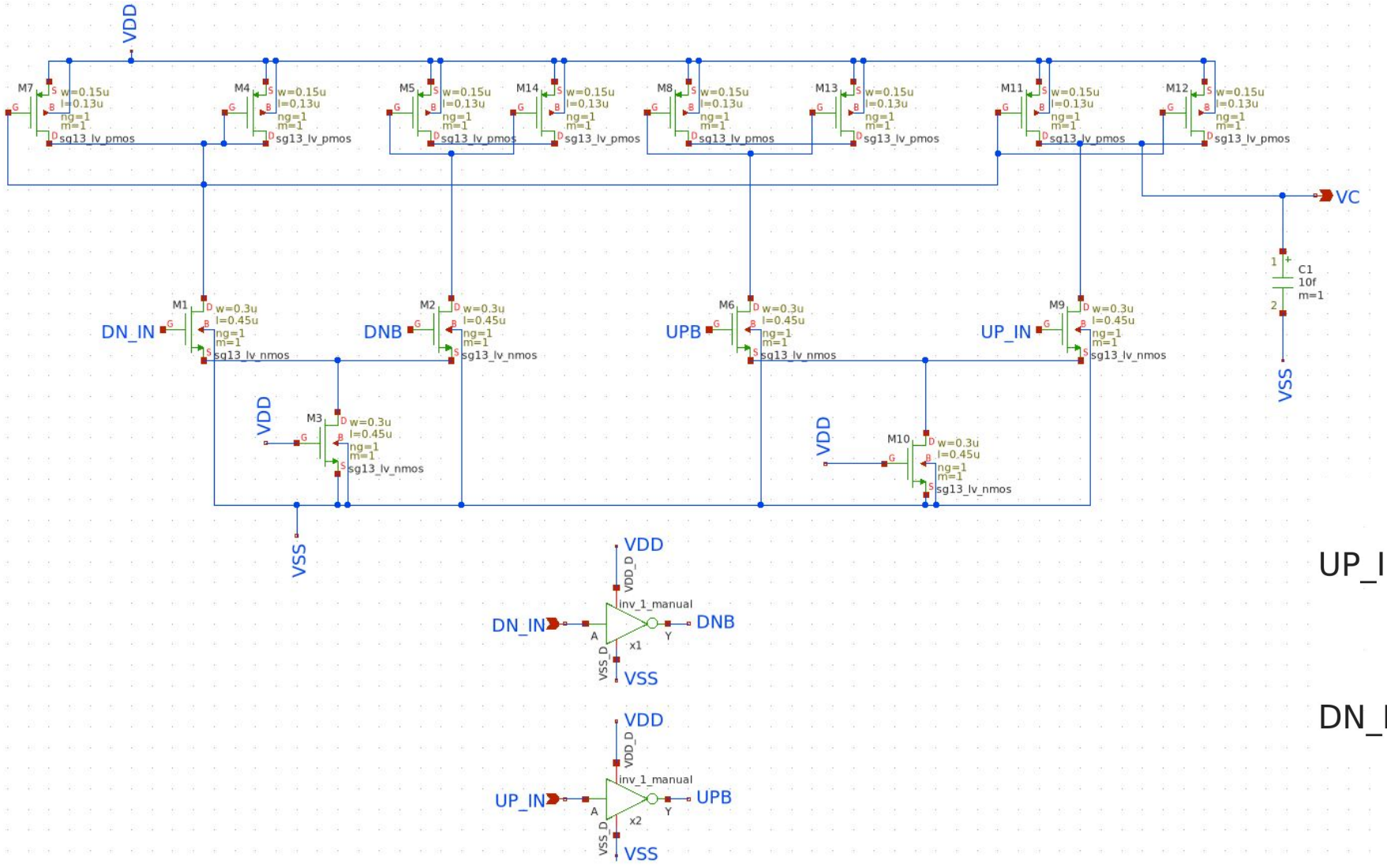
Schematic: Phase Detector

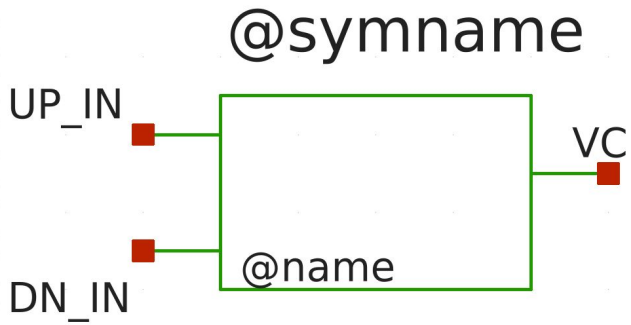






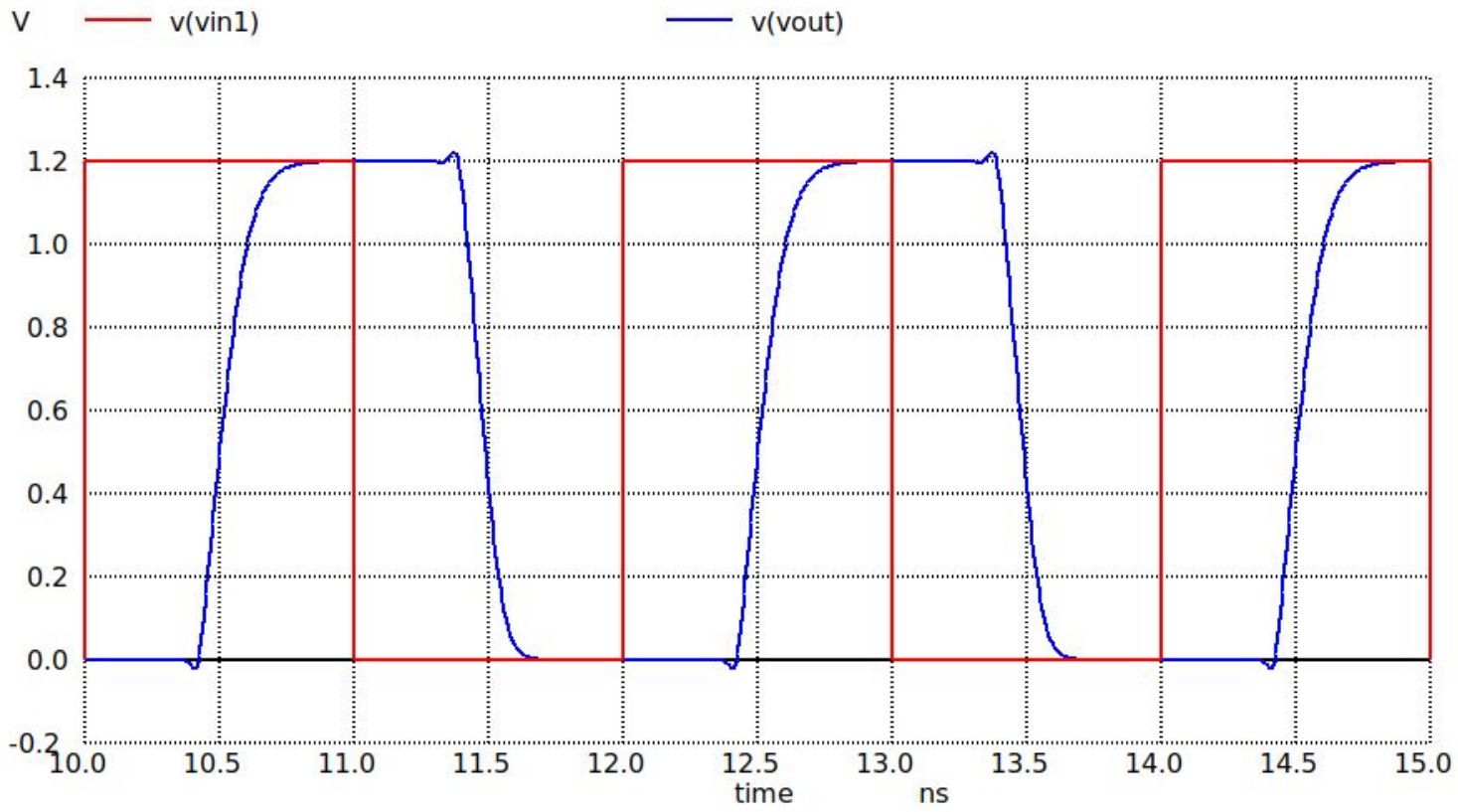
Schematic: Charge - pump





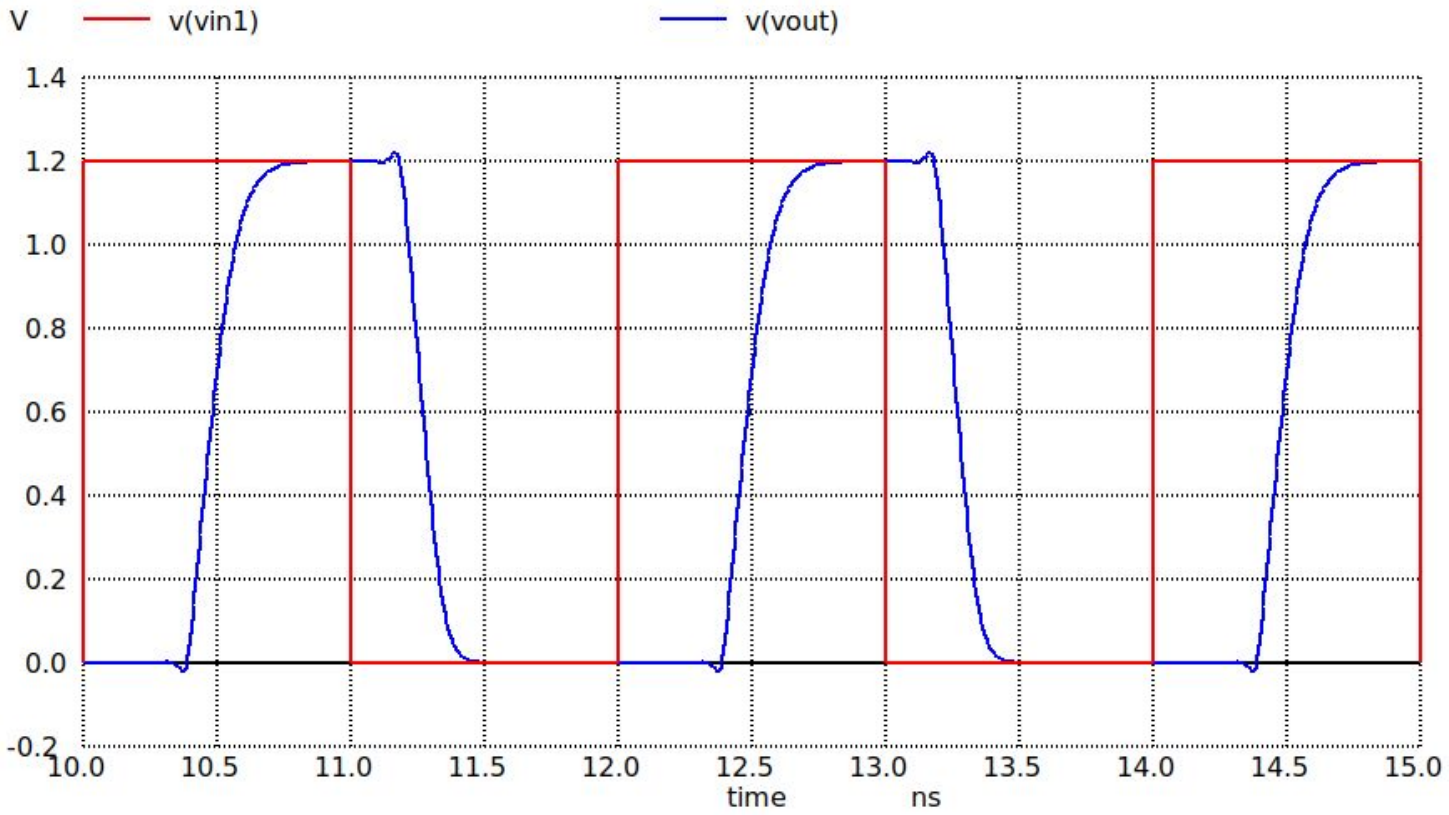
Simulations: open loop VCDL

- VControl = 0 V
- Phase Shift = 94°



Simulations: open loop VCDL

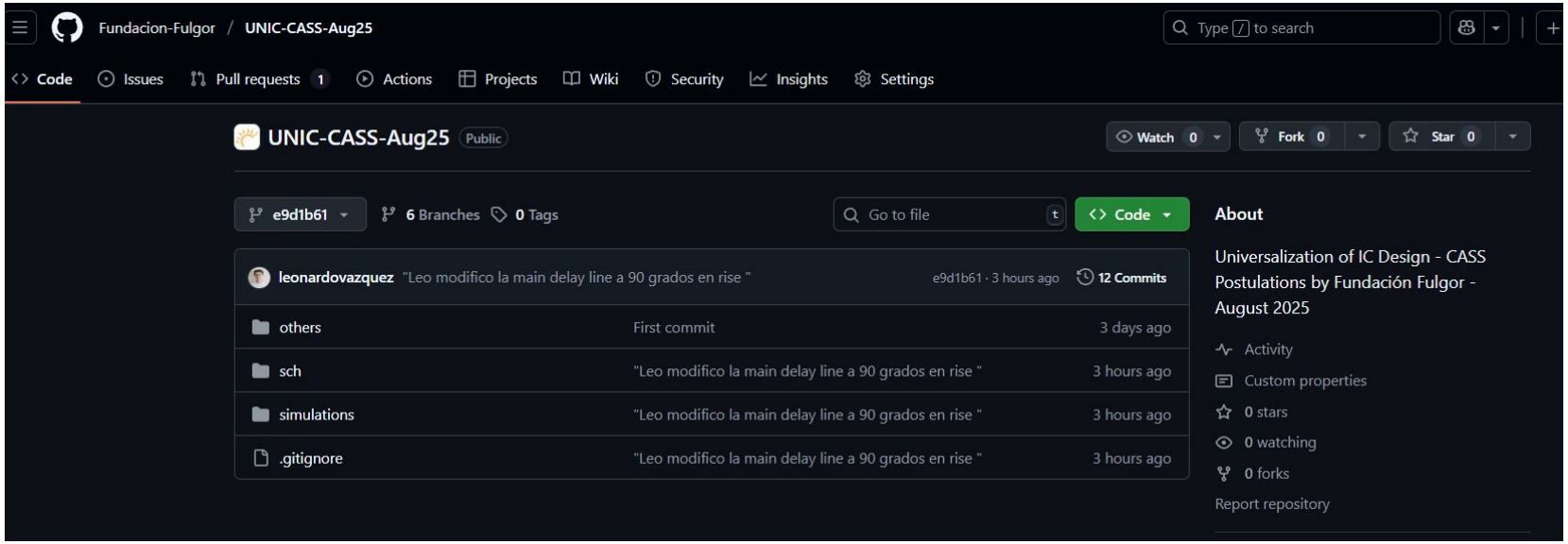
- VControl = 1.2 V
- Phase Shift = 86°



Simulations: closed-loop

You can view the progress in the Repo project

[Fundacion-Fulgor/UNIC-CASS-Aug25 at e9d1b61a308cbfd85f680fc90a6ecec01b0072fd]



The project is open-sourced and publicly available through GitHub for non-profit organizations, realeased under a GNU GPL 3.0 license