ELECTRICAL ENGINEERING 360
PHYSICAL ELECTRONICS
FALL 2019

PROJECT #3

DUE: Friday, December 6, 2019 by 11:59:59PM EST (Just Before Midnight)

(Points: 7.5% of Final Class Grade)

Statement of Problem: the Audio Amplifier

In the context of this assignment, your team (consisting of no more than three students) will design an audio amplifier capable of supplying 30 mW of power to a 32 Ω load corresponding to a *Listen Technologies Corp.* model LA-163 Single Ear Bud (see specification sheet uploaded to Springboard). Figure 1 shows the topology of the amplifier that you will use broken down into five stages. The signal generator output resistance is taken to be $R_{sig} = 50\ \Omega$. The first stage is a simple voltage divider that will be used for controlling the *volume* of the audio signal. Since physically one would realize this stage using a potentiometer, the sum of the two resistances should equal a chosen value of R, i.e. $(R - \Delta R) + \Delta R = R$. The second stage should ideally be an amplifier that offers significant gain and has a sufficiently large input resistance. Such criteria are met using a common emitter amplifier with an emitter resistance. In order to benefit from the enhanced DC input resistance, offered by adding resistor R_{E1}, while allowing for adjustable small-signal voltage gain, we have shunted R_{E1} with a DC blocking capacitor (DCB) connected in series with a relatively small resistor R_1. The third and fourth stages of the audio amplifier consist of PNP and NPN emitter followers, respectively, which will serve as a buffer for driving the low-impedance earphone load $R_L = 32\ \Omega$. The PNP stage is included to reduce the drive requirements and to cancel the V_{BE} offset produced by the NPN stage.

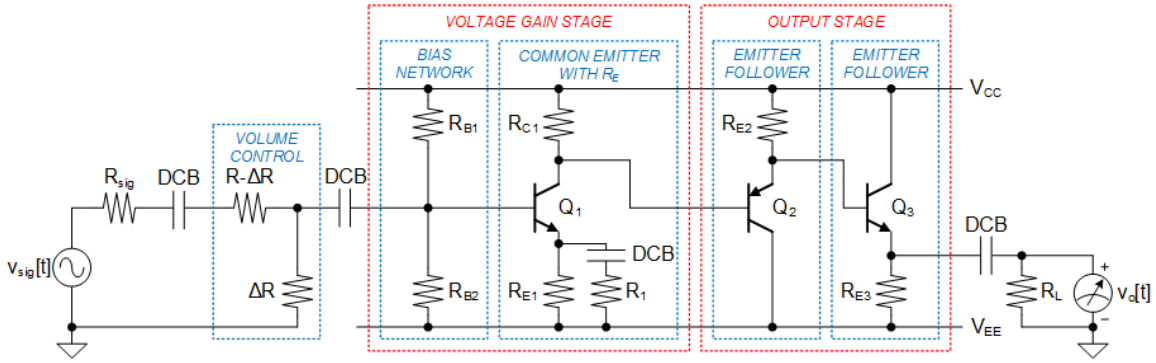

Figure 1. Audio amplifier consisting of five stages: (i) volume control, (ii) bias network, (iii) NPN common emitter amplifier with an emitter resistance, (iv) PNP emitter follower amplifier, and (v) NPN emitter follower amplifier.

Criteria for grading your project will include: 1) completion of the project, 2) accuracy of reported figures-of-merit, 3) compliance of figures-of-merit with design requirements, and 4) the overall quality of the written report. Use the template entitled, "Preparation of Papers for IEEE TRANSACTIONS and JOURNALS (February 2017)," which has been uploaded to the Brightspace.

Table I lists the relevant input parameters, which are given as design constraints.

Table I. Design constraints (input parameters).

Design Constraint	Symbol	Nominal Value
Operating Temperature	T	300 K
Top-Rail DC Supply Voltage	V_{CC}	+6 V
Bottom-Rail DC Supply Voltage	V_{EE}	−6 V
Audio Signal Frequency	f_m	261.626 Hz
Signal Generator Output Resistance	R_{sig}	50 Ω
Load Resistance	R_L	32 Ω

Your design must rely on the use of real transistor models – not ideal transistor models. Any resistance or capacitance values you use may only be specified with three-significant digits or less. For example, using resistors with resistance values of 0.152 Ω or 1.37 kΩ would be acceptable whereas using resistance values of 0.1523 Ω or 1.374 kΩ would not be acceptable.

To complete Table II, you must find the maximum collector or drain current for each transistor used in your circuit and compare these values to the amounts of quiescent and transient current that actually flow through the devices in your circuit. The current rating can be obtained from a specification sheet or by *right-mouse clicking* on the transistor symbol, selecting "Pick New Transistor" and finding the value labeled "Ic[mA]." Points will be deducted for designs with transistors that experience currents that exceed their rating specifications – in reality, exceeding the current specification would cause the transistors to *burn up*. The simulated quiescent collector current value is determined when the input signal is set to $v_{sig} = 0$. The simulated maximum transient collector current value is determined when the input signal is set to $v_{sig} = v_{sig,1\text{dB}}$ (see description of 1-dB output compression point).

Table II. Absolute maximum transistor ratings for final design of audio amplifier.

Collector Current	Data Sheet Rating (mA)	Simulated Quiescent Value (mA)	Simulated Maximum Transient Value (mA)
Q1			
Q2			
Q3			

The design requirements for the performance figures-of-merit are listed in Table III. Ensure that your simulated values comply with the requirements.

Table III. Performance figures-of-merit (output parameters) for final design of audio amplifier.

	Symbol	Requirement	Sim. Value	Unit
Quiescent Power Supply Current	I_Q	≤ 200		mA
Small-Signal Voltage Gain Deviation	GD	≤ 0.1		dB
1-dB Output Compression Point	${v^2}_{\text{1dB}}$	≥ 56.8		dBmV RMS

Quiescent Power Supply Current:

The maximum quiescent current consumption will be defined as the current that leaves the DC power supplies when the input signal is equal to zero. This parameter will be defined as:

$$I_Q \equiv |I_{CC}|_{v_{sig}=0} = |I_{EE}|_{v_{sig}=0}$$

where I_{CC} and I_{EE} represent the quiescent current leaving the top and bottom voltage rails, respectively.

Small-Signal Voltage Gain Deviation:

The overall small-signal voltage gain will be defined as:

$$G_v[v_{sig}] \equiv (20\text{ dB})\ \log_{10}\left|\frac{v_o}{v_{sig}}\right|.$$

You should design an amplifier that provides 20 dB of gain in the limit $v_{sig} \to 0$. The parameter for quantifying gain deviation will be defined at the relatively small input voltage amplitude of $v_{sig} = 0.1$ mV as follows:

$$GD \equiv \left|20\text{ dB} - G_v[v_{sig} = 2.828\text{ mV}]\{\text{dB}\}\right|.$$

Your design requirement is achieve $GD \leq 0.1$ dB, but ideally you would want a value of GD that is as close to 0 dB as possible. The requirement for keeping resistor values to only three-significant digits of accuracy will present a challenge for minimizing GD.

1-dB Output Compression Point ${v^2}_{\text{1dB}}$:

In accordance with the transfer function shown in Fig. 3, the parameter ${v^2}_{\text{1dB}}$ will be defined in terms of the output voltage squared that deviates from an extrapolated linear response by an amount of 1 dB. This parameter will be measured in units of dBmV according to the relation:

$${v^2}_{\text{1dB}}\{\text{dBmV}\} = 20\log_{10}\left|\frac{v_{\text{1dB}}\ \{\text{mV RMS}\}}{1\text{ mV RMS}}\right|.$$

From the logarithmic plot of Fig. 3, it is also possible to extract the parameter G_v, which is equal to the offset of the straight line of unity slope.

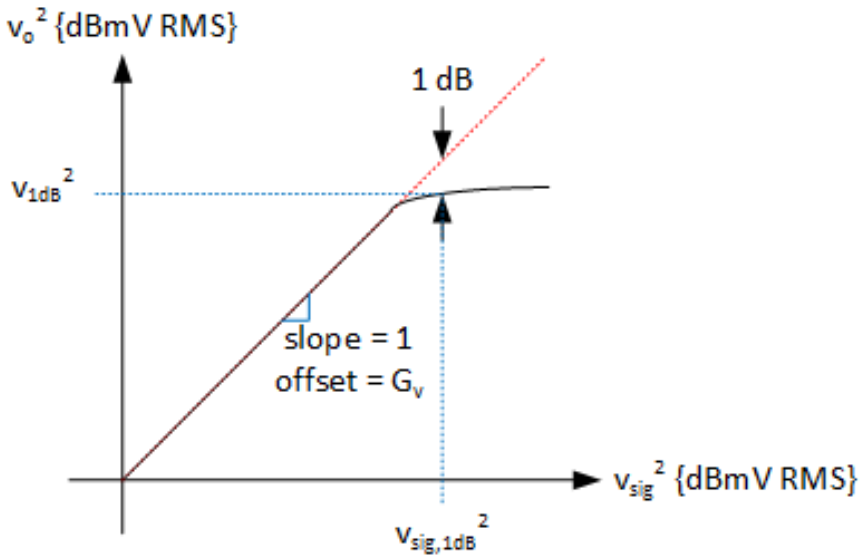

Fig. 3. Transfer function that will be used to determine ${v^2}_{1\text{dB}}\{\text{dBmV}\}$ as well as $G_v\{\text{dB}\}$.

Your design requirement is achieve $GD \leq 0.1$ dB, but ideally you would want a value of GD that is as close to 0 dB as possible. The requirement for keeping resistor values to only three-significant digits of accuracy will present a challenge for minimizing GD.

To simulate the 1-dB compression point using LTSpice, it is beneficial to plot decibel gain ($G_v = 20\log|v_o/v_{sig}|$ dB) as a function v_{sig}. Let the parameter $v_{sig,1\text{dB}}$ be defined at the point where the overall voltage gain differs from its small-signal limit by 1 dB, in accordance with the relation:

$$\left|G_v\left[v_{sig}^2 \approx 6.021 \text{ dBmV RMS}\right]\{\text{dB}\} - G_v\left[v_{sig,1\text{dB}}^2\right]\{\text{dB}\}\right| = 1 \text{ dB}.$$

Recall that $v_{sig}^2 \approx 6.021$ dBmV RMS corresponds to $v_{sig} = 2$ mV RMS ≈ 2.828 mV peak. By inspection of a G_v versus v_{sig}^2 plot, $v_{sig,1\text{dB}}^2$ can be determined. Fig. 4 is a piecewise depiction of what such a plot should look like.

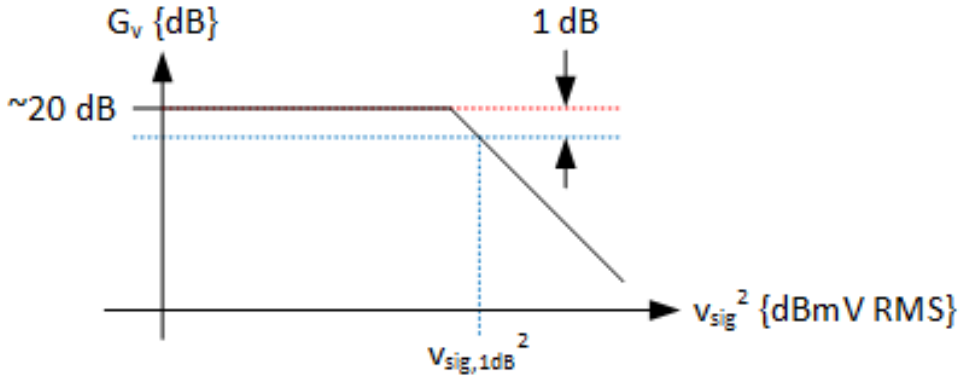

Fig. 4. Gain compression plot.

The output 1-dB compression point is the value of v_o^2 that corresponds to the value of $v_{sig,1\text{dB}}^2$ such that: $v_{1\text{dB}}^2 = v_o^2\left[v_{sig,1\text{dB}}^2\right]$.

Grading

You are required to upload two and only two files (the **AudioAmplifier.ASC** simulation file and your **final report in PDF format**) to the Brightspace in a repository found under the path *Assessments → Assignments → Submission Folder → Project 3 Repository* no later than the specified deadline.

Your Project 3 submission will be graded in accordance with the following scoring key.

Simulated Design (40% of Grade):

1. AudioAmplifier.ASC Simulation File: subtract 40% for a missing simulation file or a simulation file that does not correspond to the design described in the written report.

2. Absolute Maximum Transistor Ratings: subtract 25% from final project grade if the collector current of any one of the transistors exceeds the maximum data-sheet rating.

3. Quiescent Power Supply Current: subtract 0.25% from final project grade for every 1 mA in excess of maximum allowable quiescent current consumption

4. Small-Signal Voltage Gain Deviation: subtract 2% from final project grade for every 0.1 dB in excess of the allowable gain deviation tolerance

5. 1-dB Input Dynamic Range: subtract 1% from final project grade for every 5 mV below minimum allowable input dynamic range

Written report (60% of Grade):

Expect a deduction of up to 15% per section from the final project grade for inadequate presentation of any of the four report sections (1. Abstract, 2. Introduction, 3. Design Description, 4. Summary). *Inadequate* will be subjectively defined at the instruction's discretion; so, do your best to impress the reader.

Your final written report should include: 1) an abstract (which explicitly states your output parameters from Table III), 2) an introduction that describes the purpose of your design and includes "Table I. Input parameters (design constraints)," 3) sections describing each stage of your amplifier design (including description of how component values were chosen and what *trade-offs* were made), 4) a summary that includes "Table II. Absolute maximum transistor ratings" and "Table III. Output parameters (performance figures-of-merit)" and a discussion on possible modifications that could be used to improve the design as well as any design *trade-offs* that were made.

In general, the purpose of an abstract is to succinctly describe (in roughly four to six sentences) the system and the stages of its architecture as well as the system-level design constraints and performance figures-of-merit. An introduction should establish the purpose / motivation (i.e. the critical need addressed by the presented system) and the approach taken to realizing the presented system (an audio amplifier). A design description should discuss in detail the purpose, design constraints, and performance figures-of-merit – not just for the overall system but for its individual stages. Additionally, plotted simulation results should be included. Finally, a summary should restate the system-level design constraints and performance figures-of-merit. It should emphasize the importance of the presented system by mentioning a variety of possible applications, and it should discuss future changes that could be made to improve the performance figures-of-merit.