INSTRUCTIONS--1-dB COMPRESSION POINT OF GAIN STAGE:

-Replace gain-stage circuit with your own design.

-Change output-stage resistance to the estimated value of the input

resistance of your output stage.

-Run simluation.

-Open Error Log (View->SPICE Error Log)

-Right-mouse-click on Error Log

-Select "Plot .step'ed .meas data"

-Right-mouse-click on Plot Window

-Select "Add Plot Pane"

-Right-mouse-click on lower plot pane

-Select "Add Traces"

-Left-mouse-click "gain"

-Left-mouse-click OK

-Right-mouse-click on plot title "gain" and change this statement

to "20\*log10(gain)"

-Right-mouse-click on upper plot pane

-Select "Add Traces"

-Left-mouse-click "vOUTrms"

-Left-mouse-click OK

-Right-mouse-click on plot title "vOUTrms" and change this statement

to "20\*log10(vOUTrms/1m)"

-Right-mouse-click on axes label "vSIG" and change this statement

to "20\*log10(vsig/(1m\*sqrt(2)))"

-To save these plot settings, select "Plot Settings-->Save Plot Settings"

(you will need to close the plot window and open a new one after running

another simultation; it does not automatically update)

-Determine the input 1-dB compression point value of vSIG--where the gain

deviates by 1-dB

-Determine the correpsonding output 1-dB compression point value of

20\*log10(vOUTrms/1m)"

-Ensure that your output 1-dB compression point meets the specification.

INSTRUCTIONS--TRANSIENT CURRENT CONSUMPTION:

-Place cursor over output node of VCC.

-Left-mouse click to plot I(VCC).

-Left-mouee click on collector or drain node of a transistor to plot

its transient collector current.

-Ensure that the value does not exceed the current rating of transistor.

INSTRUCTIONS--QUIESCENT CURRENT CONSUMPTION

-Comment-out the .tran, .step, and .meas SPICE directives by

hovering cursor over directive and right-mouse-clicking.

If ".meas Statement Editor" window appears left-mouse-click "Cancel."

-Run simulation.

-A DC operating point window will appear; the value of I(Vcc) is your

quiescent current consumption.

ADDITIONAL NOTE:

To place an additional voltage node label, right-mouse-click on a circuit node

after running simulation then left-mouse-click on "Place .op Data Labe" (sic).

DESIGN STRATEGY:

-Drop at least 30\*VT across RE1 (such that RE1 >> re1)

-Drop about 0.7V across base-to-emitter of Q1

-Drop about (VCC-VEE)/3 across collector-to-base of Q1 (rule of thumb)

-Adjust R1 for desired gain

-Ensure design can drive input resistance of emitter follower stage (estimate: beta\*RE2)