EEEN40690 Quantum Computing

Homework Problem Set for Topic 9: Error Correction Techniques Part 1

Instructions

- This is homework set 6 of 8. This homework set accounts for 5% of the marks for this module.
- In your report, please provide answers to the questions of this homework set. Explain clearly how the answers are obtained and what are their meaning or interpretation. Include relevant intermediate steps of the solution and explain your approach.
- Make sure that the report is readable, and the graphs (if any) are presented according to scientific/engineering standards.
- Some of the questions of the homework sets and the projects in this module may be open-ended and include a research component. Please formulate clearly your hypothesis and explain what will prove (or disprove) your hypothesis. Make sure that you provide sufficient evidence (analytical results, numerical results, modelling and simulations, evidence from the literature) to support your answer to open-ended or research problems.
- The report must be submitted online through UCD Brightspace:

  My Brightspace → EEEN40690 → Assessment → Assignments → Homework 6 (Homework for Topic 9: Error Correction Techniques Part 1)
- Late submissions will be accepted but a penalty will apply. In the case of late submissions, this module applies the standard UCD policy.
- Plagiarism and copying are offences under the terms of the Student Code, and you should be aware of the possible consequences.

Aim

The aim of this homework assignment is to introduce basic error correction techniques and understand some basic considerations behind error correction techniques.

- Repetition error correction
- Kraus operators
- Qubit metrics and their connection to the channel models
- Basic repetition code
- Transpiling quantum circuits

Problem Set

We are given a 5-qubit processor with a linear connectivity map (Fig. 1). Available gates are X, Y, Z, H and CZ. A qubit connection map is a high level representation of how physical qubits are connected in a processor. A line connecting two qubits indicates an available entangling 2-qubit gate that can be applied directly to these two qubits. We use a linear architecture as an example in this homework assignment. These

architectures are relatively common in the case of solid-state qubits (superconducting and semiconductor). Qubits 1 and 5 can be measured directly, other qubits cannot (also a common case).

A qubit connectivity map is not the same as a quantum circuit. A quantum circuit shows a sequence of one-, two- or many-qubits gates implemented on qubits. The key difference is that in a quantum circuit we can place a two-qubit gate between a pair of qubits, while in a real device there may be no direct connection between these two qubits at all.

In addition, we can usually use any set of quantum gates in a quantum circuit. However, when executed in a real processor, the quantum gates of a given circuit must be translated ("transpiled") into the quantum gates available for a given processor. As a result, the actual sequence of actions on a quantum processor can be *very* different from what was originally presented as quantum circuit. Translations between different sets of quantum gates (for instance, expressing CX in terms of CZ) are common and can be easily found in the literature and on the Internet.

This assignments contains elements of research and open ended quesions.

1. How would you use this 5-qubit processor for a basic repetition code (3 data qubits, 2 ancilla qubits). Outline what qubits would you choose as data, what qubits – as ancilla. Comment on your choice.
2. What would change if only Qubit 1 can be measured directly?

   Hint: If you are not sure if this architecture is compatible with the repletion code, try to identify the exact issues that may impede the use of this architecture with the repetition code.

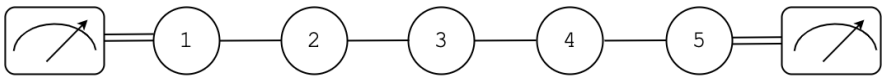

Figure 1: A qubit connection map for Problem 1.

3. Consider a version of this processor with semiconductor qubits whose $T_1 = 40$ ms and $T_2 = 10$ μs. What version of the repetition error correction code we should be using? (What type of error should we really correct?) Draw a circuit using the set of gates available for this processor.
4. Consider a version of this processor with superconducting qubits whose $T_1 = 20$ μs and $T_2 = 50$ μs. What version of the repetition error correction code we should be using? (What type of error should we really correct?) Draw a circuit using the set of gates available for this processor.