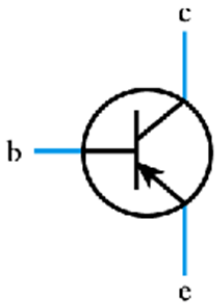
Solution set 4 TFY4185 Måleteknikk Issued 12 October 2015

1) Which terminal represents the control input of a bipolar transistor?

a) The gate
b) The collector
c) <u>The base</u>
d) The emitter

It is the current to the base of the transistor (controlled by the bias V_{BE}) that is amplified to produce the current through the collector and emitter of the transistor, I_{CE}. Note, when we say that the current is amplified, we mean that this current is supplied by the power supply to which the collector is connected, and the amount of current drawn from the power supply is controlled by the base current .

2) What kind of device does the following symbol represent?



a) An *npn* bipolar transistor.
b) An *n*-channel JFET.
c) <u>A *pnp* bipolar transistor.</u>
d) A *p*-channel JFET.

*This represents a pnp transistor (or **P**ointing-in transistor). Since the majority charge carriers in the collector and emitter are positive "holes", a base held at a lower potential than the emitter would cause a small current to flow from the emitter to the base, and the size of this current (controlled by the negative bias V_{BE}) would allow a large current to flow from the emitter to the collector (since current is defined as the motion of positive charge carriers).*

*This could be contrasted to an npn (or **N**ot-pointing in) transistor, where the emitter and collector have electrons as the majority charge carriers. Thus, the base at a higher potential than the emitter will cause a small current to flow from the base to the emitter, and the size of this current (controlled by the positive bias V_{BE}) would allow a large current to flow from the collector to the emitter (since current is defined as the opposite direction as the motion of the negative charge carriers)*

3) Which of the following expressions represents the DC current gain of a bipolar transistor?

a) dI_C/dI_B

b) $\underline{I_C/I_B}$

c) dI_C/dV_{BE}

d) I_C/V_{BE}

As we have seen, the current flowing in the base is a consequence of the bias between the base and the emitter. The sense of this bias is to reduce the base-emitter depletion region and allow the current to flow between the base and emitter. However, since the base is lightly doped, there is a huge excess of majority charge carriers from the emitter entering the base material, and these crowd into the collector-base depletion region, where they are accelerated further to the collector. This is then the origin of the current between the collector and the emitter. Thus, the size of base current is representative of how many excess majority charge carriers from the emitter we are allowing to pass through to the collector. The gain of the device is how much I_C changes for a given change in I_B. However, since the relationship between I_C and I_B is approximately linear, so $dI_C/dI_B \approx I_C/I_B$, the gain of the device is how much current we get out, I_C, divided by how much current we have to create to cause that current, I_B.

4) Which of the following expressions represents the transconductance of a bipolar transistor?

a) I_C/V_{BE}

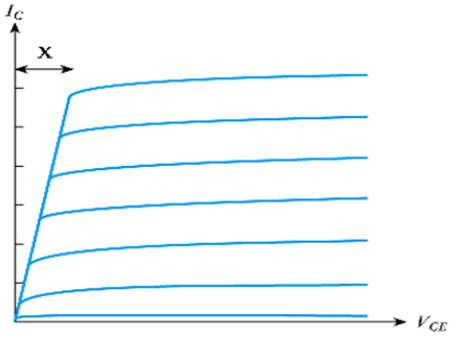
b) $\underline{dI_C/dV_{BE}}$

c) I_C/I_B

d) dI_C/dI_B

Any time you see the word transconductance, it will mean a current to voltage relationship (remember our current to voltage amplifier is also called a transconductance amplifier). As mentioned in question 3, the collector current is linearly related to the base current, and so a single constant scales I_B to I_C. However the bias, V_{BE} is related to the base current, I_B, the same way the current in the diode (a pn junction) would relate the bias voltage to the current flow. But this relationship in a diode is non-linear (exponential in fact). Thus if we substitute V_{BE} in for I_B, we have the output collector current, I_C in a non-linear (exponential) relationship with the base-emitter bias, V_{BE}. So instead of I_C having a nearly constant slope with V_{BE}, (the way it did with I_B), the slope depends on the current, I_C. Thus we have to keep the differential in the gain if we want to relate I_C to V_{BE}, and dI_C/dV_{BE}, the transconductance, is a function of I_C.

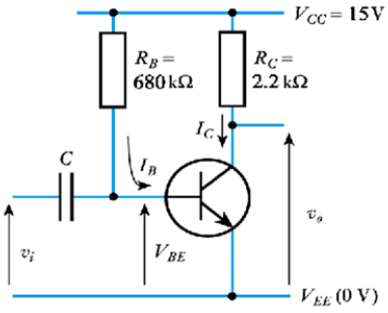
5) In the bipolar transistor output characteristics shown below, what region is represented by the symbol 'X'?



a) The active region
b) The space-charge region
c) <u>The saturation region</u>
d) The ohmic region

Here the region of the curve at low values of V_{CE} is called the saturation region. At these low values of V_{CE}, the transistor action does not occur and the transistor is in an "on" condition. This means that, assuming the base potential creates a forward bias between the base and emitter, there will also be a forward bias between the base and the collector due to the small potential between the collector and emitter, V_{CE}. Under forward bias the depletion regions are physically very small, and a potential between the collector and the emitter drives the collector majority charge carriers into the base, where they recombine. However, it also drives the base majority charge into the emitter where they recombine. This represents a current between the collector and the emitter. This current will increase with V_{CE} until we reach a point where the collector becomes forward biased relative to the base, and transistor action can occur. Since both junctions are conducting and on, this is called saturation.

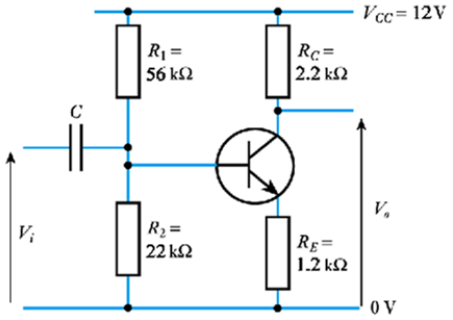
6) Determine the quiescent collector current of the following circuit, given that the h_{FE} of the transistor is 150.



a) 1.15 mA
b) 2.1 mA
c) <u>3.15 mA</u>
d) 5.3 mA

*The current gain is 150.The base current is driven by the voltage drop across the 680 kΩ resistor, which is 15V –V_{BE}. Now VBE is the "on" voltage of this pn-junction, ~0.7 V. Hence I_B = (15-0.7)V/680 kΩ = 21μA, and I_C=h_{FE}*I_B = 150*21μA = 3.15 mA*

7) Determine the quiescent output voltage of the following circuit.



a) 4.3 V
b) 4.8 V
c) 5.6 V
d) <u>7.1 V</u>

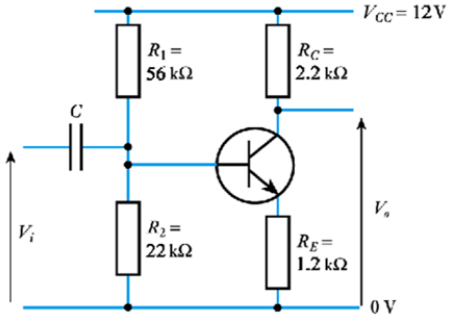
For the DC, or quiescent voltage, we know that Vo is going to be the whatever voltage from V_{CC} is left after the collector current (determined by the transistor) drops voltage across R_C. How do we get the collector current? We know that the collector current across R_E will be proportional to the voltage at the emitter, and this we can get from the potential on the base and the forward voltage drop across the pn-junction. The base voltage is determined by the voltage divider set up by R_1 and R_2: $V_B = V_{CC} \cdot R_2/(R_2+R_1)=22000/(22000+56000) = 3.38V$.

Now, from the base, there is the forward drop of the pn-junction, 0.7V, and what is left will be the voltage across R_E, so that $V_E = V_B-0.7V = 3.38V-0.7V= 2.68V$. Now from this we get the current flowing through the emitter resistor, I_E which is the same as I_C. So:

$I_E = I_C = V_E/R_E = 2.68\ V/\ 1200\Omega = 2.24\ mA$.

Finally, the voltage dropped across $V_C = I_C \cdot R_C = 2.24mA \cdot 2200\ \Omega = 4.92V$, and this plus Vo must equal V_{CC}. Thus, Vo = 12V -4.92V = 7.08 V.

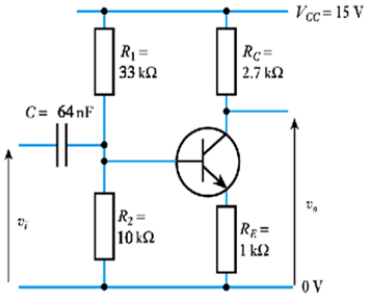
8) What is the magnitude of the small-signal voltage gain of the circuit given in the last question?



a) -<u>1.83</u>
b) -2.2
c) -2.56
d) -2.83

For small-signal, or the AC gain of the circuit, we should consider the equivalent circuit of the transistor where R_C and R_E are in parallel. However, since this circuit has feedback ($R_E \neq 0$) we can make the assumption that the AC component of the forward voltage across the base to emitter forward junction, v_{be}, is small compared to either $v_b \approx v_i$ or v_e. Thus, $v_b \approx v_i \approx v_e$, and $v_e = i_e/R_E$. Now, as above, $i_c \approx i_e$, and $v_o = -i_c \cdot R_C \approx -i_e \cdot R_C$. We can use our previous results from the line above that $v_b \approx v_i \approx v_e = i_e/R_E$ to say that $i_e \approx v_i/R_E$ above, and that the voltage gain $v_o/v_i \approx -R_C/R_E = -2.2k\Omega/1.2k\Omega = -1.83$.

9) Determine the low-frequency cut-off of the following circuit.



a) 18 Hz
b) 178 Hz
c) <u>324 Hz</u>
d) 2037 Hz

Since we are talking about AC signals, we have to consider the equivalent circuit of the transistor where R_1 and R_2 are in parallel (an AC signal will see a coupling between V_{CC} and ground, perhaps through the filter capacitors of the power supply of V_{CC}). Thus, an AC signal v_i will see a capacitor of 64 nF in series with the equivalent resistance, $R = R_1 // R_2 = R_1 \cdot R_2/(R_1+R_2) = 33k\Omega \cdot 10\ k\Omega/(33\ k\Omega + 10\ k\Omega) = 7.7\ k\Omega$. The cut off frequency of this high-pass filter (we are taking the voltage across R) will be:

$\omega_c = 1/(R \cdot C) = 1/(7.7x10^3\ \Omega \cdot 64x10^{-9} F) = 2.04x10^3 rad/s$, and $f_c = \omega_c/(2\pi) = 324$ Hz.

10) The noise power produced by a resistor is not dependent on its resistance.

a) True b) False

The noise Voltage does depend on the resistance, but the power is just 4kT·bandwidth

11) What form of noise is produced as a result of the random, thermally induced motion of the atoms in a material?

a) Johnson noise b) Shot noise c) Flicker noise d) Interference

12) What form of noise is produced as a result of random variations in the diffusion of charge carriers within devices?

a) Johnson noise b) Shot noise **c) Flicker noise** d) Interference

13) What is meant by 'pink noise'?

a) Most of the noise power is concentrated at low frequencies.
b) The noise has a frequency equal to that of pink light.
c) Most of the noise power is concentrated at high frequencies.
d) The noise has a uniform spectrum.

14) At low temperatures, noise in bipolar transistors tends to be dominated by thermal noise.

a) True **b) False**

Remember, reducing the temperature will reduce the noise so that other forms (flicker noise at frequencies below a few kHz and shot noise) will dominate.

15) Shot noise is normally insignificant in all forms of FET.

a) True b) False

Flicker noise at low frequencies and thermal noise from the resistance of the channel dominate in an FET

16) At a particular point in a circuit, a signal of 1 V r.m.s. is corrupted by 1 mV r.m.s. of noise. What is the S/N ratio at this point?

a) 30 dB b) 40 dB c) 50 dB **d) 60 dB**

*20log(Vs/Vn) = 20log(1000) = 20*3 = 60*

17) Combinations of conductors and components that form loops within a circuit act as electric dipoles.

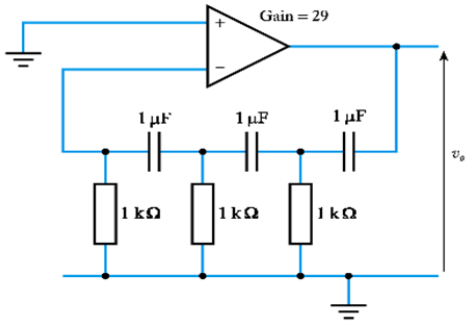
a) True **b) False**

The current flowing in a loop will create a magnetic dipole, not an electric one.

18) Which of the following is not an appropriate design method for tackling EMC related problems?

a) Routing noise sensitive signals around the outside of a printed circuit board to keep them away from other signals.
b) Minimise the area of any loops formed.
c) Use multilayer boards to reduce coupling between circuits.
d) Minimise track lengths.

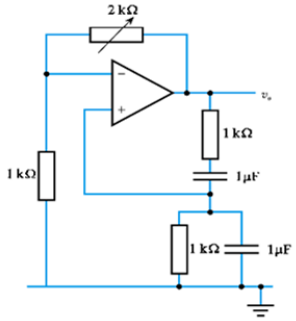
19) Calculate the frequency of oscillation of the phase-shift oscillator shown here.



a) 26 Hz. **b) 65 Hz.** c) 135 Hz. d) 238 Hz.

While one could repeat the node analysis to get the equivalent frequency and phase shift, here the better part of valour is to know the formula for the oscillation frequency $\omega = 1/(RC\cdot\sqrt{6})$, and $f=\omega/(2\pi)$. So, $R=1000\Omega$ and $C = 1x10^{-6}F$ give $f = 65$ Hz

20) Calculate the frequency of oscillation of the Wien-bridge oscillator shown here.

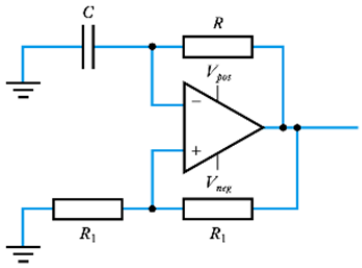


a) 159 Hz. b) 238 Hz. c) 327 Hz. d) 424 Hz.

Once again, one could do a non-trivial circuit analysis to get the equivalent frequency and

phase shift. But again the better part of valour is to know the formula for the oscillation frequency $\omega = 1/(RC)$, and $f=\omega/(2\pi)$. So, $R=1000\Omega$ and $C = 1x10^{-6}F$ give $f = 159$ Hz

21) What is the maximum positive output voltage of the relaxation oscillator shown here?



a) $\underline{V_{pos}}$ b) $V_{pos}/2$ c) $V_{pos}/4$ d) $(C/R)V_{pos}$

When the output is V_{pos}, the V_+ input will be at $V_{pos}/2$ as it is divided by 2 by the resistor network. When the capacitor charges to this voltage, and $V_->V_+$, then the output will switch to $-V_{pos}$, and the capacitor will discharge until the V_- will again go below V_+.

22) Crystals have two resonant frequencies.

a) <u>True</u> b) False

This is true. The piezoelectric crystal represents a series resistance, inductance and capacitance, but this is in parallel with the overall capacitance of the crystal (between the contacts). Thus there is a parallel resonance (where the impedance approaches infinity) and at a slightly lower frequency there is a series resonance (where the impedance approaches zero). At all other frequencies, the crystal looks like a capacity.

23) What elements are found within the equivalent circuit of a crystal?

a) Resistance alone. b) Resistance and capacitance.
c) Resistance and inductance. **d) <u>Resistance, capacitance and inductance</u>.**

As mentioned above, the piezoelectric crystal represents a series resistance, inductance and capacitance (that simulate the piezoelectric characteristics), but this is in parallel with the overall capacitance of the crystal (between the contacts).

24) In order to ensure stability in a circuit, the designer must ensure that the phase shift reaches 180 degrees before the gain falls to unity.

a) True **b) <u>False</u>**

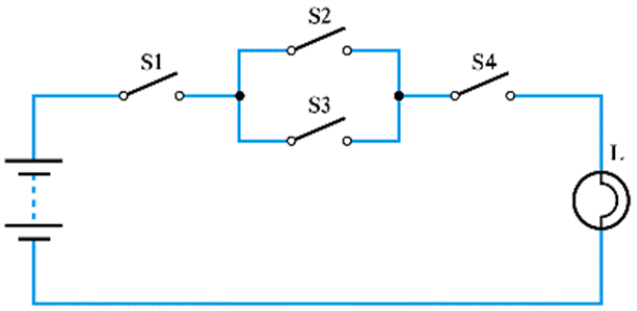
This is the wrong way around. Assuming we have built a stable feedback circuit with gain greater than one, the feedback will be used to cancel the voltage difference at the inputs of the amplifier. If there is a phase shift in the feedback loop of 180°, the phase shifted feedback will in fact enhance the voltage difference at the inputs of the amplifier, causing an even larger output voltage (i.e., positive feedback). The differences between the inputs will be: $(|V_+|-|V_-|)+G((|V_+|-|V_-|)$. If the gain of the circuit is > 1 when this happens, then the output will grow quickly. If $G < 1$, then the resonance will damp quickly.

25) What is the name given to the amount (in dB) by which the loop gain is less than 0 dB when the phase reaches 180 degrees?

a) <u>The gain margin.</u>
b) The transition point.
c) The zero-gain bandwidth.
d) The phase margin.

The gain margin is the space we have between the frequency at which the gain becomes < 1, where a positive feedback will damp quickly, and the frequency would create a phase shift that would result in positive feedback.

26) What logic function corresponds to the following arrangement?



a) <u>*L* = S1 AND (S2 OR S3) AND S4.</u>
b) *L* = S1 OR (S2 AND S3) OR S4.
c) *L* = (S1 OR S2) AND (S3 OR S4).
d) *L* = (S1 AND S2) OR (S3 AND S4).

Here either S2 or S3 must be closed to light the bulb. However, without both S1 and S4 closed there will be an open circuit and the bulb will not light. Thus we have S1 and S4 must be closed, and at the same time either S2 or S3 must be closed)

27) Which logic gate has the following truth table?

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

a) A two-input AND gate.
b) An exclusive OR gate.
c) An exclusive NOR gate.
d) <u>A two-input OR gate.</u>

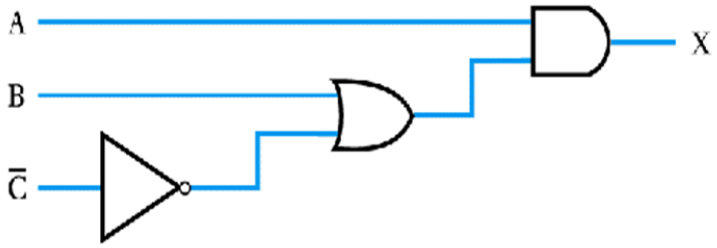
Two input is clear since we have columns A and B. Next, we see that C is one if either A or B are 1, indicating an OR gate. The fact that A=1 at the same time that B=1 also produces C=1 is a characteristic of the OR gate. Whenever A = 1 includes the times when B is =1.

28) In Boolean algebra the AND function is represented by the '+' sign.

a) True
b) <u>False</u>

This is false. We represent and AND function with a multiplication since only 1·1 will produce a non-zero product.

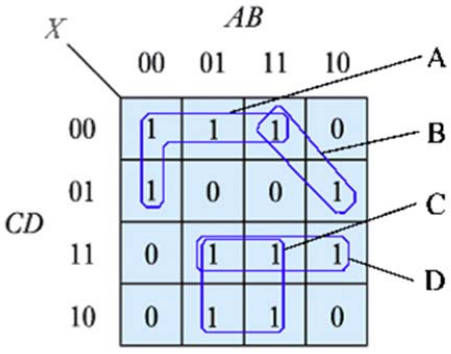
29) What Boolean expression describes the output X of this arrangement?



a) X = A + B + C
b) <u>X = A·(B + C)</u>
c) X = (A·B) + C
d) X = A + (B·C)

Start at the left hand side and look how the signals are combined at the first gate. We have Č being inverted to C. Continuing to the right, at the next gate we come to, this C input is being OR'ed with B, so the output of this next gate is (C+B). Again, continue to the right to find this OR-gate output being AND'ed with A, so the final output is X = A·(B+C).

30) In the Karnaugh map shown below, which of the loops shown represents a legal grouping?



A) B) **<u>C)</u>** D)

The Karnaugh map allows one to combine inputs that do not influence the output. The groups can be rectangles or squares. One might think group "D" would be legal. However, this would be the term ABCD+$\bar{A}$BCD+A$\bar{B}$CD. This can be simplified either to BCD+A$\bar{B}$CD=CD(B+A$\bar{B}$), but no farther, or the first and third terms can be combined to give ACD+$\bar{A}$BCD=CD(A+$\bar{A}$B), but no farther simplification is possible. Thus, for n variables, we can from groups of 2^n elements provided they represent all state of the n

variables. This will be true if each side of the rectangles formed by the groups have 2^m elements, where m = 0, 1, 2…n.