

## Exam on 2 December

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- Format:
  - 20 multiple-choice homework style questions (4 pts each)
  - 2 “show your work” questions (10 points each)
- You can have with you
  - 1 side of A5 with your formulae on it (not a special sheet)
  - Dictionary or bi-lingual dictionary
  - Any calculator
- Need 53% for pass

# Key Points Chapter 3

## Resistance and DC Circuits

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- An electric current is a flow of charge
- A voltage source produces an e.m.f. which can cause a current to flow
- Current in a conductor is directly proportional to voltage
- At any instant the sum of the currents into a node is zero
- At any instant the sum of the voltages around a loop is zero
- Any two terminal network of resistors and energy sources can be replaced by a Thévenin or Norton equivalent circuit
  - Know this and perhaps simple examples
- Nodal and mesh analysis provide systematic methods of applying Kirchhoff's laws



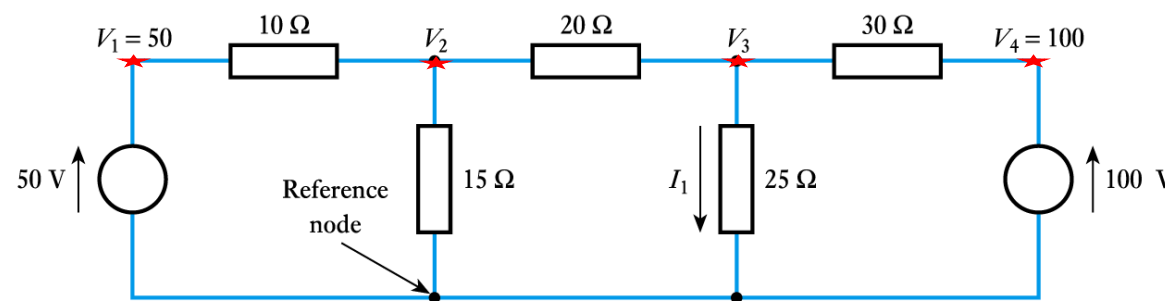
Video 3B



3.10

# Nodal Analysis

- Six steps:
  1. Chose one node as the reference node
  2. Label remaining nodes  $V_1$ ,  $V_2$ , etc. (★)
  3. Label any known voltages & postulate currents
  4. Apply Kirchhoff's current law to each unknown node
  5. Solve simultaneous equations to determine voltages
  6. If necessary calculate required currents



Neil Storey, *Electronics: A Systems Approach*, 5<sup>th</sup> Edition © Pearson Education Limited 2013



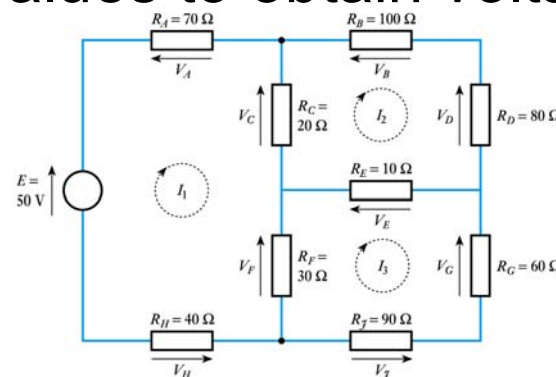
Video 3C



3.11

# Mesh Analysis

- Four steps:
  1. Identify the meshes and assign a clockwise-flowing current to each. Label these  $I_1$ ,  $I_2$ , etc.
  2. Apply Kirchhoff's voltage (&  $V=IR$ ) law to each mesh
  3. Solve the simultaneous equations to determine the currents  $I_1$ ,  $I_2$ , etc.
  4. Use these values to obtain voltages if required



3.4

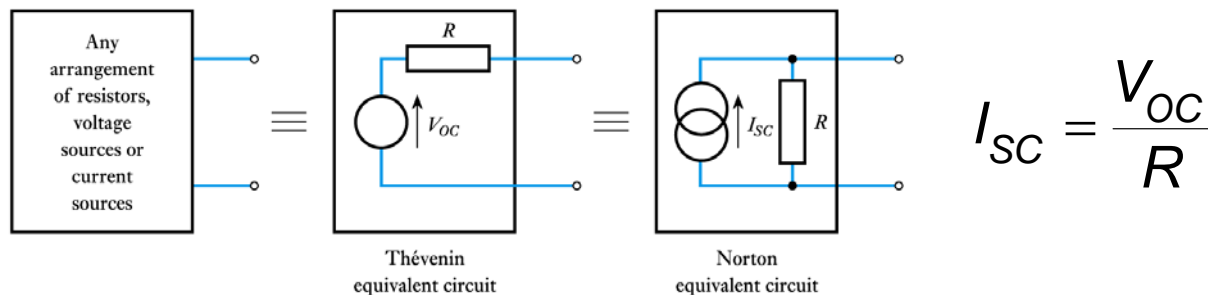
# How to Apply Superposition

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- To find the contribution due to an individual independent source, zero out the other independent sources in the circuit.
  - Voltage source  $\Rightarrow$  short circuit.
  - Current source  $\Rightarrow$  open circuit.
- Solve the resulting circuit using your favorite technique(s).
- Add the contributions of the independent sources.

# Generalized Thevenin/Norton Analysis

1. Pick a good breaking point in the circuit.  
Example of a good break point, remove the load resistor.
2. **Thevenin:** Compute the open circuit voltage,  $V_{OC}$ .  
**Norton:** Compute the short circuit current,  $I_{SC}$ .
3. Compute the Thevenin equivalent resistance,  $R_{Th}$  (or impedance,  $\mathbf{Z}_{Th}$ ) by short circuiting all the voltage sources and open circuiting all the current sources. Remember  $R_{Th}$  (or  $\mathbf{Z}_{Th}$ ) =  $V_{OC}/I_{SC}$
4. **Thevenin:** Replace circuit with  $V_{OC}$  in series with  $R_{Th}$ ,  $\mathbf{Z}_{Th}$ .  
**Norton:** Replace circuit with  $I_{SC}$  in parallel with  $R_{Th}$ ,  $\mathbf{Z}_{Th}$ .

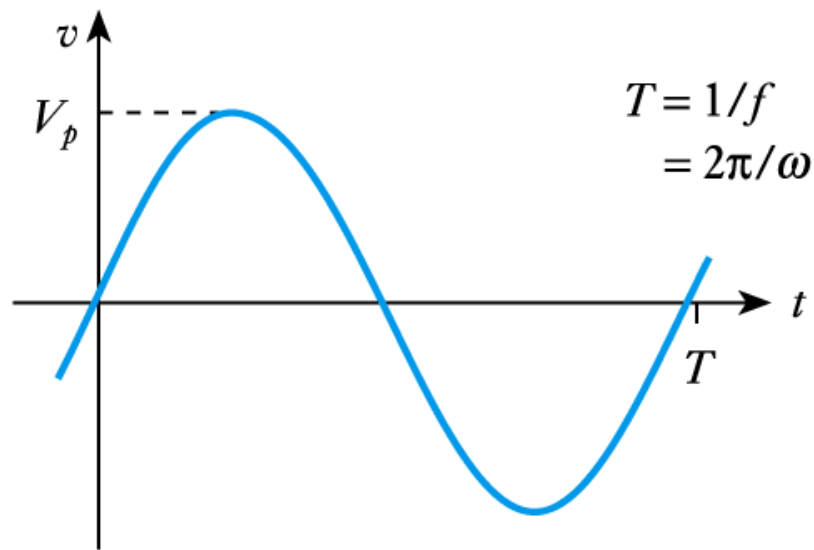


## Key Points chapter 6- Alternating Voltages and Currents

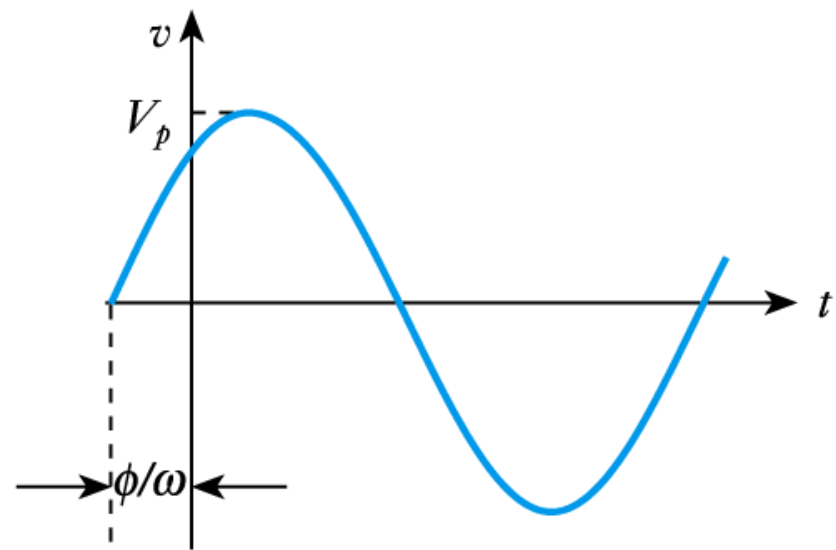
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- A sinusoidal voltage waveform can be described by the equation  $v = V_p \sin(\omega t + \phi)$
- The voltage across a resistor is *in phase with* the current, the voltage across an inductor *leads* the current by  $90^\circ$ , and the voltage across a capacitor *lags* the current by  $90^\circ$
- The reactance of an inductor  $X_L = \omega L$
- The reactance of a capacitor  $X_C = 1/\omega C$
- The relationship between current and voltage in circuits containing reactance can be described by its impedance
- The use of impedance is simplified by the use of complex notation

- If  $\phi$  is in radians, then a time delay  $t$  is given by  $\phi / \omega$  as shown below



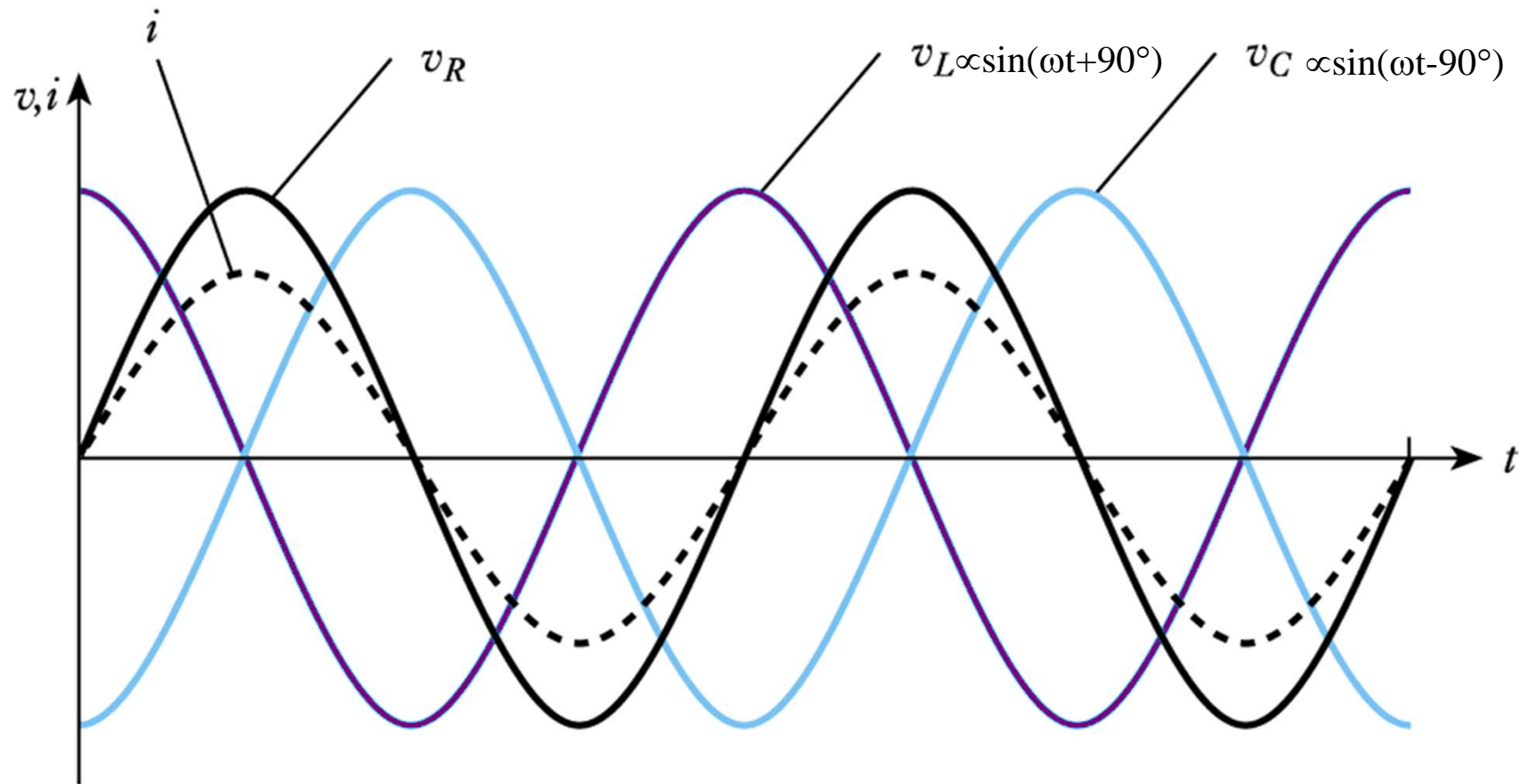
(a)  $v = V_p \sin(\omega t)$



(b)  $v = V_p \sin(\omega t + \phi)$

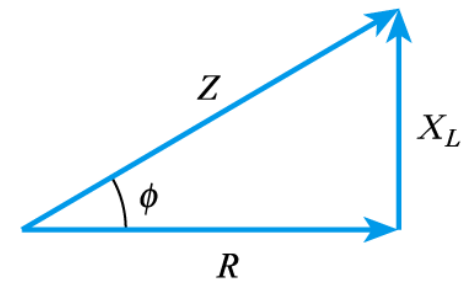
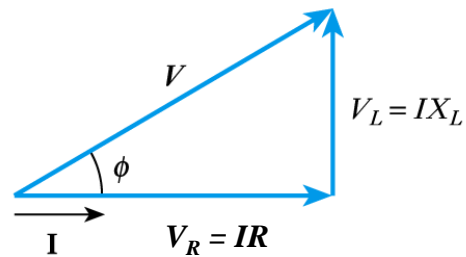
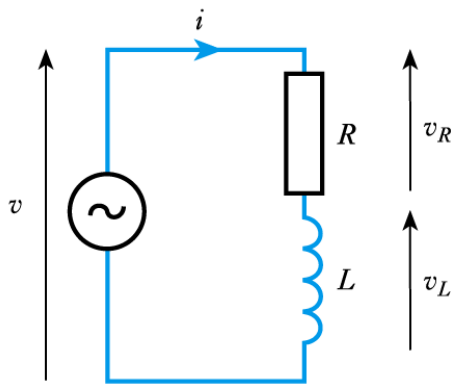


**CIVIL (in C, I before V, but V before I in L) or  
ELI the ICE man (E leads I in L, I leads E in C)**

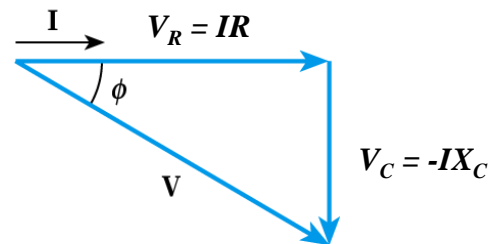
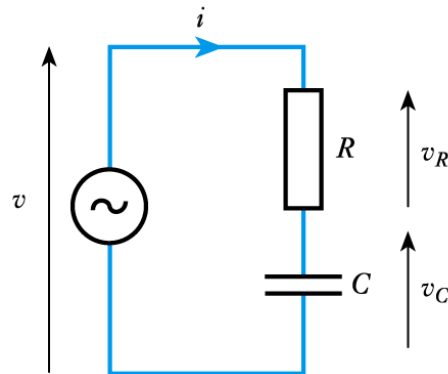


In parallel circuits,  $V$  is the same across all elements  $\Rightarrow I = V/R$   
 so  $V$  leading  $I$  in  $L \Rightarrow I$  lags  $V$  in  $L \Rightarrow I_L = -V/X_L$

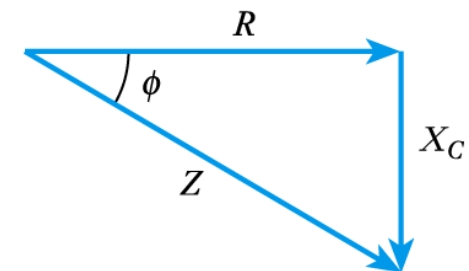
- Consider these series circuits and phasor diagrams



(a)



(b)



(b)

3.10



6.6

## Complex Notation

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- We can represent impedance using complex notation where
- Resistors:  $Z_R = R$
- Inductors:  $Z_L = jX_L = j\omega L$
- Capacitors:  $Z_C = -jX_C = -j\frac{1}{\omega C} = \frac{1}{j\omega C}$

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## Key Points Chapter 7- Power in AC Circuits

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- In resistive circuits the average power is equal to  $VI$ , where  $V$  and  $I$  are r.m.s. values
- In a capacitor the current *leads* the voltage by  $90^\circ$  and the average power is zero
- In an inductor the current *lags* the voltage by  $90^\circ$  and the average power is zero
- In circuits with both resistive and reactive elements, the *instantaneous power* is:  $p = vi = VI \cos \phi - VI \cos(2\omega t - \phi)$  and *the average power* is  $VI \cos \phi$
- The term  $\cos \phi$  is called the power factor
- Power factor correction is important in high-power systems
- High-power systems often use three-phase arrangements

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- Know

Active Power dissipated in R	$P = VI \cos \phi$	watts
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Reactive Power stored in C & L	$Q = VI \sin \phi$	var
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Apparent Power	$S = VI$	VA
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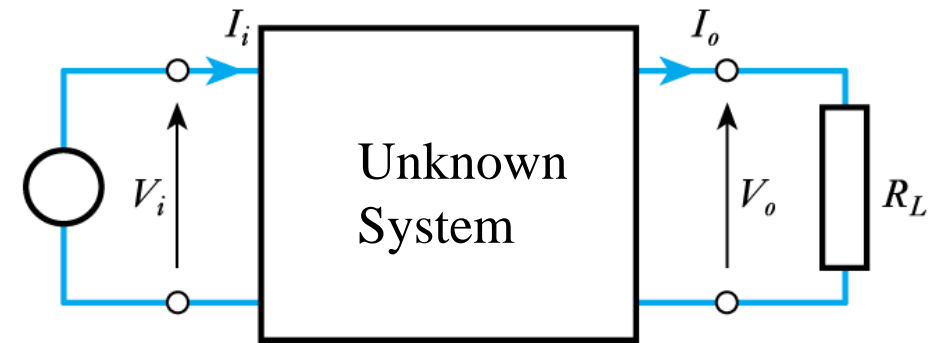
$$S^2 = P^2 + Q^2 \text{ and Power factor } \equiv \cos \phi$$

## Key Points Chapter 8-

# Frequency Characteristics of AC Circuits

- The reactance of capacitors and inductors is dependent on frequency
- Single  $RC$  or  $RL$  networks can produce an arrangement with a single upper or lower cut-off frequency
- In each case the angular cut-off frequency  $\omega_o$  is given by the reciprocal of the time constant  $T$
- For an  $RC$  circuit  $T = CR$ , for an  $RL$  circuit  $T = L/R$
- Resonance occurs when the reactance of the capacitive element cancels that of the inductive element
- Simple  $RC$  or  $RL$  networks represent single-pole filters
- Stray capacitance and inductance are found in all circuits

- We then define voltages and currents at the input and output



(b) A typical arrangement

- Then power gain ( $A_p$ ) =  $\frac{P_o}{P_i}$

$$\text{Power gain (dB)} = 10 \log_{10} \frac{P_o}{P_i}$$

$$\text{voltage gain } (A_v) = \frac{V_o}{V_i}$$

$$\text{Voltage gain (dB)} = 20 \log_{10} \frac{V_o}{V_i}$$

$$\text{current gain } (A_i) = \frac{I_o}{I_i}$$

$$\text{Current gain (dB)} = 20 \log_{10} \frac{I_o}{I_i}$$

**3.15**

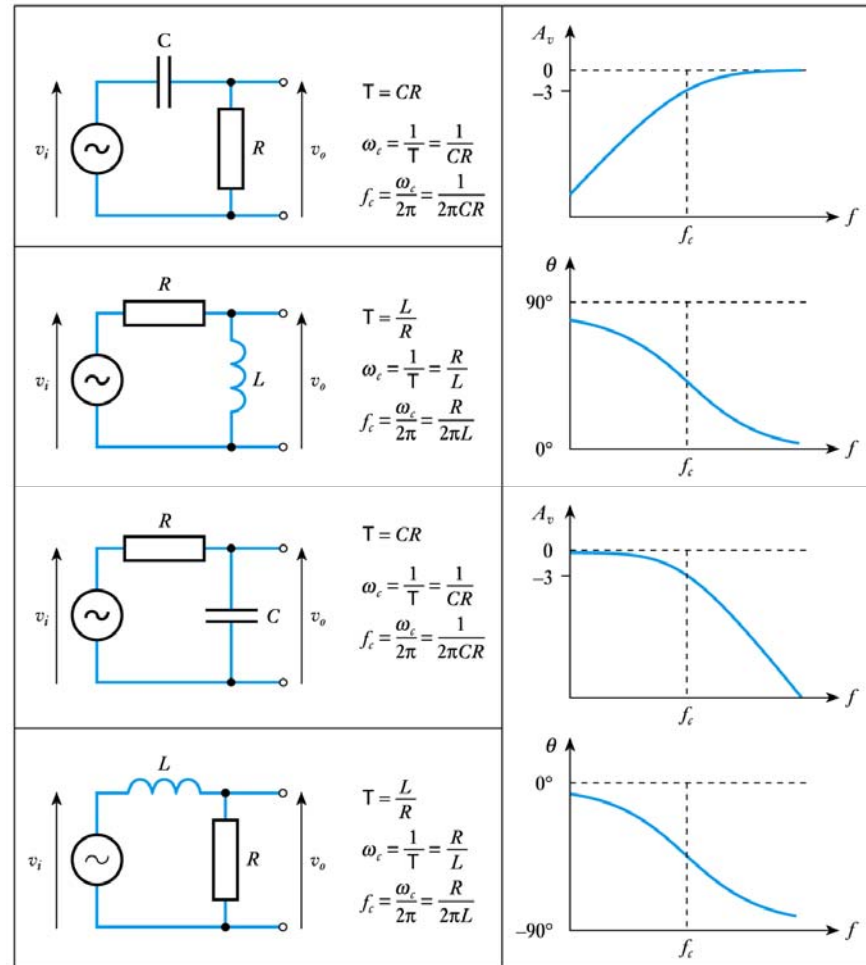
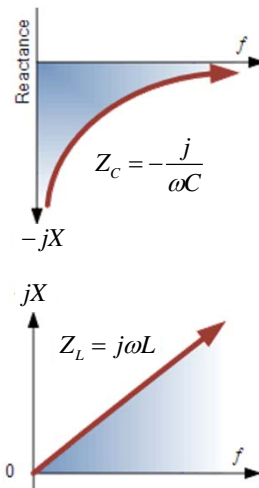
# A Comparison of RC and RL Networks

- Circuits using RC and RL techniques have similar characteristics

– see **Figure 8.12** in the course text

At High frequencies  
C looks like a wire  
At Low frequencies  
C looks like a big resistor

At Low frequencies  
L looks like a wire  
At High frequencies  
L looks like a big resistor





# RLC Circuits and Resonance

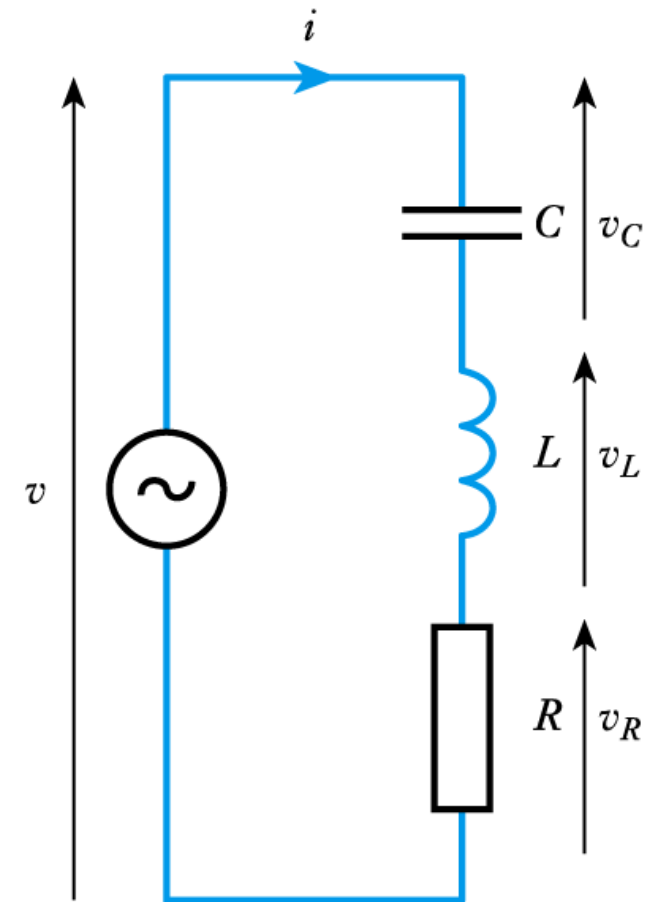
## ■ Series RLC circuits

- the impedance is given by

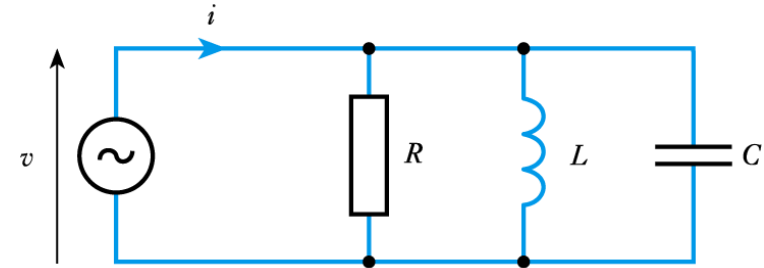
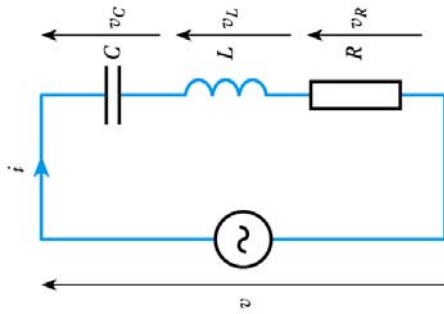
$$\mathbf{Z} = R + j\omega L + \frac{1}{j\omega C} = R + j(\omega L - \frac{1}{\omega C})$$

- if the magnitude of the reactance of the inductor and capacitor are equal, the imaginary part is zero, and **the impedance is simply  $R$**
- this occurs when

$$\omega L = \frac{1}{\omega C} \quad \omega^2 = \frac{1}{LC} \quad \omega_o = \frac{1}{\sqrt{LC}}$$



3.17



- Know the resonant frequencies of series and parallel RLC circuits

$$\omega_o = \frac{1}{\sqrt{LC}} \quad f_o = \frac{1}{2\pi\sqrt{LC}}$$

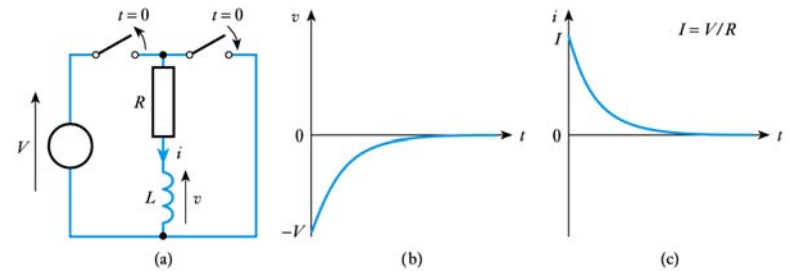
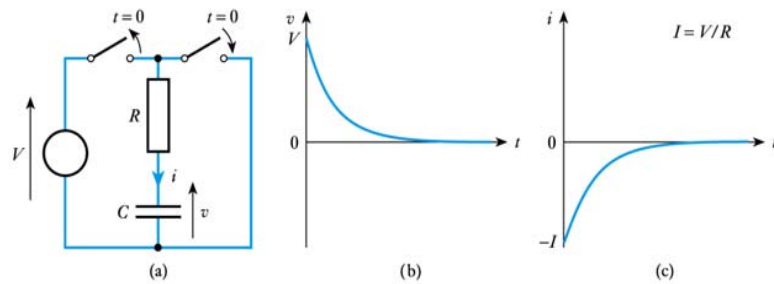
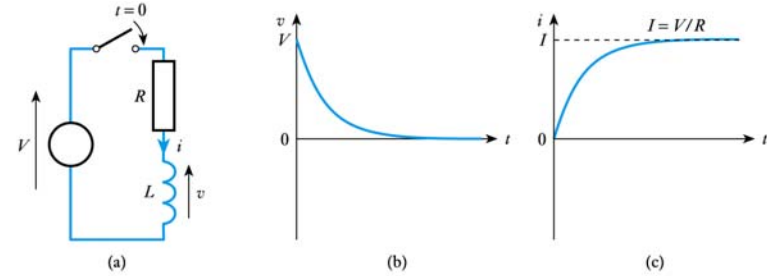
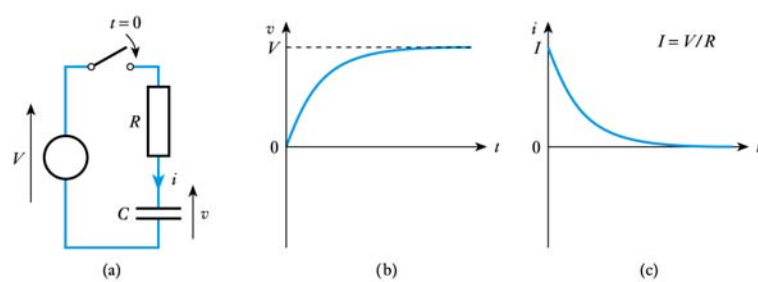
- Know whether the resonant condition is a maximum (parallel) or minimum (series) impedance
- Know the quality factor, Q for each circuit and what it means.
  - this is the ratio of the power stored (in L or C) to the power dissipated (in R) in each cycle

## Key Points Chapter 9-Transient Behaviour

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- The charging or discharging of a capacitor, and the energising and de-energising of an inductor, are each associated with exponential voltage and current waveforms
- Circuits that contain resistance, and either capacitance or inductance, are termed first-order systems
- The increasing or decreasing exponential waveforms of first-order systems can be described by the initial and final value formulae
- Circuits that contain both capacitance and inductance are usually second-order systems. These are characterised by their undamped natural frequency and their damping factor

## ■ A comparison of the four circuits



# Response of First-Order Systems

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- **Know Initial and final value formulae (& how to use)**

- increasing or decreasing exponential waveforms (for either voltage or current) are given by:

$$v = V_f + (V_i - V_f)e^{-t/T}$$

$$i = I_f + (I_i - I_f)e^{-t/T}$$

- where  $V_i$  and  $I_i$  are the *initial* values of the voltage and current
- where  $V_f$  and  $I_f$  are the *final* values of the voltage and current
- the first term in each case is the **steady-state response**
- the second term represents the **transient response**
- the combination gives the **total response** of the arrangement

# Second-Order Systems

- Circuits containing both capacitance and inductance are normally described by second-order differential equations. These are termed **second-order systems**

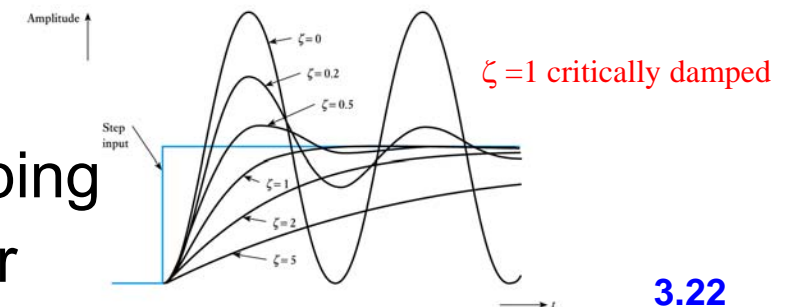
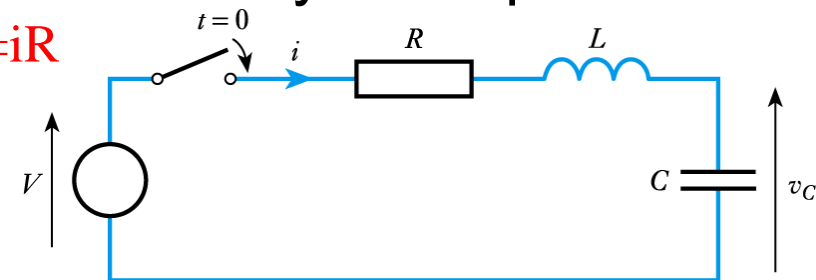
– for example, this circuit is described by the equation

$v_R + v_L + v_C = V$  and  $v_L = L(di/dt)$ , and  $v_R = iR$   
but  $i = C(dv_C/dt)$ . So

$$LC \frac{d^2 v_C}{dt^2} + RC \frac{dv_C}{dt} + v_C = V$$

– Or general form:

$$\frac{1}{\omega_n^2} \frac{d^2 y}{dt^2} + \frac{2\zeta}{\omega_n} \frac{dy}{dt} + y = x \quad \zeta = \text{damping factor}$$



3.22

## What about chapters 11, 12 and 13?

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- These were for your information
- We use regard a sensor as a device that has a Thevenin (Norton) Voltage (current) and resistance
- This will interact with the rest of the circuit
- Note, the voltage detected or amplified may not be the same as the sensor voltage

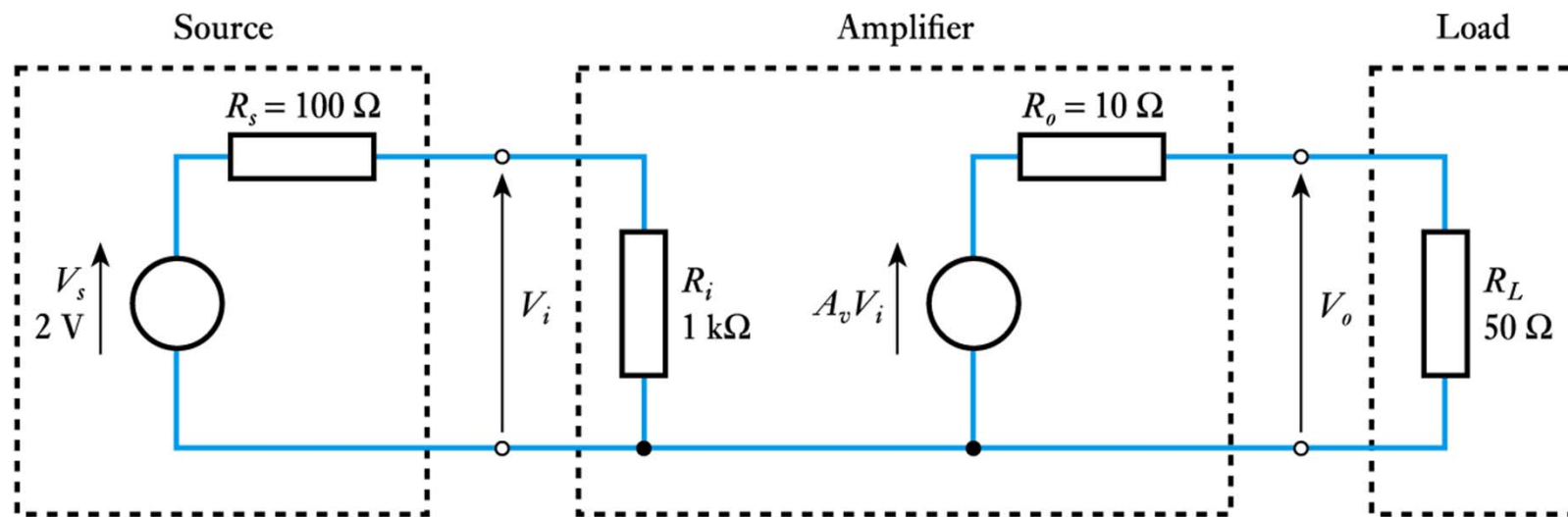
## Key points Chapter 14- Amplification

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- Amplification forms part of most electronic systems
- Amplifiers may be *active* or *passive*
- Equivalent circuits are useful when investigating the interaction between circuits
- The gain of all amplifiers falls at high frequencies
- The gain of some amplifiers falls at low frequencies
- Differential amplifiers take as their input the difference between two input signals
- Some amplifiers are very simple in construction

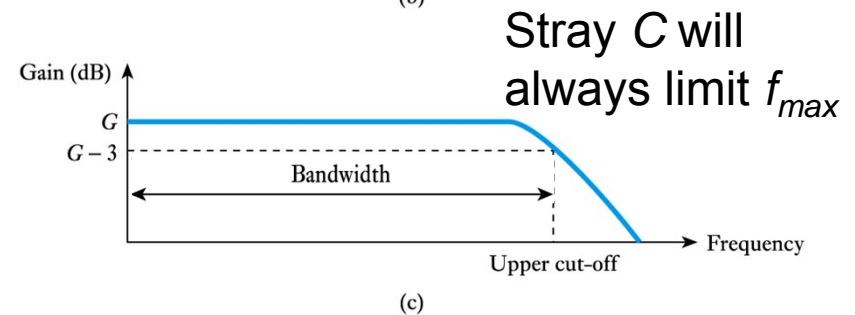
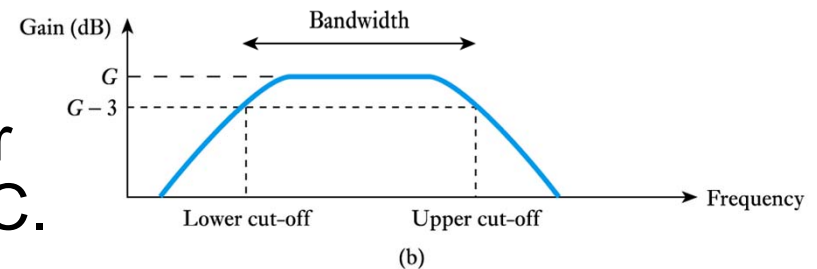
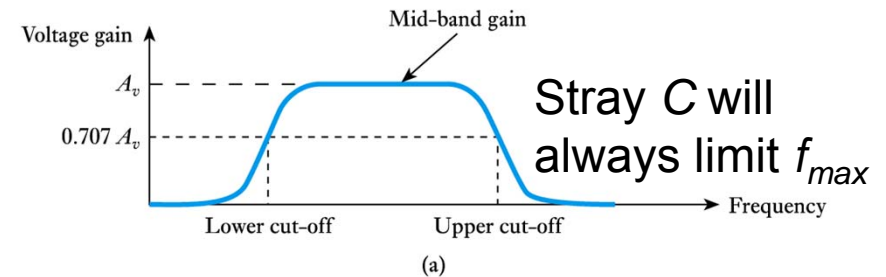


- Construct an equivalent circuit of the amplifier, the source and the load to calculate loading effects
  - $V_i$  divided between  $R_i$  and  $R_s$ ,  $V_o$  between  $R_o$  and  $R_L$
  - Amplifier gain is  $A_v$ , but Actual gain of circuit is  $V_o/V_i$



# Frequency response and bandwidth

- (a) shows an AC coupled amplifier.
- (b) shows the same amplifier – with gain in dBs,
- (c) shows a DC coupled amplifier – the gain is constant down to DC.
- The **bandwidth** is the difference between the upper and lower (or zero) cut-off frequencies



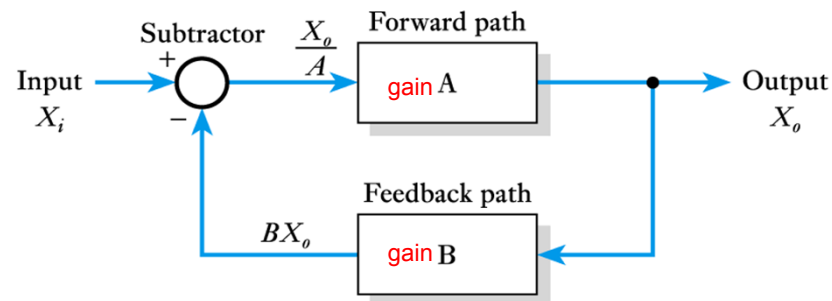
## Key points Chapter 15- Control and feedback

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- Feedback is used in almost all automatic control systems
- Feedback can be either negative or positive
- If the gain of the forward path is  $A$ , the gain of the feedback path is  $B$  and the feedback is subtracted from the input then

$$G = \frac{A}{1 + AB}$$

- If  $AB$  is positive and much greater than 1, then  $G \approx 1/B$
- Negative feedback can be used to overcome problems of variability within active amplifiers
- Negative feedback can be used to increase bandwidth, and to improve other circuit characteristics

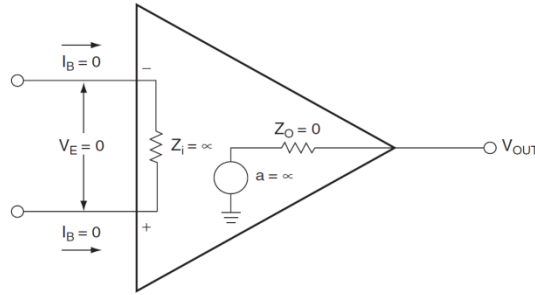


$$G = \frac{X_o}{X_i} = \frac{A}{1 + AB}$$

- Effects of the product  $AB$ 
  - If  $AB$  is negative
    - If  $AB$  is negative and less than 1,  $(1 + AB) < 1$
    - In this situation  $G > A$  and we have **positive feedback**
  - If  $AB$  is positive
    - If  $AB$  is positive then  $(1 + AB) > 1$
    - In this situation  $G < A$  and we have **negative feedback**
    - If  $AB$  is positive *and*  $AB \gg 1$

$$G = \frac{A}{1 + AB} \approx \frac{A}{AB} = \frac{1}{B}$$

- gain is independent of the gain of the forward path  $A$



– negative feedback can either *increase* or *decrease* the input or output resistance depending on how it is used.

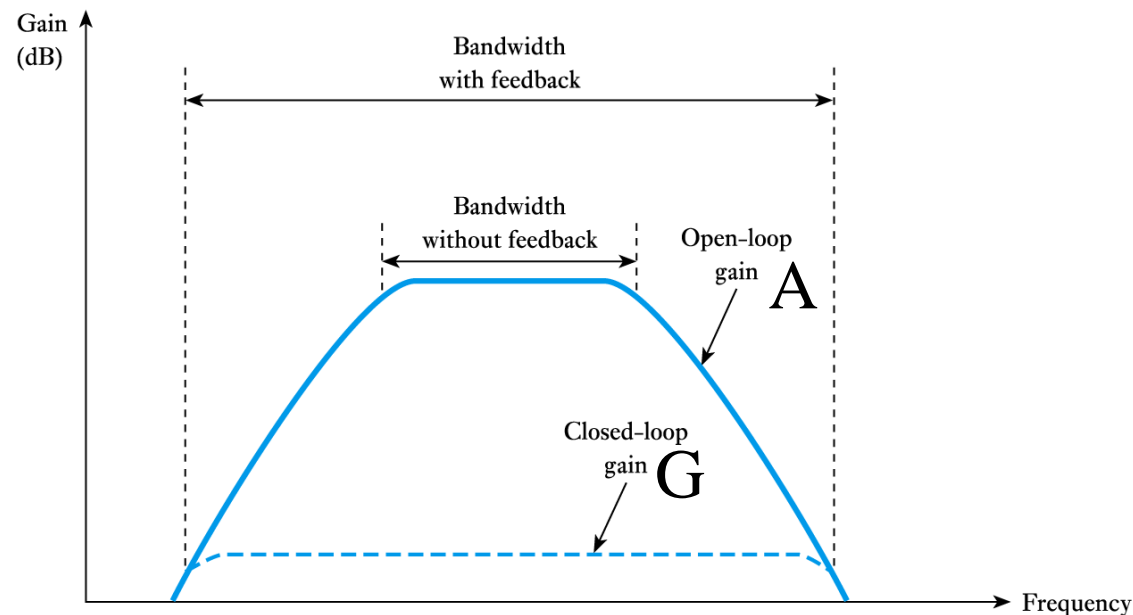
- if the output **voltage** is fed back this tends to make the output voltage more stable by *decreasing* the output resistance

Not  
covered

- if the output current is fed back this tends to make the output current more stable by *increasing* the output resistance
- if a **voltage** related to the output voltage is subtracted from the input voltage this *increases* the input resistance
- if a **current** related to the output voltage is subtracted from the input current this *decreases* the input resistance
- the factor by which the resistance changes is  $(1 + AB)$ 
  - Looking towards  $R_{in}$  from the source, or  $R_{out}$  from the load parallel paths lower effective impedance but series paths raise effective impedance

3.29

- therefore the bandwidth *increases* as the gain is *reduced* with feedback
- in some cases the **gain x bandwidth = constant**



3.30



15.7

## Negative feedback – a summary

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- All negative feedback systems share some properties
  1. They tend to maintain their output independent of variations in the forward path or in the environment
  2. They require a forward path gain that is greater than that which would be necessary to achieve the required output in the absence of feedback
  3. The overall behaviour of the system is determined by the nature of the feedback path

3.31

# Key points Chapter 16-Operational amplifiers

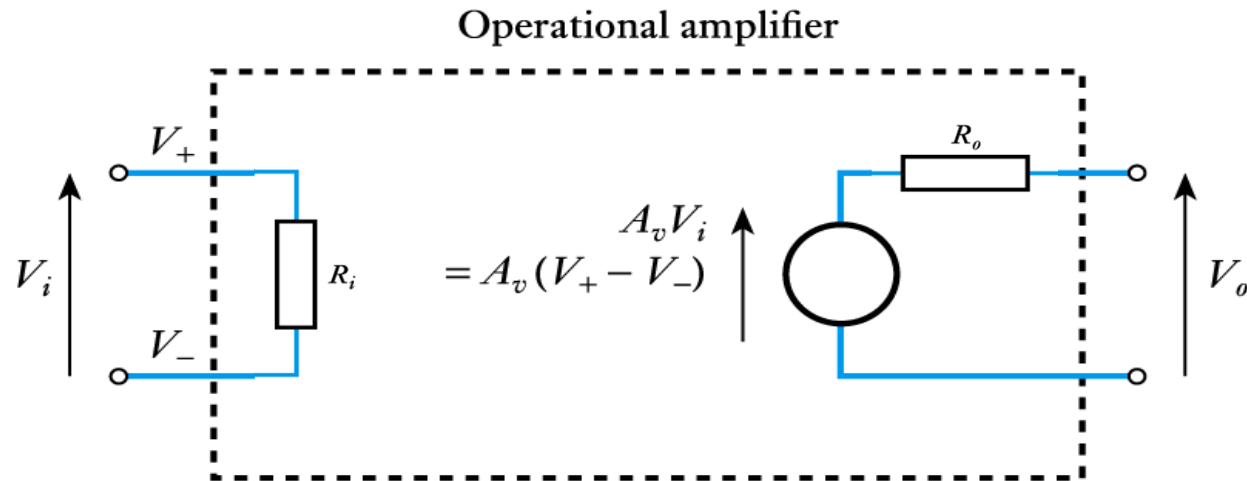
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- Operational amplifiers are among the most widely used building blocks in electronic circuits
- An *ideal* operational amplifier would have infinite voltage gain, infinite input resistance and zero output resistance
- Real op-amps have several non-ideal characteristics However, if we choose components appropriately this should not affect the operation of our circuits
- Feedback allows us to increase bandwidth by trading gain against bandwidth
- Feedback also allows us to alter other circuit characteristics



## An Real operational amplifier

- An *ideal* op-amp would be an ideal voltage amplifier and would have:  $A_v = \infty$ ,  $R_i = \infty$  and  $R_o = 0$
- A *real* op-amp typically has:  
 $A_v = 10^5$ - $10^9$ ,  $R_i = 10^6 \Omega$  (bipolar),  $10^9$ - $10^{12} \Omega$  (FET) and  
 $R_o = 10^2$ - $10^3 \Omega$



# Basic operational amplifier circuits

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- Two Basic Rules

1)An Op-Amp will do whatever is necessary with its output to adjust the voltage at its inverting input so that it is equal to the voltage at its non-inverting input. I.e. make the voltage difference between its inputs equal to zero.

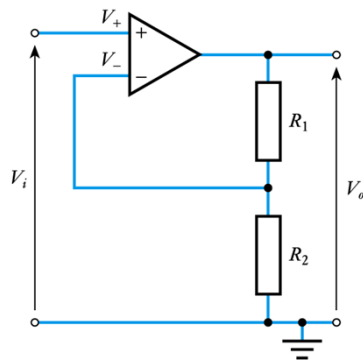
2)Op-Amp inputs draw virtually no current (0.2nA to fA). (*For an ideal op-amp  $I_{in} = 0$* )

Horowitz, Paul and Hill, Winfred, The Art of Electronics, Cambridge University Press, 1980

Neil Storey, *Electronics: A Systems Approach*, 5<sup>th</sup> Edition © Pearson Education Limited 2013

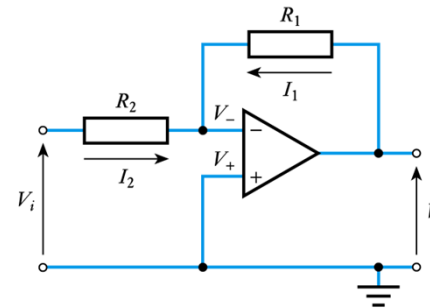
# Amplifier Circuits

Analyses using ideal op amp valid if:  
 gain of circuit  $\ll$  open-loop gain of op-amp  
 input resistance of op-amp  $\gg$  external input resistors  
 output resistance of op-amp  $\ll$  external output resistor  
 Generally we use external resistors in the range 1 to 100 k $\Omega$



Non-inverting amplifier

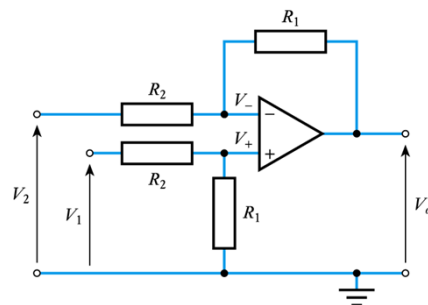
$$G = \frac{V_o}{V_i} = \frac{R_1 + R_2}{R_2}$$



Inverting amplifier

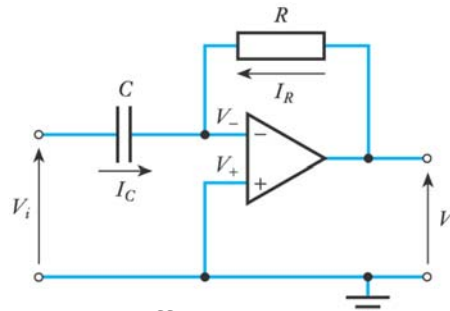
$$G = \frac{V_o}{V_i} = -\frac{R_1}{R_2}$$

Should know how to analyse the amplifiers above  $\uparrow$   
 And be familiar with the results of those below  $\downarrow$



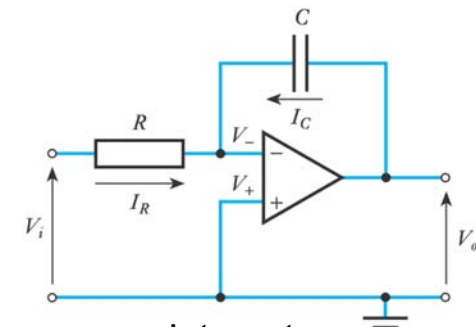
Differential amplifier

$$V_o = (V_1 - V_2) \frac{R_1}{R_2}$$



Differentiator

$$V_o = -RC \frac{dV_i}{dt}$$

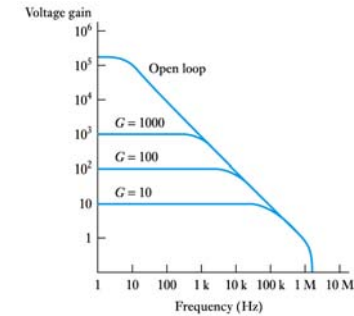


Integrator

$$V_o = -\frac{1}{RC} \int_0^t V_i dt$$

16.35

# Effects of feedback on op-amp circuits



- negative feedback *reduces* **gain** from  $A$  to  $A/(1 + AB)$
- But **gain** becomes independent of the op-amp properties
  - If the open-loop gain is much greater than the closed-loop gain (that is,  $A \gg 1/B$ )
- gain *reduced*  $\Rightarrow$  **bandwidth** *increased* by a factor  $(1+AB)$ 
  - If  $\text{Gain} \times \text{Bandwidth} \approx \text{constant}$
- If feedback applied in parallel at input/output
  - Input/output **impedance** reduced by  $(1+AB)$
- If feedback applied in series at input/output
  - Input/output **impedance** increased by  $(1+AB)$

## Key points Chapter 17: Semiconductors and diodes

---

- Diodes allow current to flow in only one direction
- Doping of semiconductors leads to the production of  $p$ -type and  $n$ -type materials
- A junction between  $p$ -type and  $n$ -type semiconductors has the properties of a diode
- Silicon semiconductor diodes approximate the behaviour of ideal diodes but have a conduction voltage of about 0.7 V

# Doping of semiconductors

---

- **Pure semiconductors**

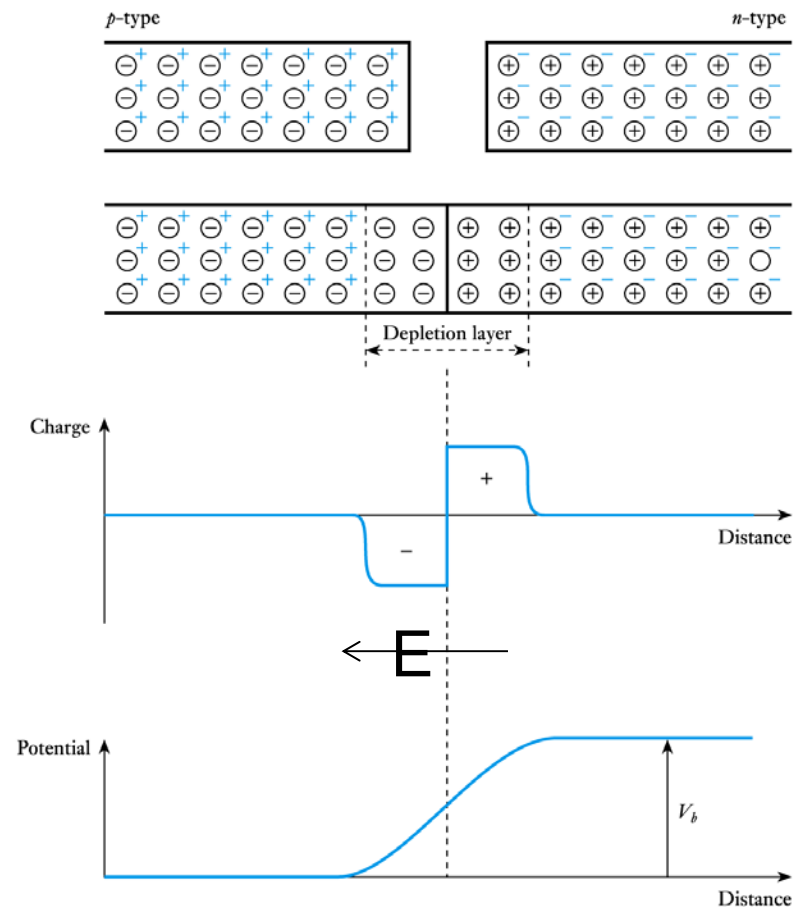
- Electrons freed by thermal motions are **negative charge carriers**
- Holes left behind that accept adjacent electrons are **positive charge carriers**
- Few charge carriers at room temperature  $\Rightarrow$  poor conductors under **intrinsic conduction**

- **Doping**

- the addition of small amounts of impurities drastically affects its properties
- some materials form an excess of *electrons* and produce an ***n*-type semiconductor** and the electrons are the **majority carrier**
- some materials form an excess of *holes* and produce a ***p*-type semiconductor** and the holes are the **majority carrier**
- both *n*-type and *p*-type materials are neutral but have much greater conductivity than pure semiconductors
- this is **extrinsic conduction**

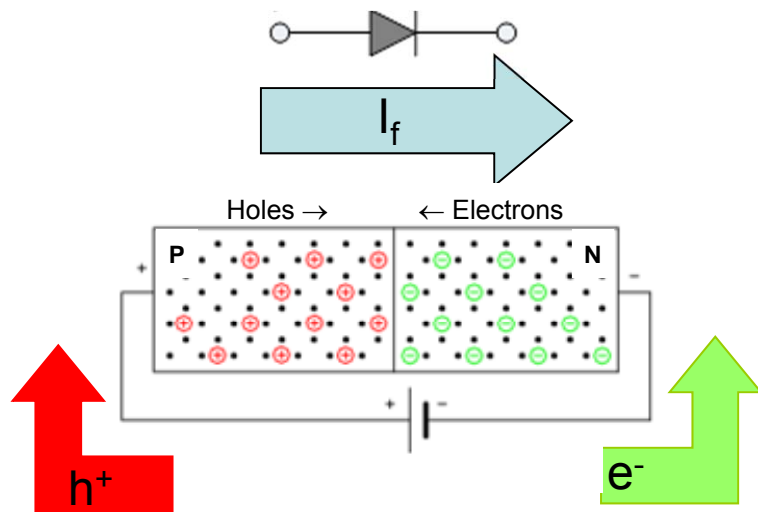
# *p*-type and *n*-type materials joined to form *pn* junction

- Majority charge carriers diffuse across (**diffusion current**) and recombine leaving the ionized dopants behind
- The dopants have opposite charge, resulting in an Electric Field or **potential barrier** across the junction.
- This impedes the diffusion of further charge carriers
- The result is a **depletion** or **space charge layer** with intrinsic conduction
- Thermally generated charge pairs swept by  $\bar{E}$  producing **drift current** that is balanced by diffusion current so  $I_{\text{net}}=0$



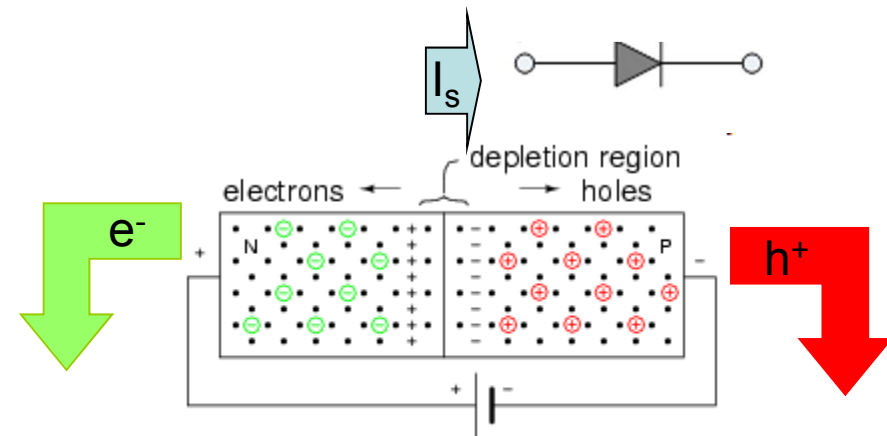
17.39

# Biasing of the p-n junction



## **Forward battery bias:**

- pushes  $h^+$  into p side,  $e^-$  into n side
- this repels other majority carriers toward junction,
- recombination there results in battery current.
- reduces the potential barrier in diode and current flows



## **Reverse battery bias:**

- attract majority carriers to battery terminal away from junction.
- Depletion region thickness increases.
- No sustained battery current flows
- Increases potential barrier in diode
- Only random thermal events supply  $I_s$



- Thus,

$$I \approx I_s \left( \exp \frac{eV}{kT} - 1 \right)$$

at room temperature  $e/kT \sim 40 \text{ V}^{-1}$

- If  $V > +0.1 \text{ V}$ ,

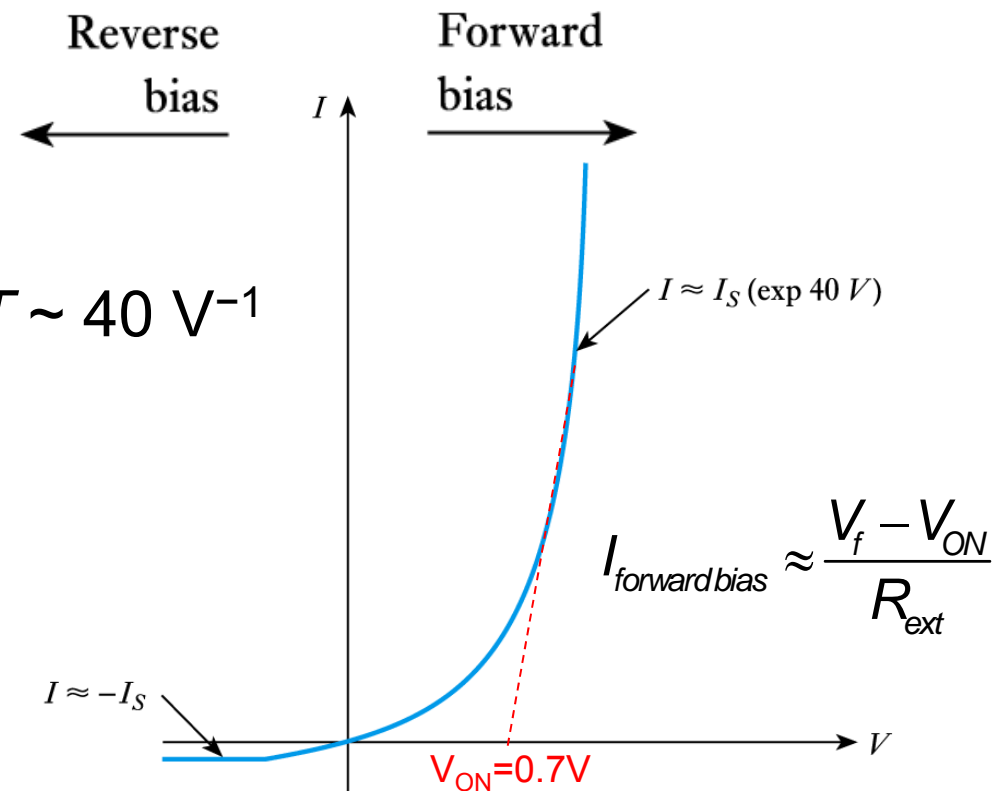
$$I \approx I_s \left( \exp \frac{eV}{kT} \right) = I_s (\exp 40 V)$$

- If  $V < -0.1 \text{ V}$ ,

$$I \approx I_s (0 - 1) = -I_s$$

–  $I_s$  is the **reverse saturation current**

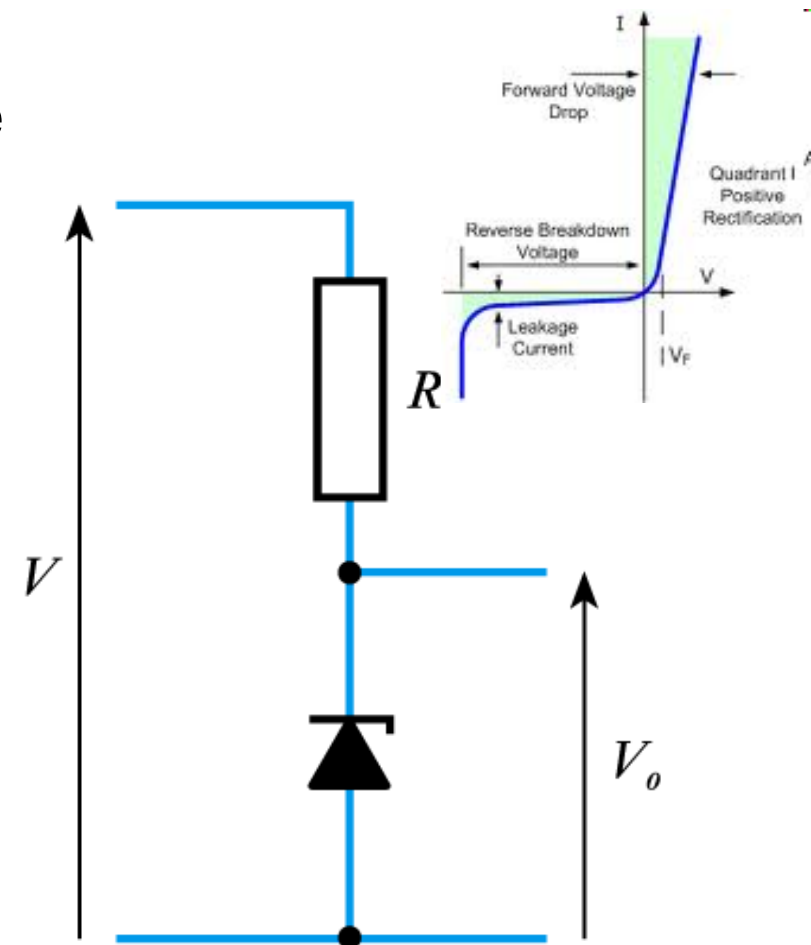
That is, our drift or thermal current,  $I_s$



# Special-purpose diodes

## ■ Zener diodes

- the relatively constant reverse breakdown voltage produces a voltage reference
- breakdown voltage is called the **Zener voltage**,  $V_Z$
- As long as  $V - I \cdot R > V_Z$  output voltage of circuit is equal to  $V_Z$  despite variations in  $V$
- a resistor is used to **limit the current** in the diode
- Understand example 17.3 in book



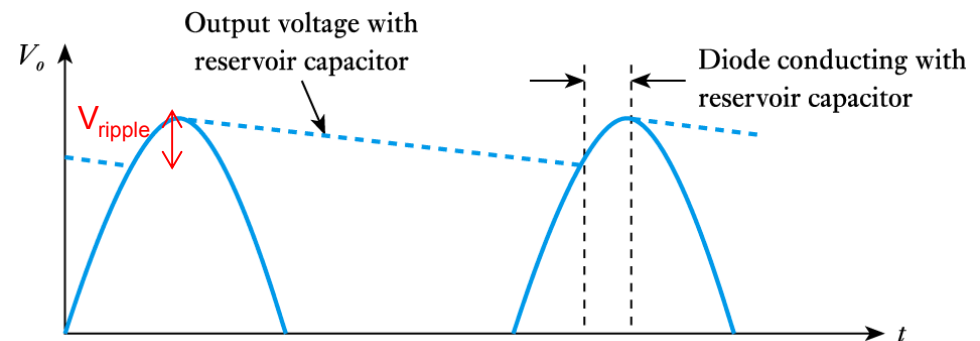
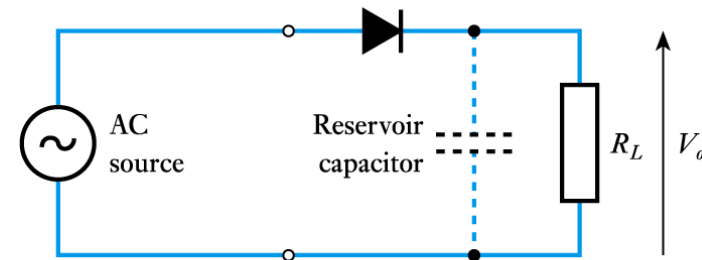
.7.42



# Diode circuits to be familiar with

Video 17A 17.8

- Half-wave rectifier
  - Full-wave rectifier
  - Voltage doubler
  - Signal rectifier
  - Signal clamper
- 
- Know how the output wave form is generated by circuit



Example: Half-wave rectifier

17.43

# Key points Chapter 18

## Field-effect transistors

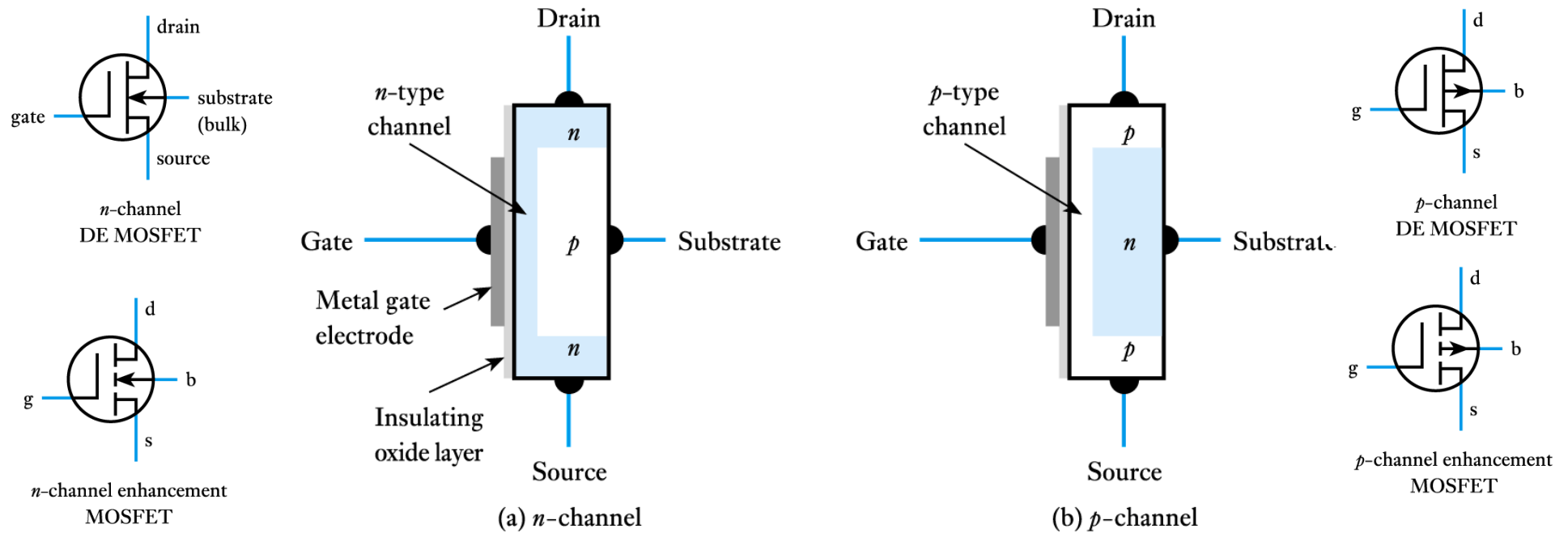
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- FETs are widely used in both analogue and digital circuits
- They have high input resistance and small physical size
- There are two basic forms of FET: MOSFETs and JFETs
- MOSFETs may be divided into DE and Enhancement types
- In each case the gate voltage controls the current from the drain to the source
- The characteristics of the various forms of FET are similar except that they require different bias voltages
- AC analysis requires equivalent circuit
  - $V_{DS}$  coupled to ground by capacitance

# DE-MOSFET

## ■ Construction

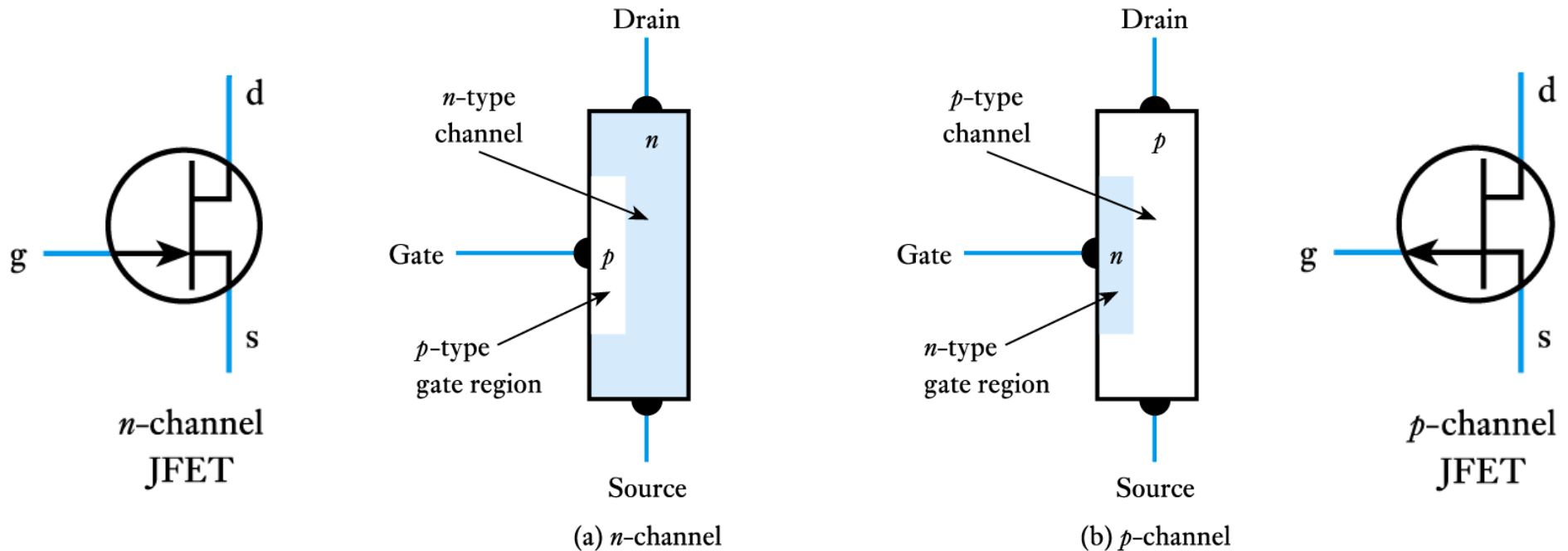
– two polarities:  $n$ -channel and  $p$ -channel



# JFET

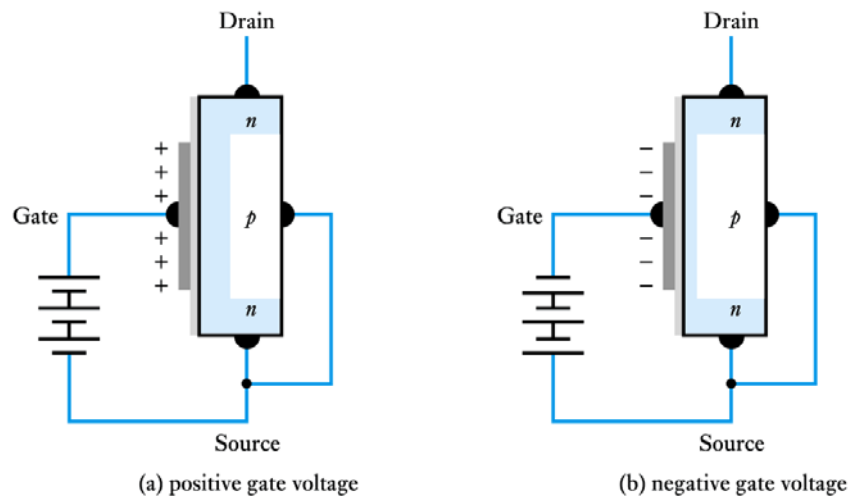
## ■ Construction

– two polarities:  $n$ -channel and  $p$ -channel

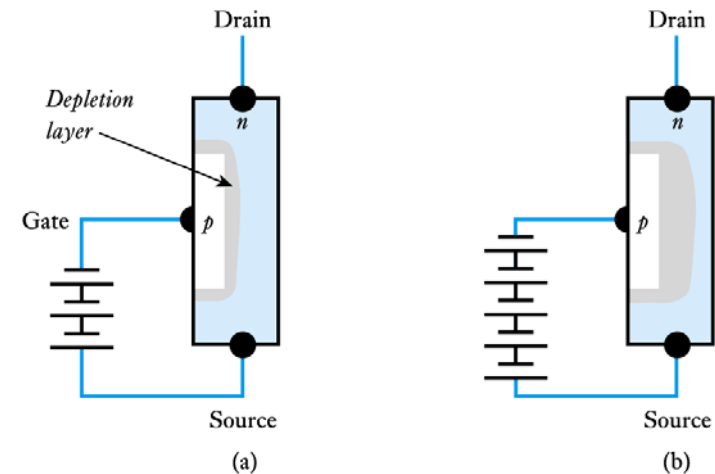


## Gate voltage controls drain to source current

- the effect of varying the gate **voltage** (n-channel device)



### DE-MOSFET

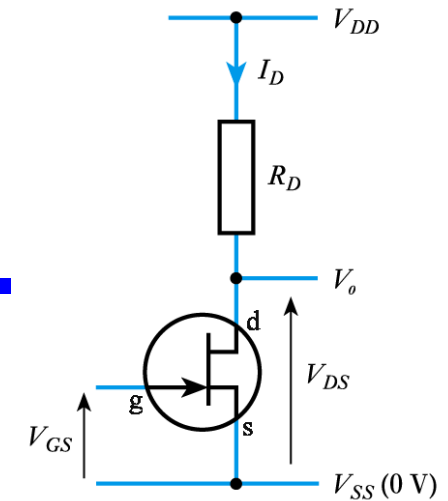


### JFET

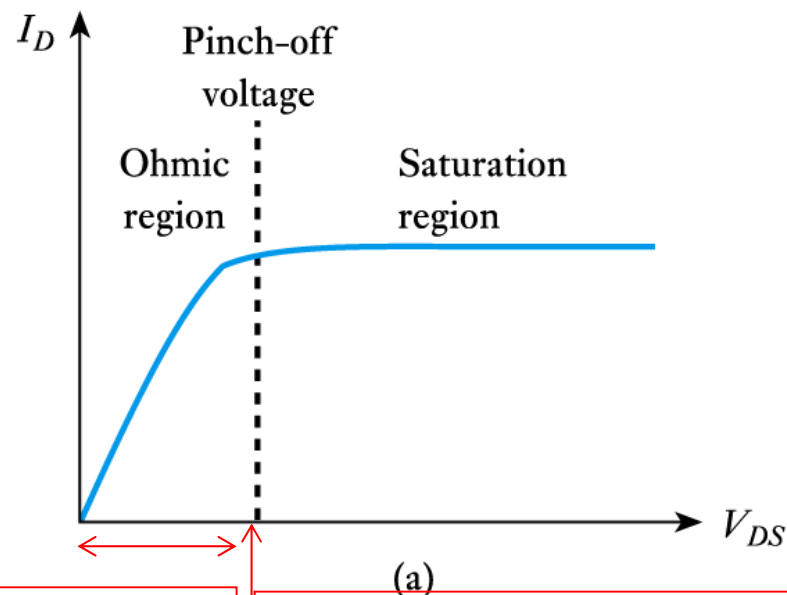
- The greater the reverse bias, the narrower the conduction channel and the lower the drain-source current
- MOSFET  $V_{Bias}$  can be  $\pm$ , JFET just reverse (-) bias.

17.47

Need to set a DC (quiescent) operating point for the small signal (AC) variations of  $v_{gs}$   
 Know why this point should avoid the Ohmic, High  $I_D$  and High  $V_{DS}$  regions

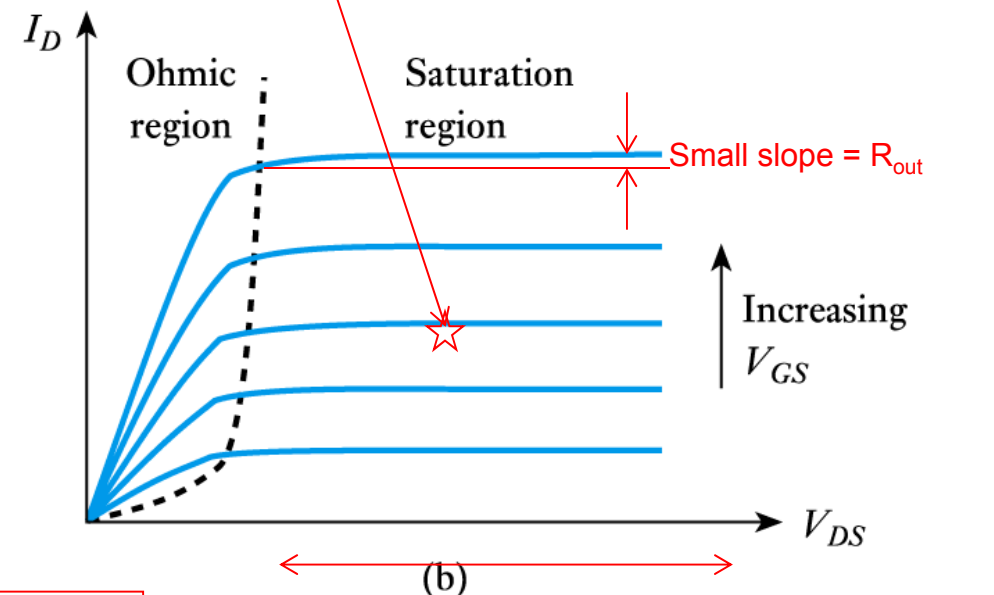


## ■ FET output characteristics



Here channel has resistance set by  $V_{GS}$

Above here the channel thickness is  $\approx 0$  at drain  
 More  $V_{DS}$  gives no more current



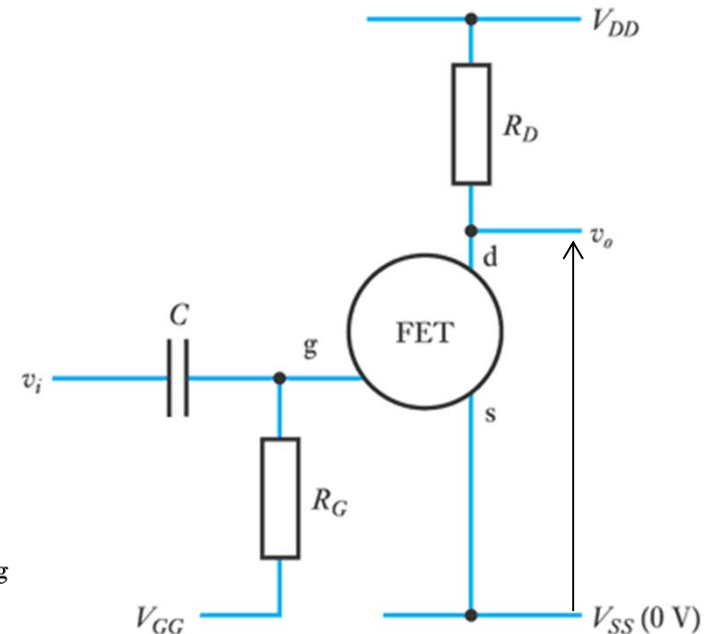
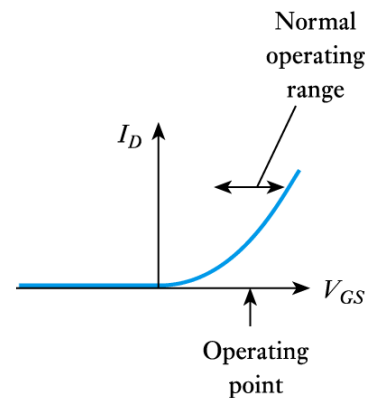
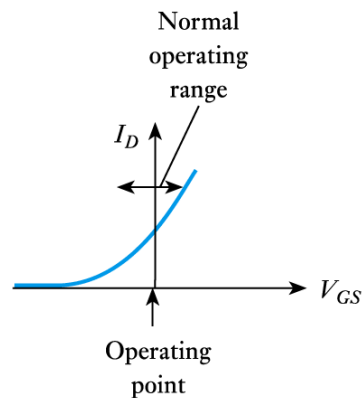
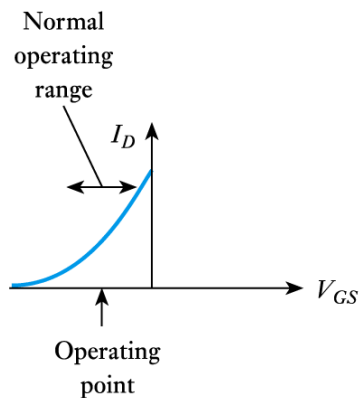
Here  $I_D \sim$  independent of the applied voltage & controlled by  $V_{GS}$

17.48



# Quiescent (DC) bias of FET transistor

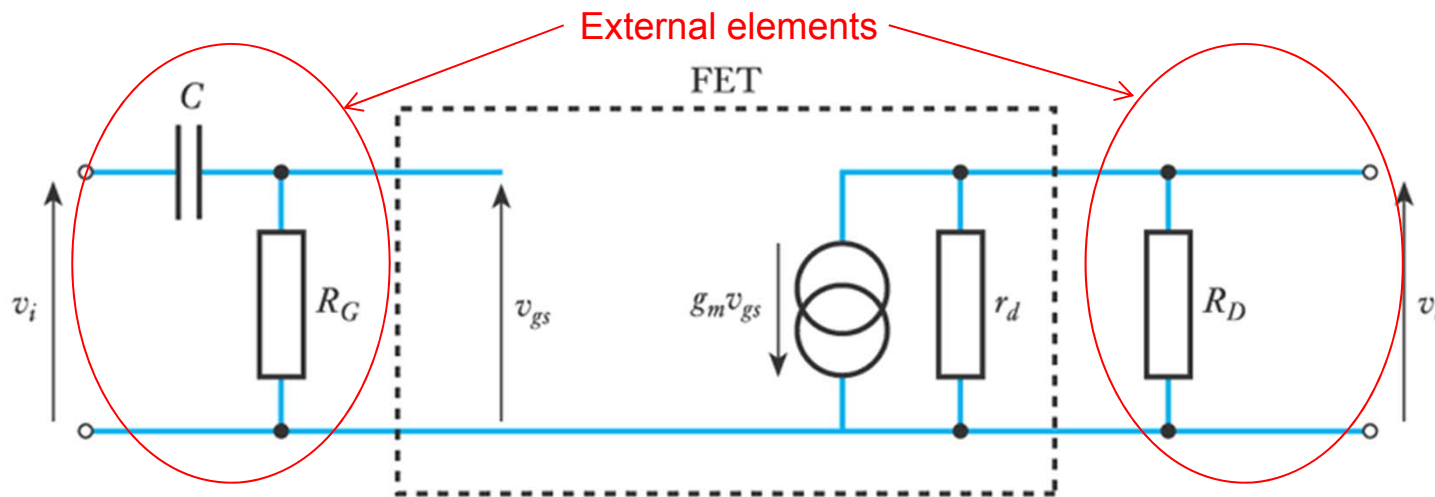
- Set a DC  $V_{GG} \Rightarrow V_{GG} = V_{GS}$
- $V_{GS}$  sets  $I_{D(\text{quiescent})}$
- $V_{o(\text{quiescent})} = V_{DD} - R_D \cdot I_{D(\text{quiescent})}$
- DC-bias sets operating point for AC signals





Video 18B

# AC or small signals must use Equivalent circuit of a FET amplifier



- This is a **small signal-equivalent circuit**
- Note that  $R_D$  goes to *ground*, since the supply voltage  $V_{DD}$  is a virtual earth point for small signals (AC) that see capacitance as a path to ground!

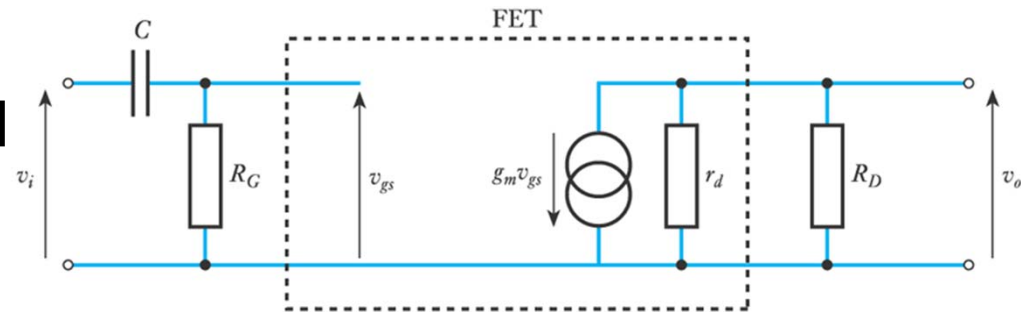
- Transconductance of a given amplifier:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

17.50

# AC or small signals gain-open loop (no feedback)

- In many cases  $r_d \gg R_D$  so  $r_d$  can often be ignored
- If this is the case



$$\text{voltage gain} = \frac{v_o}{v_i} \approx -g_m R_D$$

$$r_i \approx R_G$$

$$r_o \approx R_D$$



Video 18C

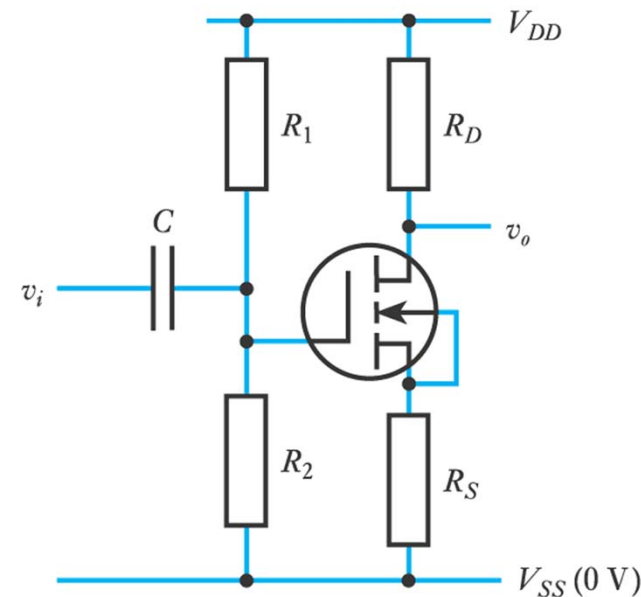
## A negative feedback amplifier

- Feedback can be used not only to stabilise the biasing conditions of a circuit, but also its voltage gain
- Analysis of equivalent circuit gives:

$$\text{voltage gain} = \frac{v_o}{v_i} \approx -\frac{R_D}{R_S}$$

$$r_i \approx R_1 \parallel R_2$$

$$r_o \approx R_D$$



– characteristics set by stable passive components

17.52

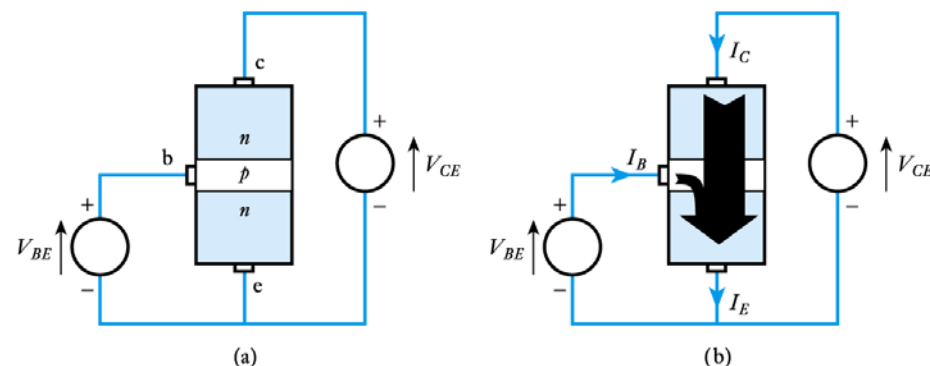
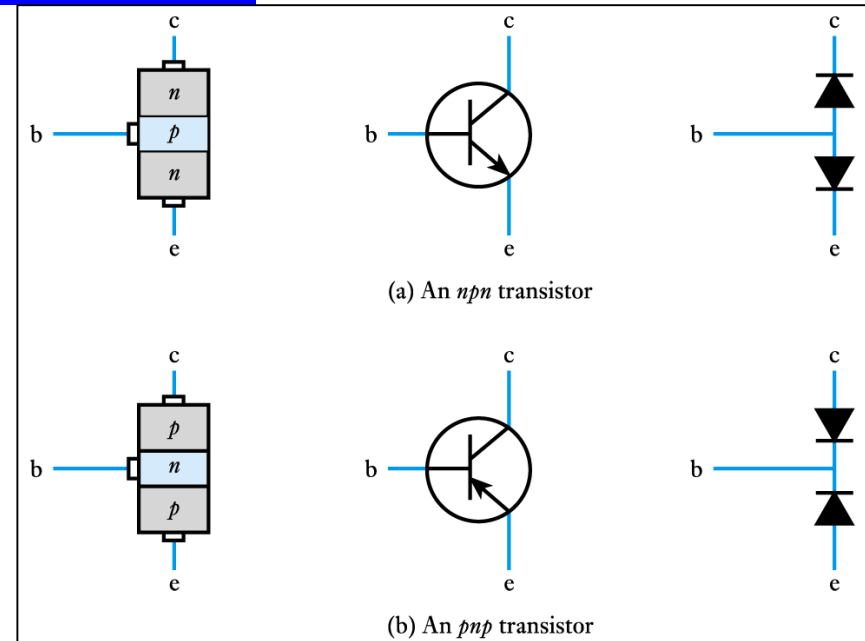
## Key points Chapter 19- Bipolar junction transistors

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- Bipolar transistors are widely used in both analogue and digital circuits
- They can be considered as either voltage-controlled or current-controlled devices
- Their characteristics may be described by their gain or by their transconductance
- Feedback can be used to overcome problems of device variability
- Again, must set DC (quiescent) bias, and use equivalent circuit to calculate small-signal (AC-signal) gain

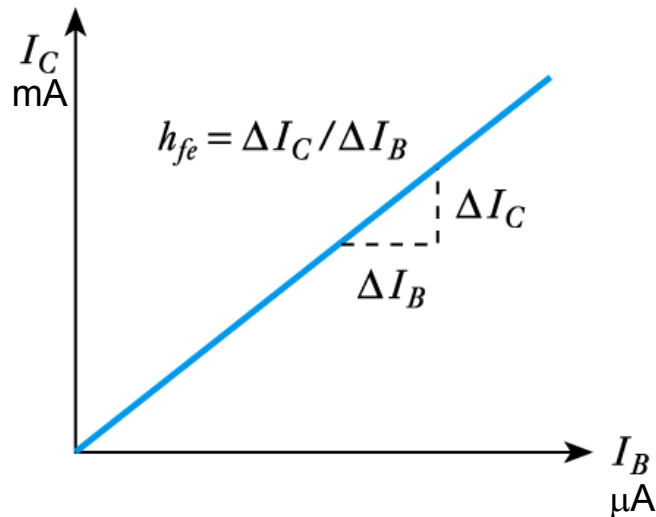
small-lightly doped base  $\Rightarrow$  most electrons from emitter get into collector-base depletion region and are swept through to collector. Thus, small base current  $I_B$  controlling  $I_C$

- Two *pn* junctions
- two polarities:  
*npn* and *pnp*
  - collector (c)
  - base (b)
  - emitter (e)
- The base is the control input:
  - b-e forward bias
  - b-c reverse bias
  - Small  $I_B \Rightarrow$  large  $I_C$



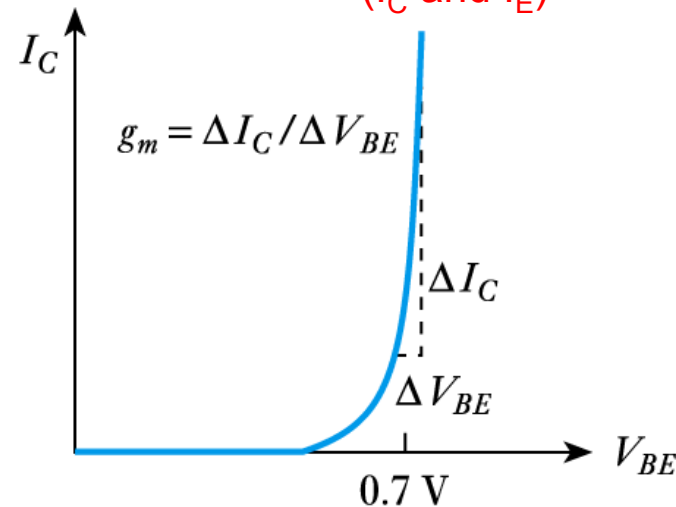
- Behaviour can be described by the **current gain,  $h_{fe}$**  or by the **transconductance,  $g_m$**  of the device

The AC gain of the device  
 $i_c = h_{fe} \cdot i_b$  ( $I \Rightarrow DC, i \Rightarrow AC, \text{ or } \Delta I$ )



(a) Relationship between output current and input current

Looks like a diode since  $I_C$  is  $\approx$  linear with  $I_B$ !  
 Note  $g_m$  depends on where device is operated ( $I_C$  and  $I_E$ )

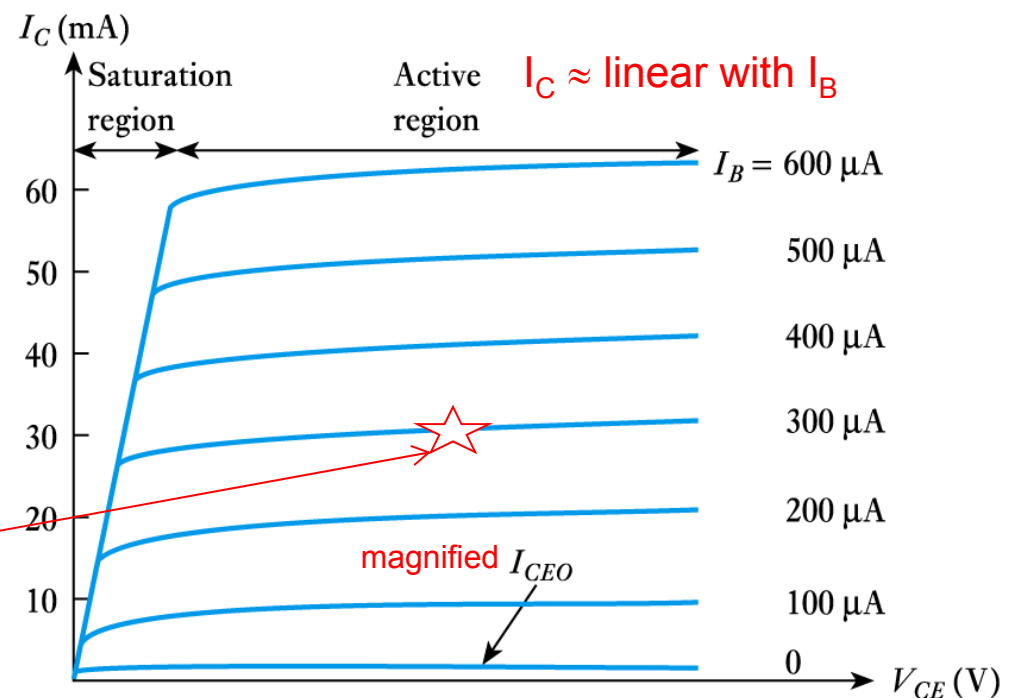


(b) Relationship between output current and input voltage

## ■ Output characteristics

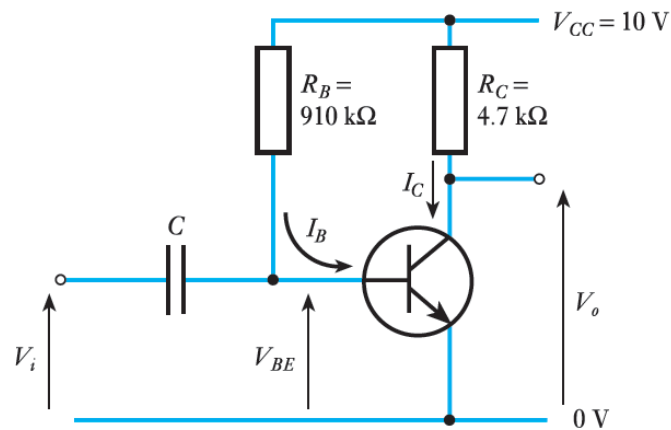
- region near to the origin is the **saturation region**
- this is normally avoided in linear circuits by selecting DC-operating point
- slope of lines represents the **output resistance**

Typical operating point  
Why in this region?





# bipolar transistor-no feedback



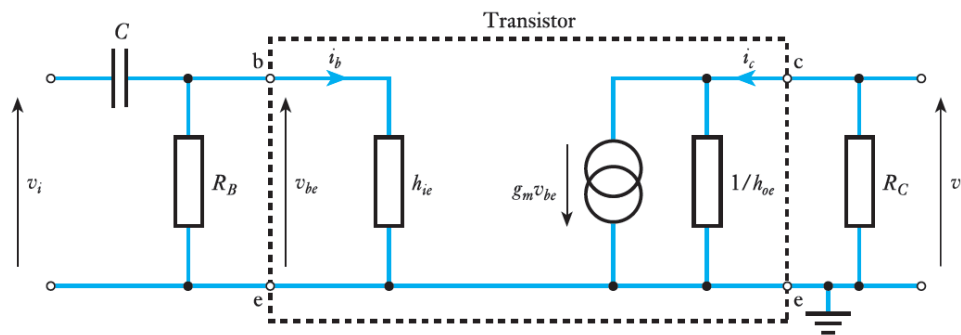
## DC-Quiescent bias

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_C = h_{FE} I_B$$

$$V_o = V_{CC} - I_C R_C$$

Depends on device characteristics



$$\frac{v_o}{v_i} = -g_m \cdot \frac{R_C}{h_{oe} \cdot R_C + 1}$$

$$r_i = \frac{h_{ie}}{\frac{h_{ie}}{R_B} + 1}$$

$$r_o = \frac{R_C}{h_{oe} \cdot R_C + 1}$$

## AC-small signal

$$R_C \ll \frac{1}{h_{oe}} \Rightarrow \frac{v_o}{v_i} \approx -g_m \cdot R_C$$

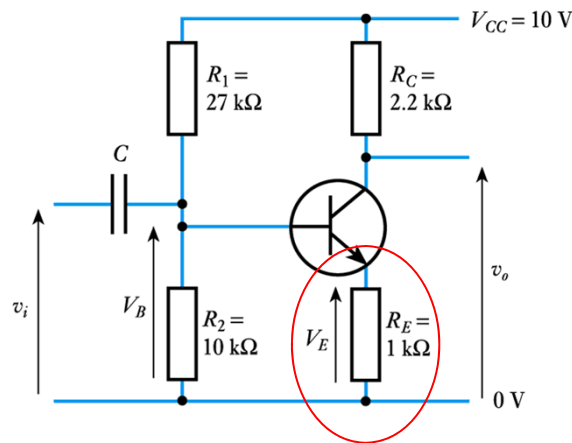
$$R_B \gg h_{ie} \Rightarrow r_i \approx h_{ie}$$

$$R_C \ll \frac{1}{h_{oe}} \Rightarrow r_o = R_C$$

17.57

# Bipolar transistor-with feedback

## DC-large signal



$$V_B \approx V_{CC} \frac{R_2}{R_1 + R_2}$$

$$V_E = V_B - V_{BE}$$

$$V_{BE} \approx \text{constant} \approx 0.7\text{V}$$

$$I_B \ll I_C \approx I_E$$

$$I_E \approx I_C = \frac{V_E}{R_E}$$

$$V_o = V_{CC} - I_C R_C$$

Gain,  $r_i$  and  $r_o$  only depend on passive components

## AC-small signal

$$\frac{v_o}{v_i} = - \frac{R_C}{R_E + \frac{1}{g_m}}$$

$$R_E \gg \frac{1}{g_m}$$

$$\Rightarrow \frac{v_o}{v_i} \approx - \frac{R_C}{R_E}$$

$$r_b = h_{ie} + (h_{fe} + 1) R_E \quad h_{fe} \cdot R_E \gg h_{ie} \gg 1 \Rightarrow r_b \approx h_{fe} \cdot R_E$$

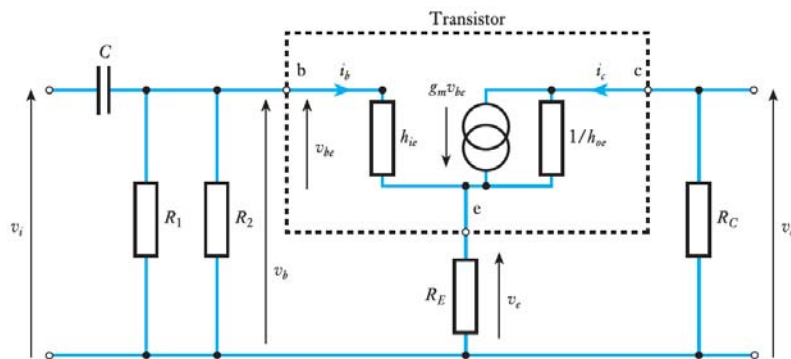
$$r_i = R_1 \parallel R_2 \parallel r_b$$

$$r_b \gg R_1 \approx R_2 \Rightarrow r_i \approx \frac{R_1 \cdot R_2}{R_1 + R_2}$$

$$r_o = R_C \parallel \left( \frac{1}{h_{oe}} + R_E \right)$$

$$R_C \ll \frac{1}{h_{oe}} + R_E \Rightarrow r_o \approx R_C$$

17.58



# Comparison of FET and Bipolar

---

	Field Effect Transistor (FET)	Bipolar Junction Transistor (BJT)
1	Low voltage gain	High voltage gain
2	High current gain	Low current gain
3	Very high input impedance	Low input impedance
4	High output impedance	Low output impedance
5	Low noise generation	Medium noise generation
6	Fast switching time	Medium switching time
7	Easily damaged by static	Robust
8	Some require an input to turn it "OFF"	Requires zero input to turn it "OFF"
9	Voltage controlled device	Current controlled device
10	Exhibits the properties of a Resistor	
11	More expensive than bipolar	Cheap
12	Difficult to bias	Easy to bias

## Key points Chapter 22-Noise

---

- Noise in electronic circuits can be of various forms, including thermal noise, shot noise,  $1/f$  noise and interference
- Both bipolar transistors and FETs suffer from noise
- Noise can be picked from radiated noise (high frequency) or poor grounding schemes (loops or serial grounding)
- Circuit layout plays a major role in determining EMC performance

# Last time: Device noise

---

- Thermal or Johnson noise  $V_{n(\text{rms})} = (4 \cdot k \cdot T \cdot R \cdot BW)^{1/2}$ 
  - Random thermal motion of charge carriers in resistive materials (both BJT and FET's)
  - Gaussian and white
- Shot noise (current noise)  $I_{n(\text{rms})} = (2 \cdot e \cdot I \cdot BW)^{1/2}$ 
  - Statistical fluctuations in the number of charge carriers flowing
  - Most apparent at low current levels
  - Source of noise in BJT transistors from low  $I_B$  flow across p-n potential barriers.
  - ~Gaussian and white
- 1/f noise
  - Variety of sources.
  - Most common is **flicker noise**, the variation of diffusion of charge carriers in devices
  - Common source of noise in FET devices
  - Power increases at low frequencies  $\Rightarrow$  “red” (6dB/octave) or “pink” (3dB/octave) noise

## Figures of merit

---

- Signal quality: Signal to noise ratio
  - Average voltage level divided by RMS noise:  $S/N \text{ ratio} = \left( \frac{V_s}{V_n} \right)$
  - Expressed in dB as:  $S/N \text{ ratio (dB)} = 20 \log_{10} \left( \frac{V_s}{V_n} \right) \text{ dB}$
  - Can get  $V_s$  by averaging input samples
- Circuit quality: Noise figure
  - Measured output RMS noise divided by  
Measured input RMS noise times the gain of the circuit:

$$NF(dB) = 20 \log_{10} \frac{\text{rms noise output voltage from amplifier}}{\text{rms noise output voltage from noiseless amplifier}}$$

## Key points Chapter 23-

# Positive feedback, oscillators and stability

- Positive feedback is used in the production of oscillators
- The requirement for oscillation is that the loop gain  $AB$  must have a magnitude of 1, and a phase shift of  $180^\circ$  (or  $180^\circ$  plus some integer multiple of  $360^\circ$ )
- This can be achieved using a circuit that produces a phase shift of  $180^\circ$  subtracted from a non-inverting amplifier's feedback (or added to an inverting amplifier's feedback)
- Alternatively, it can be achieved using a circuit that produces a phase shift of  $0^\circ$  subtracted from an inverting amplifier's feedback (or added to a non-inverting amplifier's feedback)
- For good frequency stability we often use crystals
- Care must be taken to ensure the stability of all feedback systems

# Oscillators

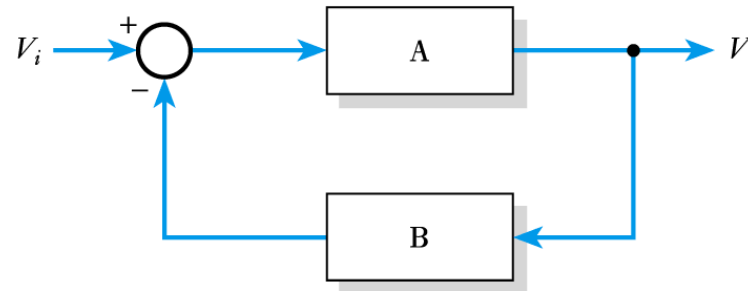


Video 23A



23.2

- Earlier we looked at a generalised feedback system



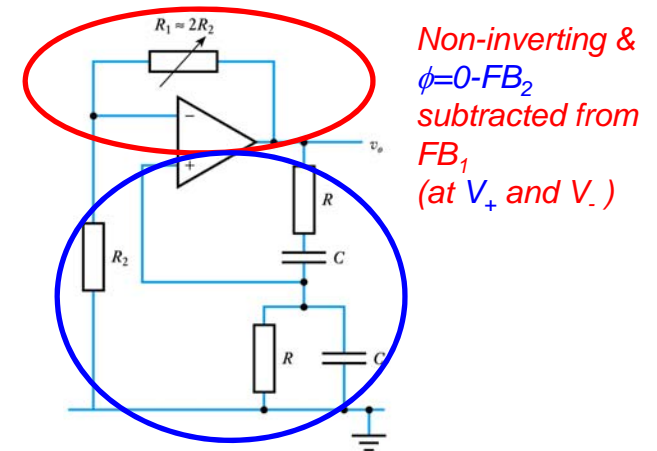
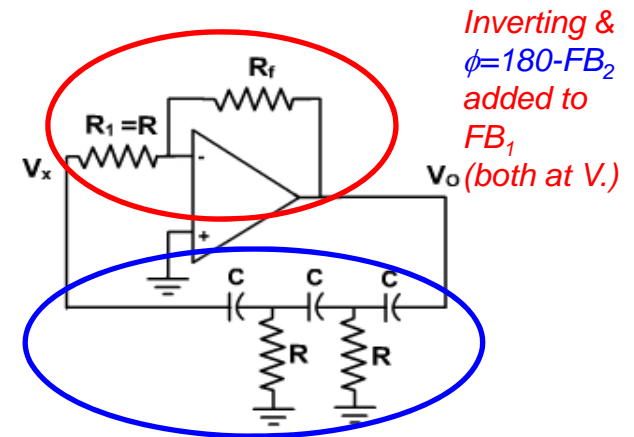
- We also derived the closed-loop gain  $G$  of this  $G = \frac{A}{(1 + AB)}$
- When  $AB = -1$ , the gain is infinite
  - this represents the condition for oscillation

17.64



# Sine-wave oscillator systems

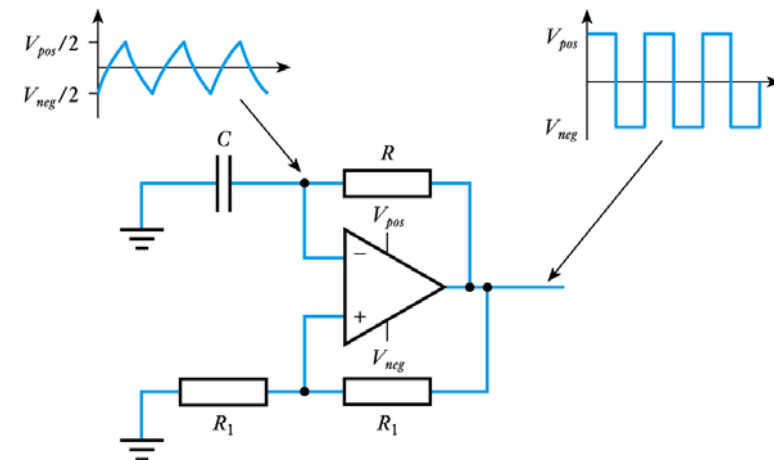
- Two feedback loops
- $FB_1$  purely resistive gain
  - $V_{fb1} = G_1 \cdot V_o$ , where  $G_1 = \text{constant}$
- $FB_2$  has  $G_2(f)$  with phase(f)
  - $V_{fb2}$  Cancels  $V_{fb1}$ , but only when  $V_o$  changes at  $f=f_o$
- Near saturation,  $V_o$  slows or stops ( $A \rightarrow 0 \Rightarrow f \rightarrow 0 \Rightarrow G_2 \rightarrow 0$ )
- $FB_2$  no longer cancels  $FB_1$  and  $V_o$  reverses



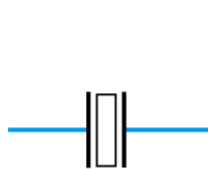


Video 23B

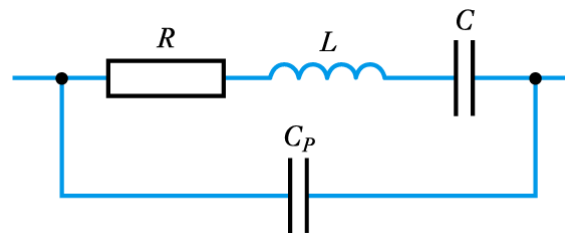
- **Digital relaxation oscillator**
  - Why  $V_{pos}/2$  in  $\Rightarrow V_{pos}$  out



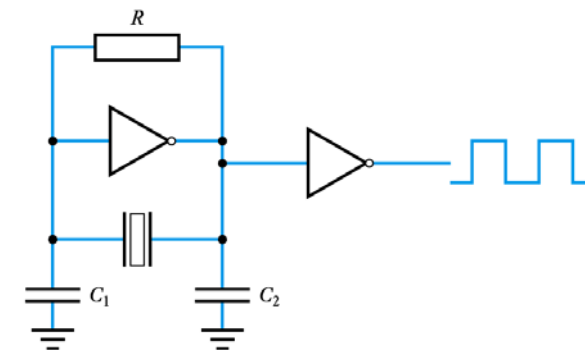
- **Crystal oscillator-piezoelectric crystals** act like resonant circuits with a very high Q – as high as 100,000



(a) Circuit symbol



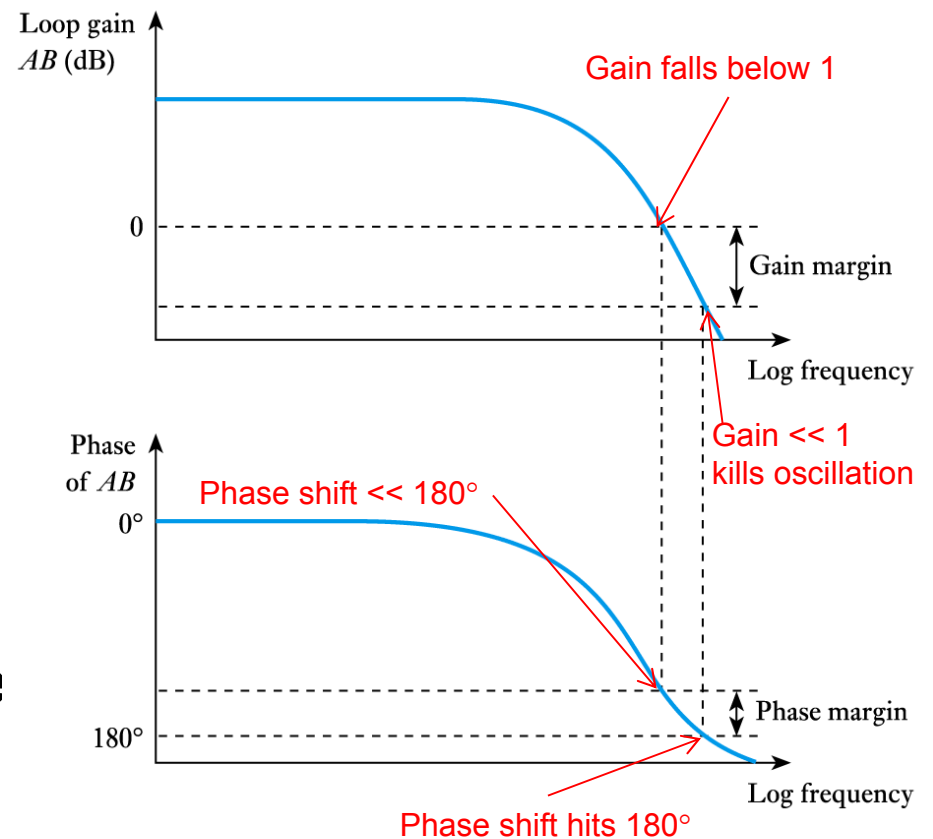
(b) Equivalent circuit



17.06

# Stability

- The gain of all real amplifiers falls at high frequencies and this also produces a phase shift
- All multi-stage amplifiers will produce  $180^\circ$  of phase shift at some frequency
- To ensure stability we must ensure that the gain falls below unity before the phase shift reaches  $180^\circ$






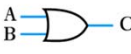
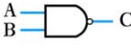
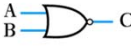


## Key points Chapter 24-Digital systems-combinational logic

---

- Logic circuits are usually implemented using logic gates
- Circuits in which the output is determined solely by the current inputs are termed combinational logic circuits
- Logic functions can be described by truth tables or using Boolean algebraic notation
- Boolean expressions can often be simplified by algebraic manipulation, or using techniques such as Karnaugh maps
- Binary digits may be combined to form digital words that can be processed using binary arithmetic

# Combinational logic building blocks

- Know the logic gates, their truth tables and their Boolean expressions
- Construct a logical function from a truth table
- Implement function with gates (e.g. gates that do:  $Y = \overline{AB} + \overline{CD}$  )
- Reverse  $\Rightarrow$  translate a gate system to a logical function
- Simplify expressions algebraically or using a Karnaugh map

Function	Symbol	Boolean expression	Truth table															
Buffer		$B = A$	<table><tr><th>A</th><th>B</th></tr><tr><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td></tr></table>	A	B	0	0	1	1									
A	B																	
0	0																	
1	1																	
NOT		$B = \bar{A}$	<table><tr><th>A</th><th>B</th></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td></tr></table>	A	B	0	1	1	0									
A	B																	
0	1																	
1	0																	
AND		$C = A \cdot B$	<table><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	A	B	C	0	0	0	0	1	0	1	0	0	1	1	1
A	B	C																
0	0	0																
0	1	0																
1	0	0																
1	1	1																
OR		$C = A + B$	<table><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	A	B	C	0	0	0	0	1	1	1	0	1	1	1	1
A	B	C																
0	0	0																
0	1	1																
1	0	1																
1	1	1																
NAND		$C = \overline{A \cdot B}$	<table><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	A	B	C	0	0	1	0	1	1	1	0	1	1	1	0
A	B	C																
0	0	1																
0	1	1																
1	0	1																
1	1	0																
NOR		$C = \overline{A + B}$	<table><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	A	B	C	0	0	1	0	1	0	1	0	0	1	1	0
A	B	C																
0	0	1																
0	1	0																
1	0	0																
1	1	0																
Exclusive OR		$C = A \oplus B$	<table><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	A	B	C	0	0	0	0	1	1	1	0	1	1	1	0
A	B	C																
0	0	0																
0	1	1																
1	0	1																
1	1	0																
Exclusive NOR		$C = \overline{A \oplus B}$	<table><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	A	B	C	0	0	1	0	1	0	1	0	0	1	1	1
A	B	C																
0	0	1																
0	1	0																
1	0	0																
1	1	1																

Example 2--Design a circuit to convert 3-bit binary numbers into Gray code



– First we produce a Truth Table

A	B	C	X	Y	Z
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Decimal	Binary	Gray code
0	0	0000
1	1	0001
2	10	0011
3	11	0010
4	100	0110
5	101	0111
6	110	0101
7	111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010

- From the truth table we produce Boolean expression and Karnaugh maps to simplify

		<i>AB</i>			
		00	01	11	10
<i>X</i>	0	0	0	1	1
<i>C</i>	1	0	0	1	1

$X = A$

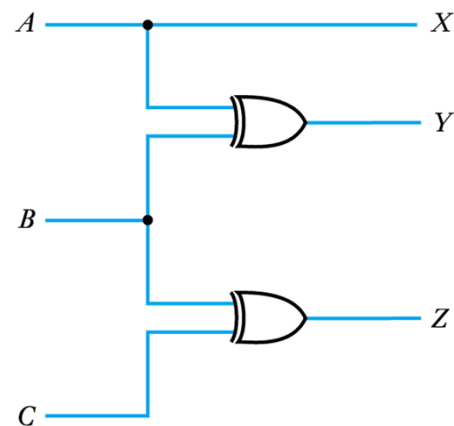
		<i>AB</i>			
		00	01	11	10
<i>Y</i>	0	0	1	0	1
<i>C</i>	1	0	1	0	1

$Y = \bar{A}B + A\bar{B} = A \oplus B$

		<i>AB</i>			
		00	01	11	10
<i>Z</i>	0	0	1	1	0
<i>C</i>	1	1	0	0	1

$Z = B\bar{C} + \bar{B}C = B \oplus C$

- and implement the circuit



# Key points Chapter 23-Sequential logic

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- Sequential logic circuits have the characteristic of memory
- Among the most important groups of sequential components are the various forms of multivibrator
  - Bistables-flip flops and latches
  - Monostables-one shots
  - Astables-digital oscillators and timers
- Know what these are and how they work (input vs. output)
- Recognize them in a circuit or logical diagram
- Be able to draw output waveforms for a given input
- Know what shift registers do and how to do serial  $\leftrightarrow$  parallel
- Know what ripple and modulo counters do and how



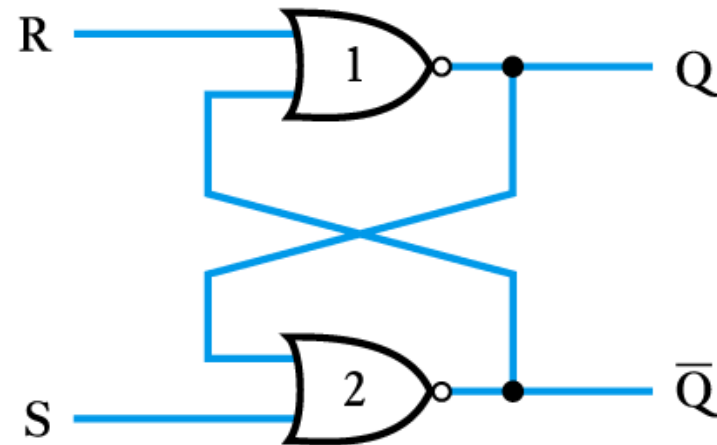
S going high sets Q to 1

R going high re-sets Q to 0

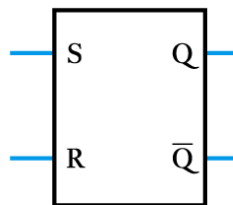
Re-setting or setting several times does not affect Q

## ■ Example 1-The S-R latch (SET-RESET latch)

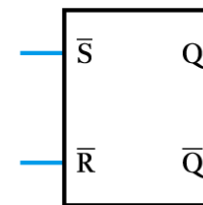
- when  $R = S = 0$ 
  - Circuit stays in current state
- when  $S = 1, R = 0$ 
  - Q is **SET** to 1 ( $\bar{Q} = 0$ )
- when  $S = 0, R = 1$ 
  - Q is **RESET** to 0 ( $\bar{Q} = 1$ )
- when  $S = 1, R = 1$ 
  - Both outputs at 0 – not allowed



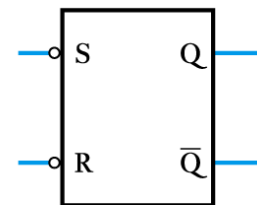
Circuit (↑) or logic diagram (↓)



(a) Active high inputs



(b) Active low inputs

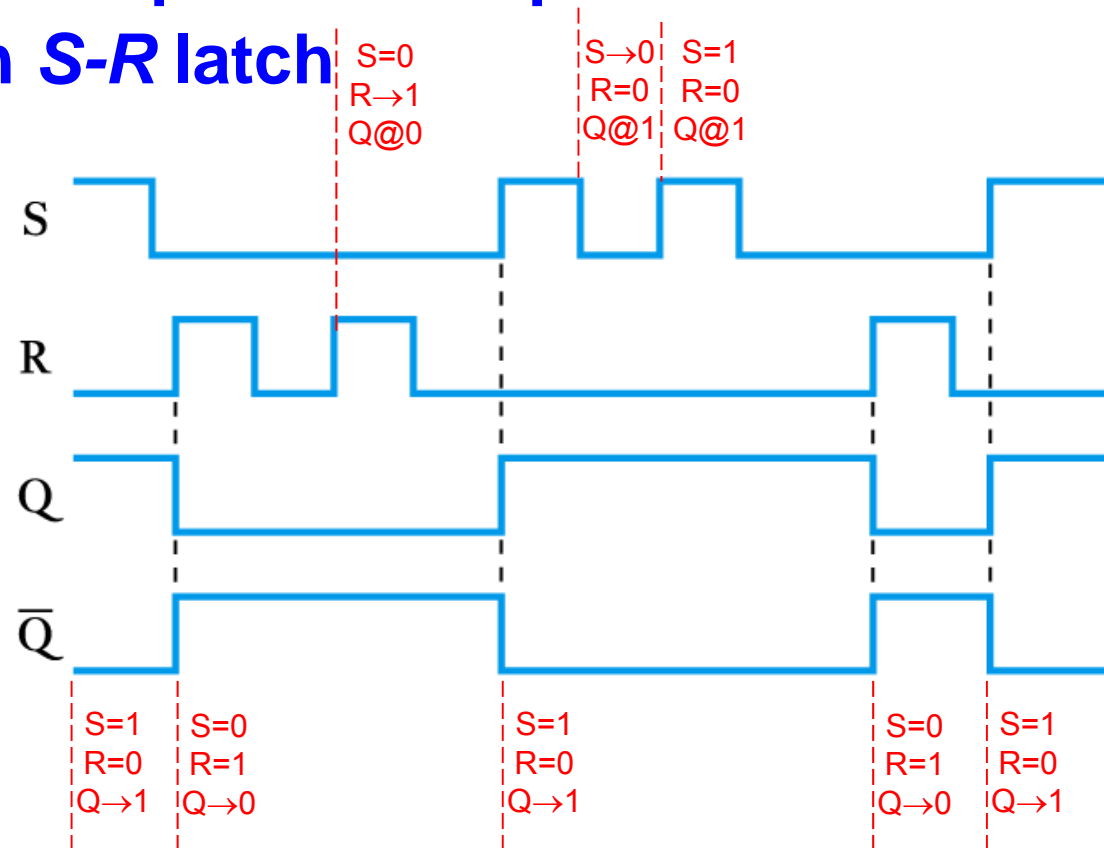


S going high sets Q to 1

R going high re-sets Q to 0

Re-setting or setting several times does not affect Q

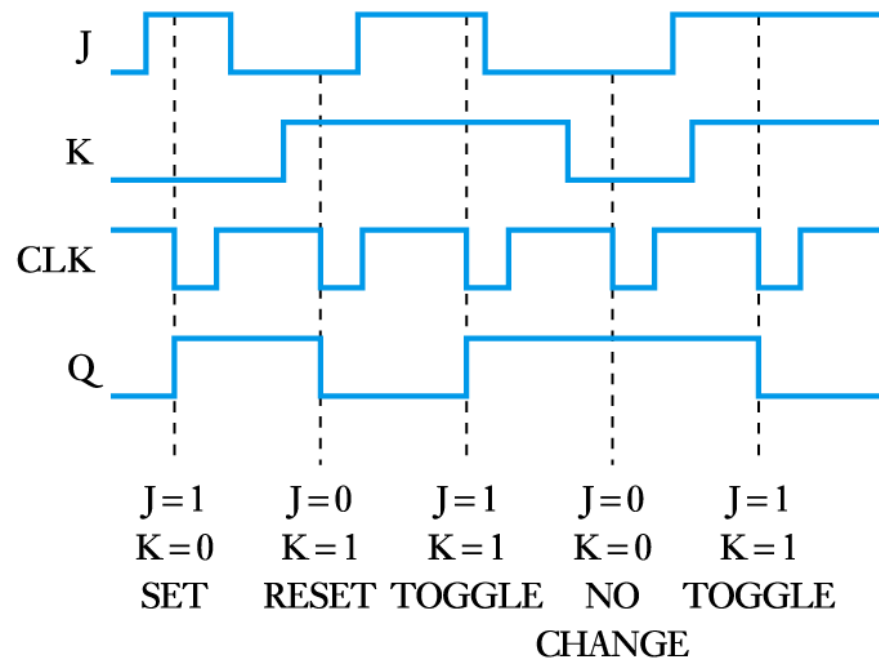
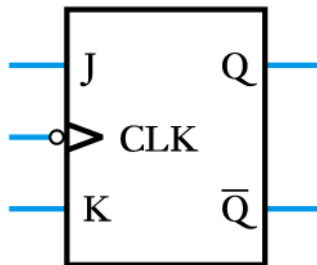
- **Sample input and output waveforms for an S-R latch**



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## ■ Example 2-The J-K flip-flop

- Similar to S-R flip-flop but *toggles* when  $J = K = 1$



(a) Logic symbol

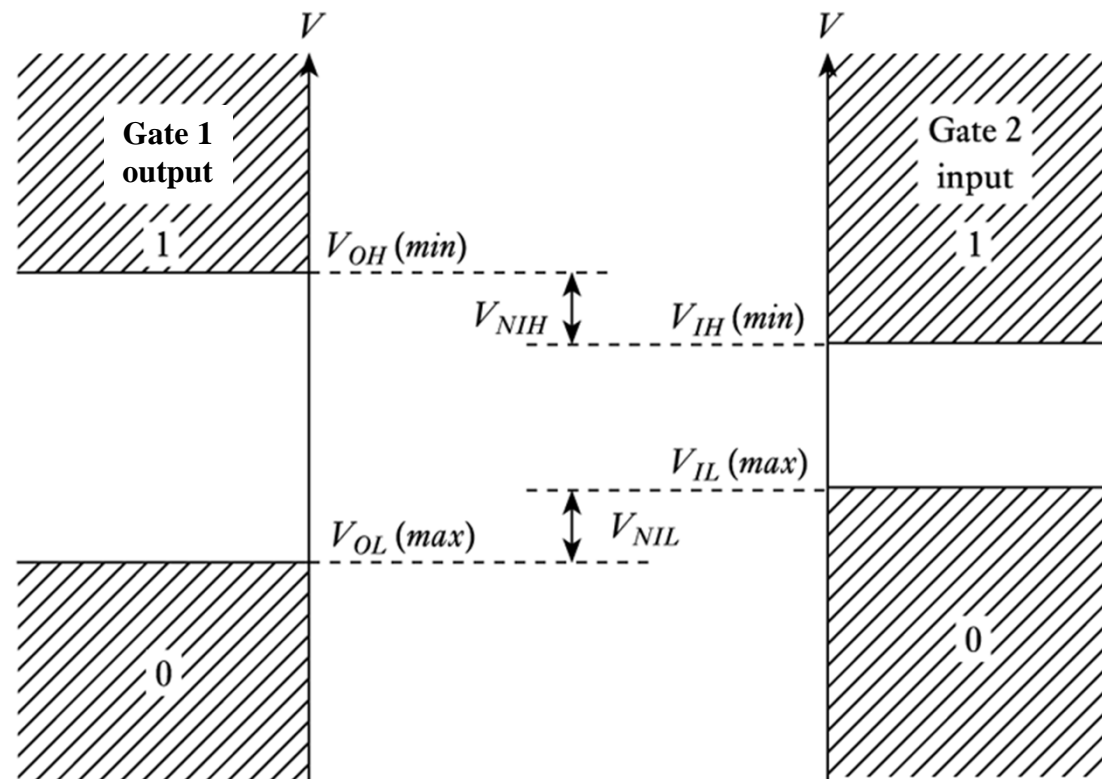
(b) Sample input and output waveforms

## Key points Chapter 24-Digital devices

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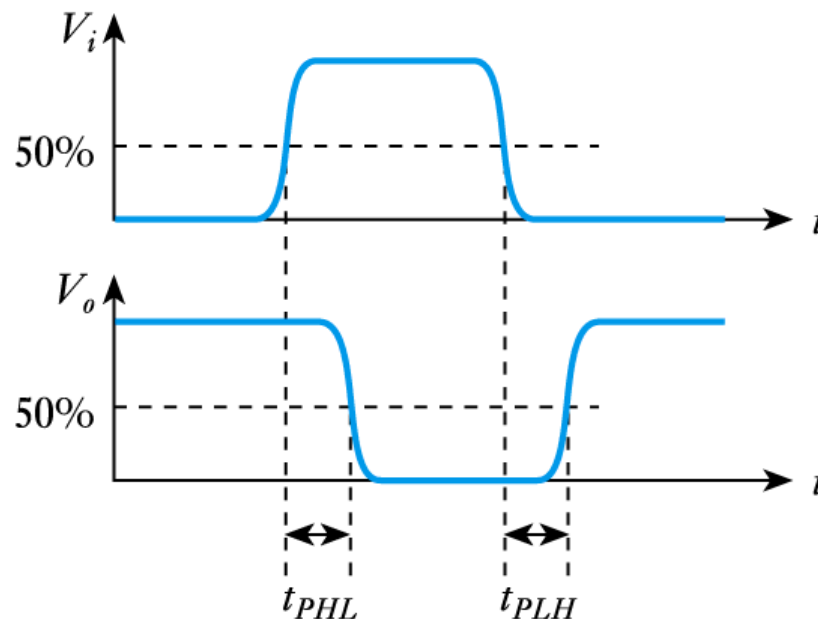
- Physical gates are not ideal components
- The ability of a gate to ignore noise is its 'noise immunity'
- All logic gates exhibit a propagation delay
- The most widely used logic families are TTL and CMOS.
  - Know general properties of each
- Interface circuitry may be needed to link devices of different families
- Noise and EMC issues must be considered during design
  - Know what to do with unused inputs

## ■ A graphical representation of noise immunity



## ■ Timing considerations

- all gates have a certain **propagation delay time**,  $t_{PD}$
- this is the average of the two switching times



$$t_{PD} = \frac{1}{2}(t_{PHL} + t_{PLH})$$

# A comparison of logic families

Transistor-Transistor (TTL) Logic (bipolar)  
Metal oxide semiconductor (MOS) logic (FET)

Know what these  
terms mean!

Parameter	TTL	CMOS
Basic gate	NAND	NAND-NOR
Fan-out	10	>50
Power per gate (mW)	1 – 22	1@1 MHz
Noise immunity	Very good	Excellent
$T_{PD}$ (ns)	.5 – 33	1.5 – 200

## Key points Chapter 25- Implementing digital systems

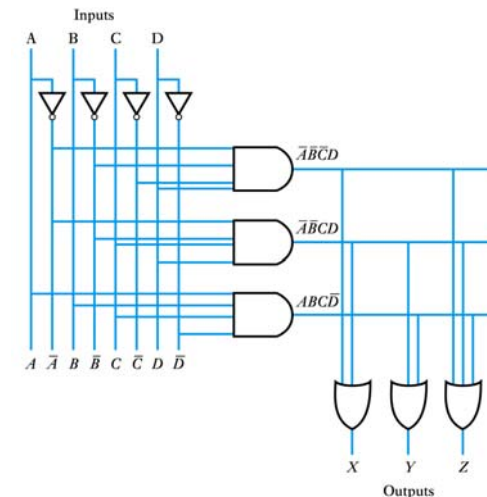
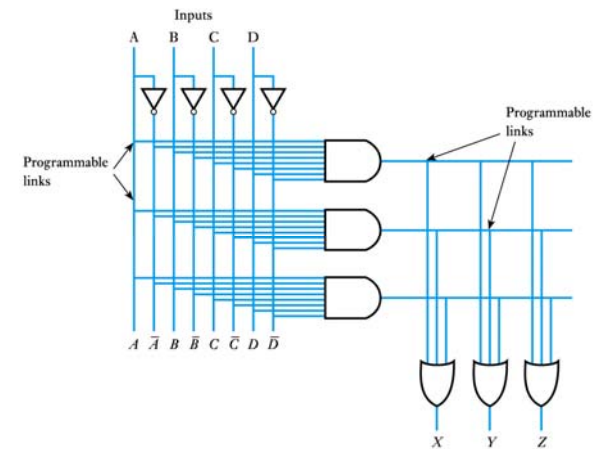
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- Array logic integrates large numbers of gates within a single package that is then configured for a particular application
- Complex digital systems can also be implemented using a microcomputer
- The implementation method used will depend on the complexity of the required system



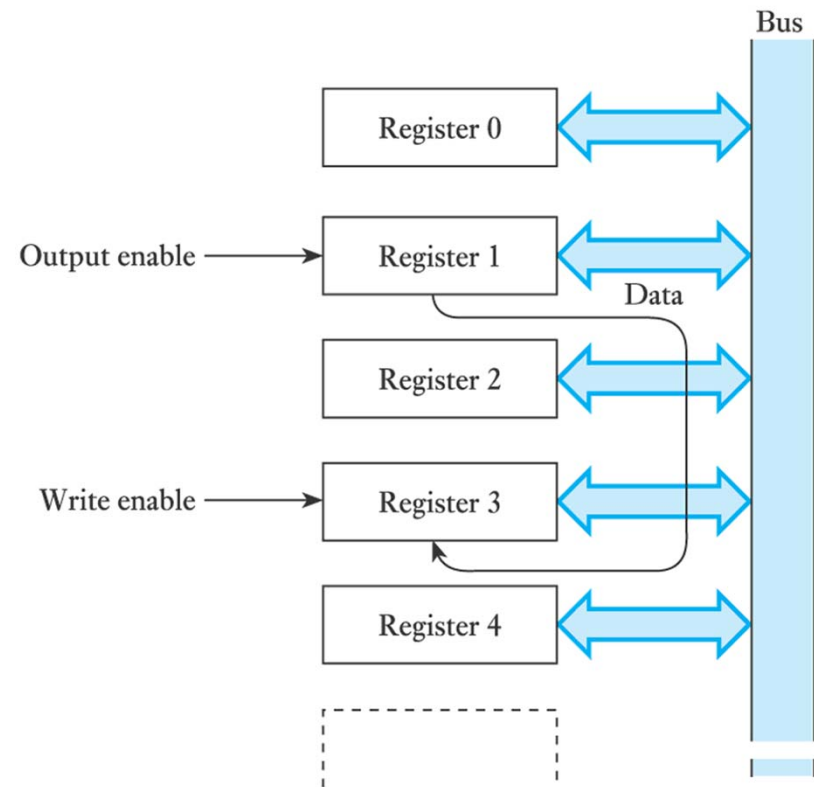
# Programmable logic array (PLA)

- the structure of a simple PLA
- To Implement
$$X = \overline{A}\overline{B}\overline{C}D + \overline{A}B\overline{C}D$$
$$Y = \overline{A}\overline{B}CD + ABCD$$
$$Z = \overline{A}\overline{B}\overline{C}D + \overline{A}\overline{B}CD + ABCD$$
- Fusible links are blown to program the device



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- **Parallel Communication within the microcomputer**
  - Via the parallel bus
- **Communications between registers (parallel I/O)**
  - achieved by enabling the output of one register and the input of another
  - as all the registers are connected by the same data bus, only one piece of information can be transmitted at any time



# Serial I/O

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- **Asynchronous serial communications**
  - Sender and receiver have (accurate) independent clocks
  - Clocks at the same frequency
  - Transition from “rest” state starts both clocks
- **Synchronous serial communications**
  - Synchronization field sent to receiver
    - A bit pattern or specific synchronization word
  - Receiver clock derived from sync-word/words

## Key points Chapter 28-

### Data acquisition and conversion

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- Converting an analogue signal to a digital form is achieved by sampling the waveform and then performing analogue to digital conversion
- As long as the sampling rate is above the Nyquist rate ( $>$  twice the highest frequency present), no information is lost as a result of sampling
- When sampling broad spectrum signals we make use of anti-aliasing filters to remove unwanted components
- When reconstructing signals, filters are used to remove the effects of the sampling
- A wide range of ADCs and DACs is available
- Sample and hold gates may be useful at the input or output
- Multiplexers can reduce the number of converters required

17.84

**Should be able to describe:**

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**The sampling system**

**Nyquist sampling rate and aliasing**

**Anti aliasing and reconstruction filters**

**Resolution of ADC**

**Sample and hold gates (good & bad features)**

**Typical speeds for ADC and DAC**