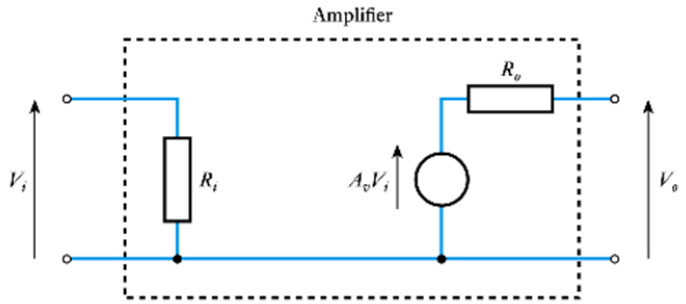
Solution set 3 TFY4185 Måleteknikk Issued 28 September 2015

1. **What is the open-circuit output voltage of the following arrangement?**



a) V_i b) R_o c) V_o **d) A_vV_i**

Without any loading effects, the output voltage of the amplifier will be whatever it sees as the voltage difference at its inputs, V_i, times the gain A_v, since gain is defined to be $V_o/V_i=A_v$.

2. **An amplifier has a voltage gain of 20, an input resistance of 500 ohms and an output resistance of 50 ohms. The amplifier is connected to a voltage source that produces an output voltage of 1 V and has an output resistance of 75 ohms, and to a load resistance of 800 ohms. What will be the voltage across the load resistor?**

a) 20 V **b) 16.4 V** c) 18.8 V d) 17.4 V

Now both the input source and output of the amplifier can be loaded down. For example, the voltage source produces an output voltage of 1 V with an internal output resistance of 75 Ω, but this is in series with any load I place on it. Thus, R_o and R_L form a voltage divider so that the voltage that will actually appear across the load will be $V_s/(R_S+R_L)$ times R_L. In this case, the load is actually the input resistance of the amplifier, R_i, stated to be 500 Ω. Now, if this resistance were very much greater than the source output resistance, we could ignore the source output resistance and the voltage across the amplifier would be 1V. But here they are relatively similar, and the voltage across the input of the amplifier will be:
$V_s/(R_S+R_i)\cdot R_i=1V/(575\Omega)\cdot 500\Omega = 0.870$ V.

Similarly, the amplifier will create a voltage $A_v\cdot V_i$, and drive this across an output impedance of 50 Ω. However, this is in series with the load resistor of 800 Ω. This means that the voltage that appears across this load is actually part of a voltage divider formed by R_o and R_L. So the voltage that appears across the load will be $A_v\cdot V_i/(R_o+R_L)$ times R_L. Now if R_L is very large compared to R_o, we can neglect R_o. Unfortunately here they are not so very different. The actual voltage across the load, the true output voltage of the amplifier, will be the divided voltage given above. This is:
$A_v\cdot V_i/(R_o+R_L)\cdot R_L = 20\cdot 0.87V/(850\Omega)\cdot 800\Omega = 16.4$ V

3. **An amplifier has a voltage gain of 20, an input resistance of 500 ohms and an output resistance of 50 ohms. The amplifier is connected to a voltage source that produces an output voltage of 1 V and has an output resistance of 75 ohms, and to a load resistance of 800 ohms. What is the voltage gain of this amplifier? (This is the same amplifier as in the previous question.)**

   a) 18.9 b) 20 c) 17.4 d) 16.4

   Since the input voltage, calculated in the previous problem, is 0.87V, and the output voltage is 16.4V, the effective gain of the amplifier is given by V_o/V_i = 16.4/0.87 = 18.8

4. **An amplifier has an input resistance of 1 kilohms and an output resistance of 25 ohms. The amplifier is connected to a load resistance of 100 ohms. What is the power gain of the amplifier if the input voltage is 3 V and the output voltage is 30 V?**

   a) 100 **b) 1000** c) 400 d) 4000

   In this case we are told that the input voltage to the amplifier is 3V, and by definition of V_i, this is the voltage that appears across the input resistance of 1 kΩ. Thus, the input power is:
   V^2/R = 9/1000 W = 9 mW.
   The amplifier is stated to have an output voltage of 30V. By definition of V_o, this is the voltage appearing across the 100Ω load resistance. Thus, the output power is:
   V^2/R = 900/100 W = 9W.
   The power gain is defined as P_o/P_i = 9/0.009 = 1000.

5. **What is the gain in dB corresponding to a power gain ratio of 300?**

   a) -24.8 dB **b) 24.8 dB** c) 49.5 dB d) 14.8 dB

   For a power gain, the gain in dB is defined as $G_p=10\cdot\log_{10}(P_o/P_i)$, where we are given that P_o/P_i=300. Thus, G_p = 24.8 dB.

6. **Differential amplifiers are designed to amplify common-mode signals while rejecting differential mode signals.**

   a) True **b) False**

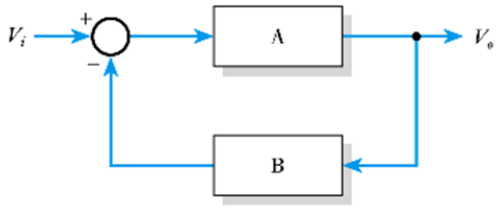
   Common mode is a voltage that appears across both the V_+ and V_- inputs. That is, it is a common offset to both inputs. A good differential amplifier should ignore these offsets and only amplify the voltage difference between the V_+ and V_- inputs. Thus, the statement is false.

7. **Which of the following correctly described the characteristics of a good operational amplifier?**

a) A very high voltage gain, a very low input resistance and a very high output resistance.
b) A very high voltage gain, a very high input resistance and a very high output resistance.
c) A very low voltage gain, a very high input resistance and a very high output resistance.
d) A very high voltage gain, a very high input resistance and a very low output resistance.

Ahh, perfection! The very high input resistance means that we can ignore any voltage divider effects when connecting a source since $R_i >> R_s$. and all the input voltage appears across R_i. Similarly, if $R_o << R_L$, then all of the voltage will appear across the load rather than some being dropped internal to the amplifier across the output impedance. And who does not want high gain! That lets me pick any gain I want using stable, external feedback resistors.

8. **What is the voltage gain of the following arrangement?**



a) *(1+AB) / B* b) *B / (1+AB)* **c) *A / (1+AB)*** d) *(1+AB) / A*

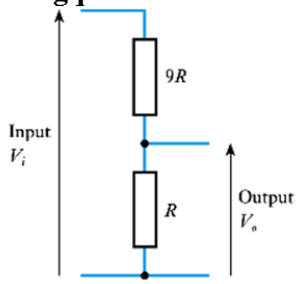
Here A and B represent the gains of the forward and feedback stages, respectively. The input to A must therefore be V_o/A, and the input to the subtraction junction from the feedback path must be $B \cdot V_o$. Thus $V_i - B \cdot V_o$ is the input to the forward stage, which we determined must be V_o/A. So:
$V_o/A = V_i - B \cdot V_o$, or the voltage gain, $V_o/V_i = A/(1+A \cdot B)$.

9. **Under what conditions does the gain of a feedback system approximate to 1/B?**

a) The loop gain AB >> 1. b) The feedback path gain B >> 1.
c) The loop gain AB << 1. d) The forward path gain A >> 1.

From above, under conditions where $AB >> 1$, then the denominator $(1+A \cdot B) \approx A \cdot B$. Then the system voltage gain is $A/(A \cdot B) = 1/B$, and the open-loop gain of the amplifier does not matter. That is, instead of the amplifier telling us how big the output could possibly be based on the open-loop gain, A of the amplifier, the feedback is telling us how big the output will be. So B represents how much of the amplifier's open-loop gain we want to use.

10. What is the gain of the following passive attenuator?



a) 0.1 b) 0.11 c) 9 d) 10

The word attenuator means that the output will be smaller than the input, so the gain must be less than 1. Here the output is the output of the voltage divider formed by the 2 resistors. The current, I, through these resistors is $V_i/(R+9R)$, and the voltage drop across the bottom resistor is $I \cdot R$. Thus, the output voltage
$V_o = I \cdot R = V_i/(R+9R) \cdot R = V_i/10$. So the gain, $V_o/V_i = 1/10$.

11. What is the effect of negative feedback on the gain of an amplifier?

a) It increases the gain by a factor of 1/B.
b) It reduces the gain by a factor of 1/B.
c) It increases the gain by a factor of (1 + AB).
d) It reduces the gain by a factor of (1 + AB).

From the equation for the gain we have $G=A/(1+AB)$, and the open-loop gain of the amplifier is $G_i = A$. Therefore, the effect of negative feedback is to reduce the gain from A by a factor of 1+AB.

12. What is the effect of negative feedback on the bandwidth of an amplifier?

a) It increases the bandwidth, often by a factor of 1/B.
b) It reduces the bandwidth, often by a factor of (1 + AB).
c) It reduces the bandwidth, often by a factor of 1/B.
d) It increases the bandwidth, often by a factor of (1 + AB).

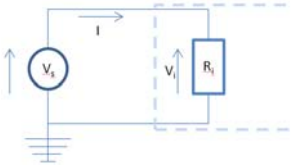
Gain x bandwidth is a generally a constant. Thus, decreasing the gain by a factor of (1+AB) will, in many cases, increase the bandwidth by the same factor (1+AB).

13. What are the effects of negative feedback on the input and output resistance of an amplifier?

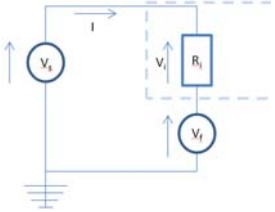
a) It can either increase or decrease the input and output resistance depending on how it is applied.
b) It increases input resistance and decreases output resistance.
c) It decreases input resistance and increases output resistance.
d) It increases both input and output resistance.

It depends upon how the output signal is sensed and how the feedback is applied. If the signal being fed back is related to the output voltage, then the output resistance will decrease. For example, this is typically done by allowing the output voltage to go to ground through a resistor divider (with the feedback derived from the fraction of output voltage dropped across the feedback resistor). Thus, there will be parallel paths to ground through the internal output resistance of the amplifier as well as through the feedback divider, giving an equivalent output resistance that is lower.

When the feedback applied at the input is a voltage, it is effectively subtracted from the input voltage derived from the source, V_s. So, before feedback the input circuit is a simple loop with the source voltage across the input resistance, so $V_i = V_s = I \cdot R_i$.

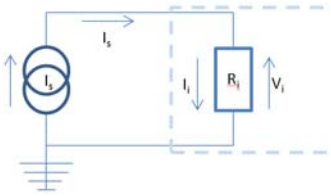


After feedback is added, the voltage across the amplifier input is generated by the source voltage, V_s, as well as the feedback voltage, $V_f = B \cdot V_o$, as shown below.

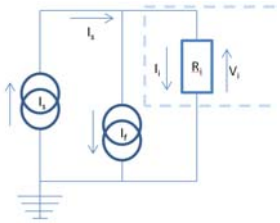


Now Kirchoff's voltage law would give $V_s = V_i + V_f$, or $V_s = I \cdot R_i + BV_o$. Since V_o is derived from the input voltage through the open-loop gain, $V_o = AV_i = A\, I \cdot R_i$. Thus, the effective amplifier input resistance, R_i', that the source sees, which is V_s/I, becomes (with feedback) $R_i' = R_i(1+AB)$, or that it has increased by a factor of $1+AB$ over the no feedback case.

On the other hand, if the feedback is a current (as it is in an inverting amplifier), then without feedback the input current is $I_s = I_i = V_i/R_i$.



However, with feedback, the feedback current represents a second, parallel current to ground.



Applying Kirchoff's current law, $I_s=I_i + I_f$, or , $I_s=I_i +BI_o$. Since I_o is derived from the input current through the open loop gain, $I_o=AI_i$. Thus, the source current is now $I_s=I_i (1+AB)$, and thus it is clear that the source current has increased over the non-feedback case by a factor of (1+AB). That means that the effective resistance of this circuit is less by the same factor. In fact, the effective resistance of the circuit, $R_i'=V_i/I_s$. From the expression for I_s above, since $I_i = V_i/R_i$, it is clear that $R_i'=V_i/I_s = R_i/(1+AB)$, and the effective input resistance is now smaller by a factor of (1+AB).

If the feedback is determined from the output current, the equivalent output resistance can be shown to increase by the same factor. For this course, we have not discussed any circuits that have used the output current to create the feedback signal (we have used the output voltage across a resistance chain to create a feedback voltage (non-inverting) or current (inverting) at the inputs. We can change the feedback resistance and change the feedback current and voltage, but V_o would remain the same).

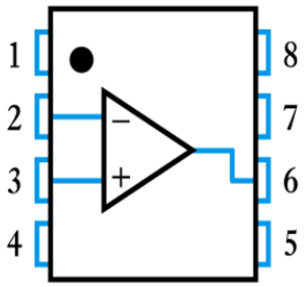
This gives rise to the rule that if the feedback connection is a parallel connection, it decreases the effective resistance of the amplifier as seen by the circuit. However, if the feedback connection is a series connection, it increases the effective resistance. For voltage feedback, the input feedback connection is in series but the output feedback connection is in parallel$\Rightarrow$ increasing R_i and decreasing R_o. But for current feedback, the input feedback connection is in parallel and the output connection in series$\Rightarrow$ increasing R_o and decreasing R_i.

14. Negative feedback reduces the noise corrupting a signal by a factor of (1 + AB).

a) True **b) False**

Well, while the noise might be reduced by a factor of 1+AB, the signal is also reduced by the same factor. Thus, once the noise is on the signal, the signal to noise is set. Amplifying it keeps the same signal to noise, and decreasing the amplification does not help.

15. What signal corresponds to pin 3 of this operational amplifier?



a) The non-inverting output.
b) The positive supply voltage.
c) The inverting input.
d) The non-inverting input.

If the voltage at the "positive" input is raised above that at the "negative" input, the output of the amplifier will attempt to control the voltage at the "negative" input to cancel the voltage difference between the two inputs. Thus, it produces a voltage so as to raise the voltage at the "negative" input. This will be in the same direction as the voltage at the positive input, and hence the amplifier output will not invert the input signal.

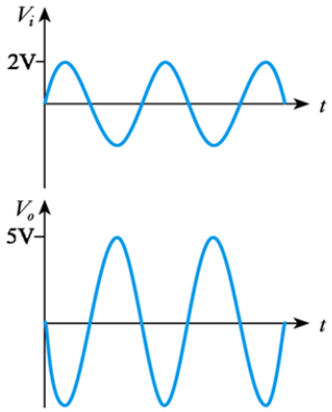
By contrast, if the voltage at the "negative" input is raised above that at the non-inverting input, the output will again attempt to control the voltage at the "negative" input in order to cancel the voltage difference between the inputs, and hence would produce a negative voltage in an attempt to lower the potential at the "negative" input. Since this would have the opposite sign of the input voltage, this input is called the inverting input.

16. What characteristics would characterize an ideal operational amplifier?

a) An infinite voltage gain, zero input resistance and an infinite output resistance.
b) An infinite voltage gain, an infinite input resistance and an infinite output resistance.
c) An infinite voltage gain, zero input resistance and zero output resistance.
d) An infinite voltage gain, an infinite input resistance and zero output resistance.

Such an amplifier would not be loaded by any source or load resistance, and the gain would not affect the bandwidth!

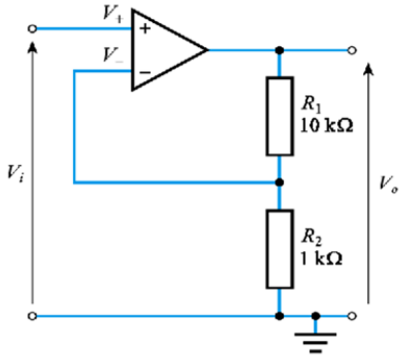
17. The graphs below show the input and output waveforms of an amplifier. What is the gain of this circuit?



a) -0.4 b) 2.5 c) 0.4 **d) -2.5**

The voltage gain is defined as the ratio of the output voltage to the input voltage. Here that would be Gain = V_o/V_i = -5V/2V = -2.5

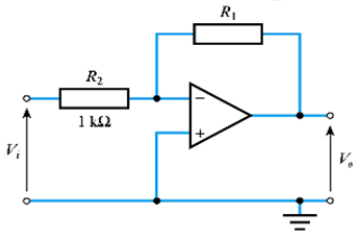
18. What is the voltage gain of this circuit?



a) 0.091 b) 0.1 c) 10 **d) 11**

Here the feedback is derived from the output voltage that is divided across the resistor network formed by R_1 and R_2. Since no current flows into the amplifier (for an ideal amplifier), the feedback voltage appearing at the inverting input, V_-, is given by $V_f = V_o \cdot R_2/(R_1+R_2)$. When the feedback voltage is equal to the input voltage, Vi = Vf, there will be no voltage difference across the inputs of the amplifier and the output voltage will stabilize. The gain, is the ratio of the output to input voltage, so, substituting Vi into the feedback voltage equation allows us to calculate the gain as: $Vo/Vi = (R_1+R_2)/R_2$. Substituting in 10 kΩ and 1 kΩ for R_1 and R_2, gives a gain of 11.

19. In the following circuit, what value of R_1 is required to give a voltage gain of -50?

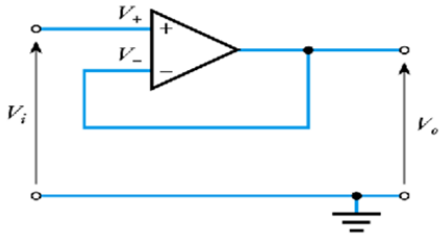


a) 50 kΩ b) -50 kΩ c) -49 kΩ d) 49 kΩ

In this case, the potential difference between V_i and V_o will cause currents to flow through R_2 and R_1. Since the non-inverting input is at ground potential (0 V), the system will be stable when the voltage at the inverting input is also at 0 V. One can either view it as the current created by V_i across R_2 will be cancelled by the current flowing through R_1 created by V_o, since there is no current flowing into the amplifier (for an ideal amplifier). Thus, $I_2 = V_i/R_2$ must be equal and opposite to $I_1 = V_o/R_1$. Under these conditions, the gain = $V_o/V_i = -R_1/R_2$. To give a gain of -50, with $R_2 = 1\ k\Omega$ requires $R_1 = 50k\Omega$.

One could also view this as the voltage difference between V_i and V_o causing a current to flow across the voltage divider formed by R_2 and R_1, since no current flows into the (ideal) amplifier. The feedback voltage at the inverting input, V_f, which is derived from the voltage drop across R_1, must be 0V. Hence $(V_f - V_o) = (V_i - V_o)/(R_1+R_2)\cdot R_1$. When Vf=0, this gives V_o/V_i = gain = $-R_1/R_2$, as above. Note that since this condition must be true even in the unloaded condition shown in the figure, the output of the amplifier must source or sink current in order to keep $V_- = 0V$.

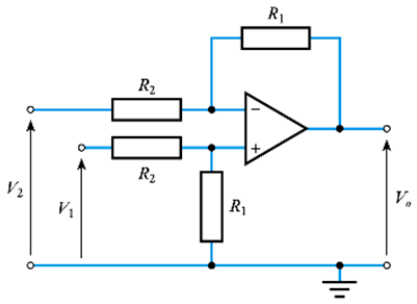
20. What are the characteristics of the following circuit?



a) It has a voltage gain of unity, a low input resistance and a low output resistance.
b) It has a voltage gain of unity, a high input resistance and a high output resistance.
c) It has a voltage gain of unity, a low input resistance and a high output resistance.
d) It has a voltage gain of unity, a high input resistance and a low output resistance.

Since no current flows into the inputs of an ideal amplifier, when the output voltage reaches V_i, the voltage at V_- will also be V_i, and there will be no voltage difference across the amplifier inputs. The source will see the high input impedance of the amplifier, and the load will see the low output impedance of the amplifier.

21. In the following circuit, the use of negative feedback decreases the output resistance.



a) True b) False

As was explained in question 13, when the output voltage is used to derive the feedback signal, then the output resistance will decrease. In all the circuits we discussed, it is the output voltage that creates the feedback signal. That is, it is the size of the output voltage that causes a current to flow in the feedback chain. If the voltage drop of that current is applied to the input of the amplifier as a negative feedback, it will increase the input resistance. If the current created by that output voltage is used as negative feedback at the inputs, then the input resistance decreases. Note that we have not discussed any circuits where it is the output current itself that determines the feedback signal.

22. Which of the following statements is incorrect?

a) Conduction within pure semiconductors is termed intrinsic conduction.
b) The dominant charge carriers within a doped semiconductor are called majority charge carriers.
c) Doping pure semiconductor material with small amounts of donor impurities produces an *n*-type semiconductor.
d) **At room temperatures, pure semiconductors make excellent conductors.**

Un-doped, or pure semiconductors have a band gap on the order of 1 eV. Although better conductors than insulators, where the band gap between the conduction and valence bands and be on the order of several eV, they are rather poor conductors compared to metals where the conduction and valence bands overlap. Thus, at room temperature, pure semiconductors are rather poor conductors.

23. What is a typical conduction voltage for a silicon diode?

a) 0.25 V b) 0.5 V c) **0.7 V** d) 1.1 V

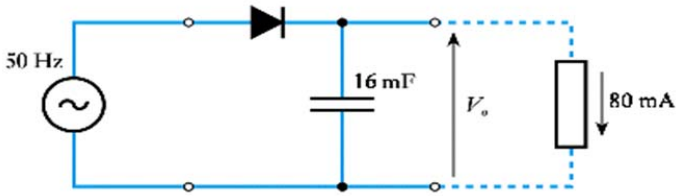
The relationship between the diode current and the voltage across the diode is given by $I \approx I_s \cdot e^{40 \cdot V}$. *Inverting this we have* $V_d \approx 1/40 \cdot \ln(I/I_s)$, *or about* $0.06 * \log_{10}(I/I_s)$. *Since* $I_s \sim 10^{-12}$ *(typically), and currents I~100 mA,* V_d *is typically 0.6 to 0.7 V.*

24. What would be a typical magnitude for the reverse current in a general-purpose silicon diode?

a) <10 picoamps **b) <10 nanoamps** c) <10 microamps d) <10 milliamps

This is a typical value, but a pretty close judgement call. The saturation current is a reverse saturation current is a strong function of temperature, varying from 500 pA at 15 ^{o}C to about 800 pA at 20^{o}C and 2 nA at 25 ^{o}C. Hence a few nA is the best choice.

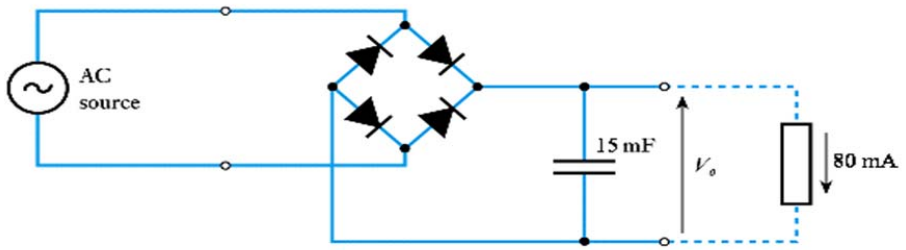
25. Estimate the peak ripple voltage in the following arrangement.



a) 10mV b) 25mV c) 50 mV d) **100 mV**

Note that the output current is held at a constant 80 mA in this example (rather than a constant load resistance). This is a physically unrealistic, but makes the calculation much easier. Starting with the voltage across the capacitor, which is given by V=q/C, and looking at its time rate of change: dV/dt = 1/C·dq/dt = I/C, then we can easily estimate how much V changes for a constant current, I, in a time span dt. Since this diode will only be conducting during one half of the cycle (less with the reserve capacitor in place), its charge will drop until the voltage on the next cycle begins to charge it again. We can estimate that the potential across the capacitor will fall for a cycle with the constant current I = 80 mA. For a 50 Hz supply, the full cycle period is 1/(50 cycles/s) = 0.020 sec, and the voltage change over that time is:
$\Delta V = I/C \cdot \Delta t = 0.080A/16x10^{-3}F \cdot 0.020s = 0.1V$, or 100 mV.

26. Estimate the peak ripple voltage in the following arrangement.

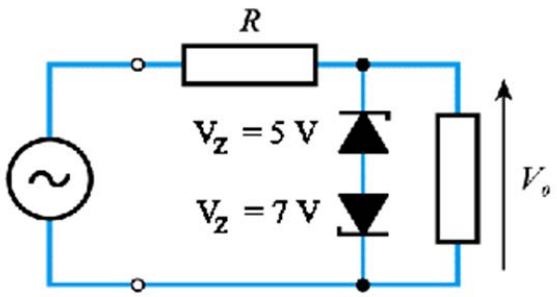


a) 10 mV b) 25mV c) **50mV** d) 100mV

Now the diode conducts every ½ cycle, halving the time the voltage can fall to 0.01 s.

Since it is the same current as above, this would allow the voltage to change by 50 mV.

27. Estimate the maximum positive voltage produced by the following arrangement.



a) 4.3 V b) **5.7 V** c) 6.3 V d) 7.7 V

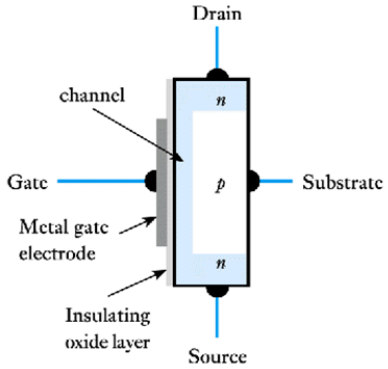
During a positive cycle, the 5 V Zener diode is reversed biased and will breakdown when the voltage exceeds 5 V plus the internal voltage drop of the diode, ~0.7 V. The voltage cannot raise above that point, so the maximum positive voltage is 5.7 V.

28. Which terminal represents the control input of a FET?

a) The drain b) The source c) The base d) **The gate.**

The voltage applied to the gate will restrict or expand the conduction channel, controlling the current flowing from the drain to the sink.

29. What form of FET is shown here?

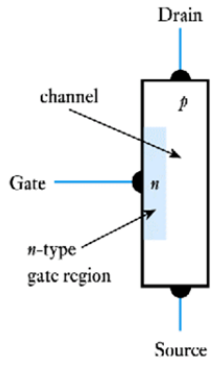


a) An *n*-channel MOSFET. b) An *n*-channel JFET.
c) A *p*-channel JFET. d) A *p*-channel MOSFET.

The conduction channel (drain-source) of this FET is n-type material, and there is a metal electrode on an insulating silicone oxide layer. Therefore this is a n-channel MOSFET. The question and answer sheet for this question was in error as it called it a p-

channel MOSFET. The channel is indeed n-type material

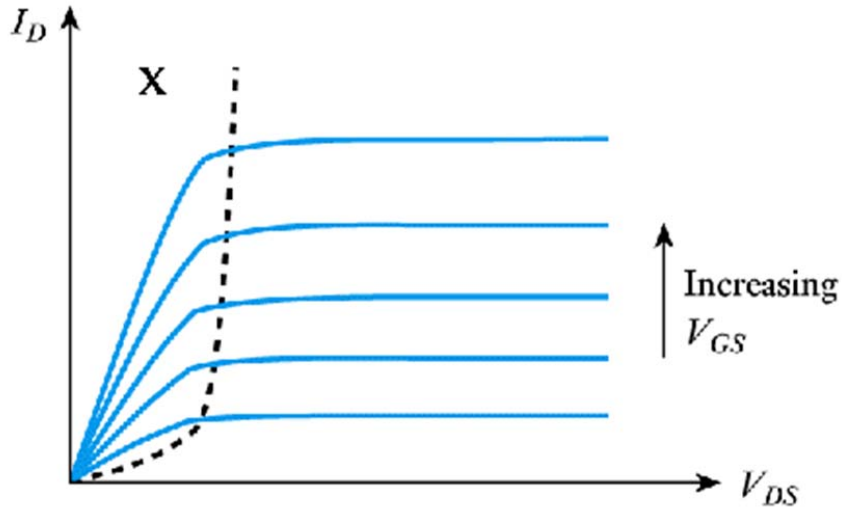
30. What form of FET is shown here?



a) An *n*-channel JFET.
b) A *p*-channel MOSFET.
c) **A *p*-channel JFET.**
d) An *n*-channel MOSFET.

Here the conduction channel (drain-source) is a p-type material. Since the gate is connected directly to the n-type gate region junction with no insulator, this is a junction FET, or p-channel JFET.

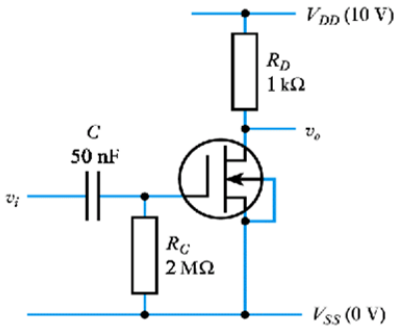
31. In the FET output characteristics shown below, what region is represented by the symbol 'X'?



a) The operating region.
b) The space-charge region.
c) The saturation region.
d) **The ohmic region.**

The region marked by X is the region where the current at the drain linearly increases with the voltage across it, or $I_D = V_{DS}$/constant. Paralleling ohms law, where I=V/R, this is called the ohmic region.

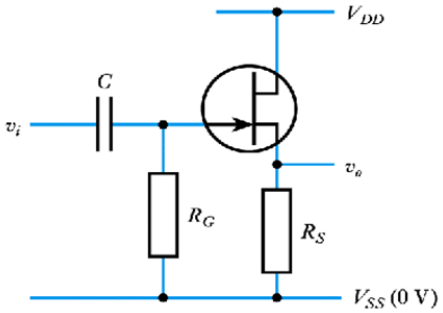
32. Determine the cut-off frequency of the following circuit.



a) 0.63 Hz b) **1.6 Hz** c) 3.6 Hz d) 10 Hz

The 50 nF capacitor and 2 MΩ resistor will form a high-pass filter (we are looking at the voltage across the resistor which is maximum when current is flowing. At high frequencies, the capacitor looks more and more like a wire, conducting the current across R_C). The time constant is R·C, and the cutoff frequency is $\omega_c = 1/(R \cdot C)$ since the natural units of frequency are radians/s. Thus, $f_c = \omega_c / 2\pi$ would be $1/(2\pi \cdot 2x10^6 \cdot 50x10^{-9})$ Hz=1.59 Hz.

33. What are the characteristics of the following circuit?



a) A voltage gain of 1, a low input resistance and a high output resistance.
b) A high voltage gain, a high input resistance and a low output resistance.
c) A high voltage gain, a low input resistance and a high output resistance.
d) **A voltage gain of 1, a high input resistance and a low output resistance.**

This is a source follower circuit, and is characterized by a gain of 1, high input and low output impedances. Note, this circuit, a source follower, would not be on the final.

34. FETs may be used as both analogue and logical switches.

a) **True** b) False

This is true and was covered in lecture. Note, this would not be on the final