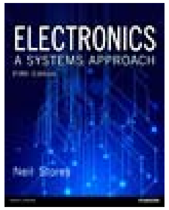
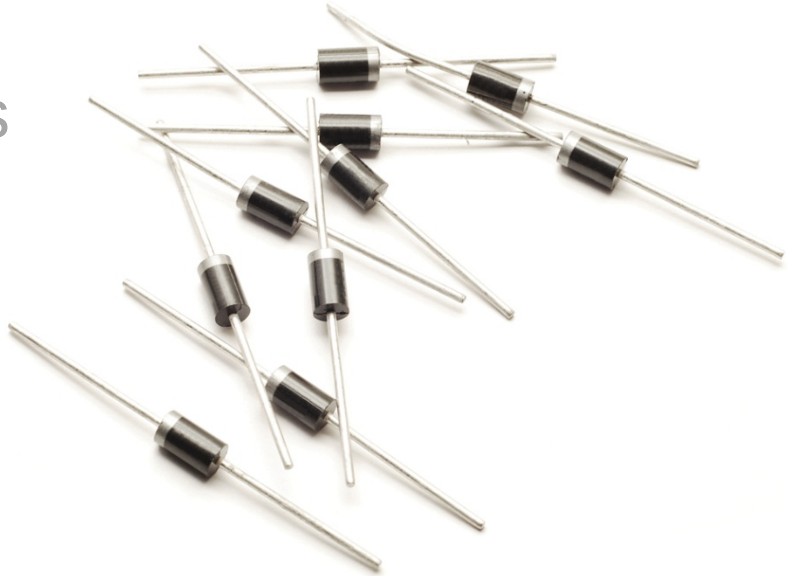
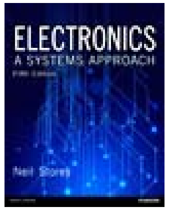


Last time: Semiconductors and diodes

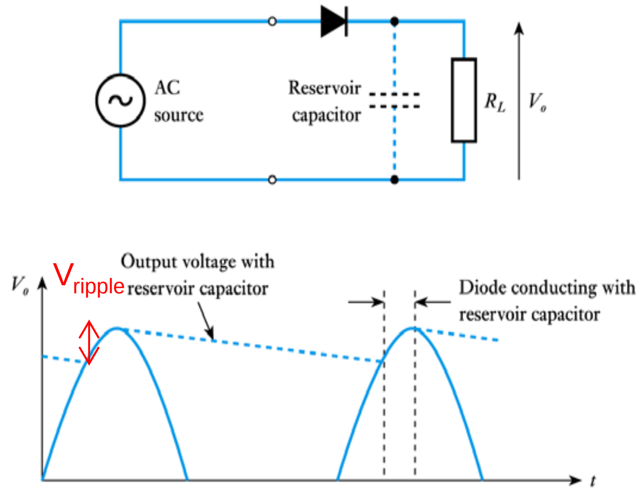
- Introduction
- Electrical properties of solids
- Semiconductors
- *pn* Junctions
- Diodes
- Semiconductor diodes
- Special-purpose diodes (Zener diode most important)
- Diode circuits.
- Field effect transistors



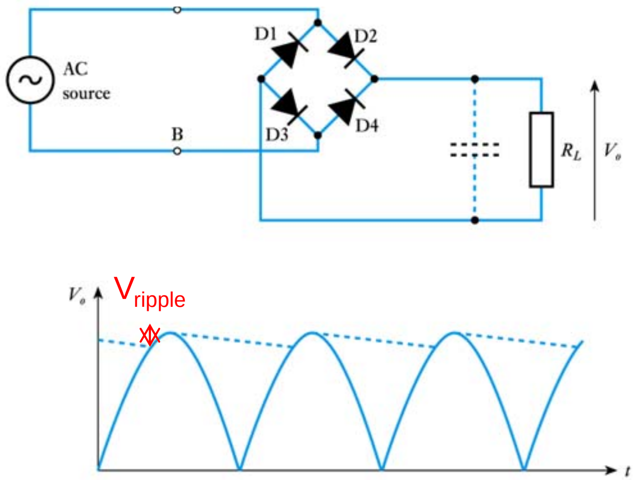
Last time Diode circuits



- **Half-wave rectifier**



- **Full-wave rectifier**
  – reservoir capacitor typically used in both to produce a steadier output

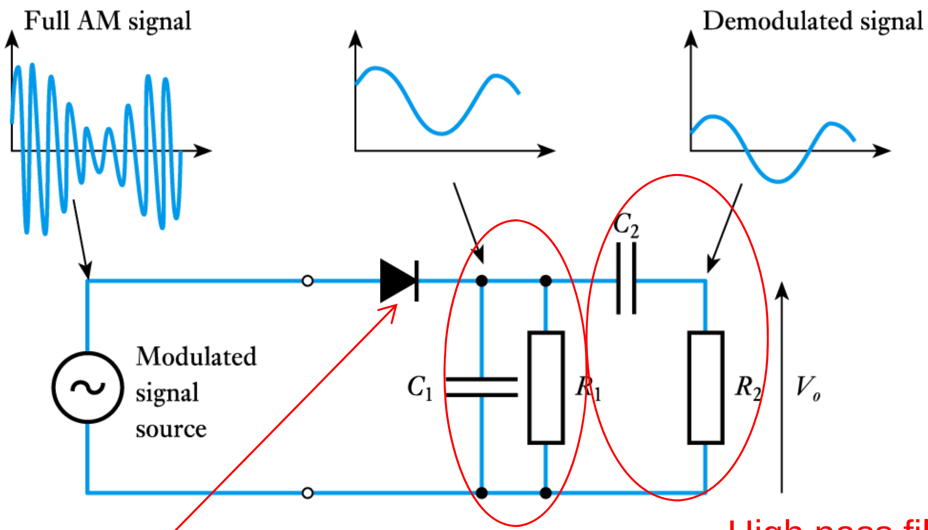


Video 17B

- **Signal rectifier**

Signal is the low frequency part
Carrier is the high frequency part

  - used to demodulate full amplitude modulated signals (**full-AM**)
  - also known as an **envelope detector**
  - found in a wide range of radio receivers from crystal sets to superheterodynes

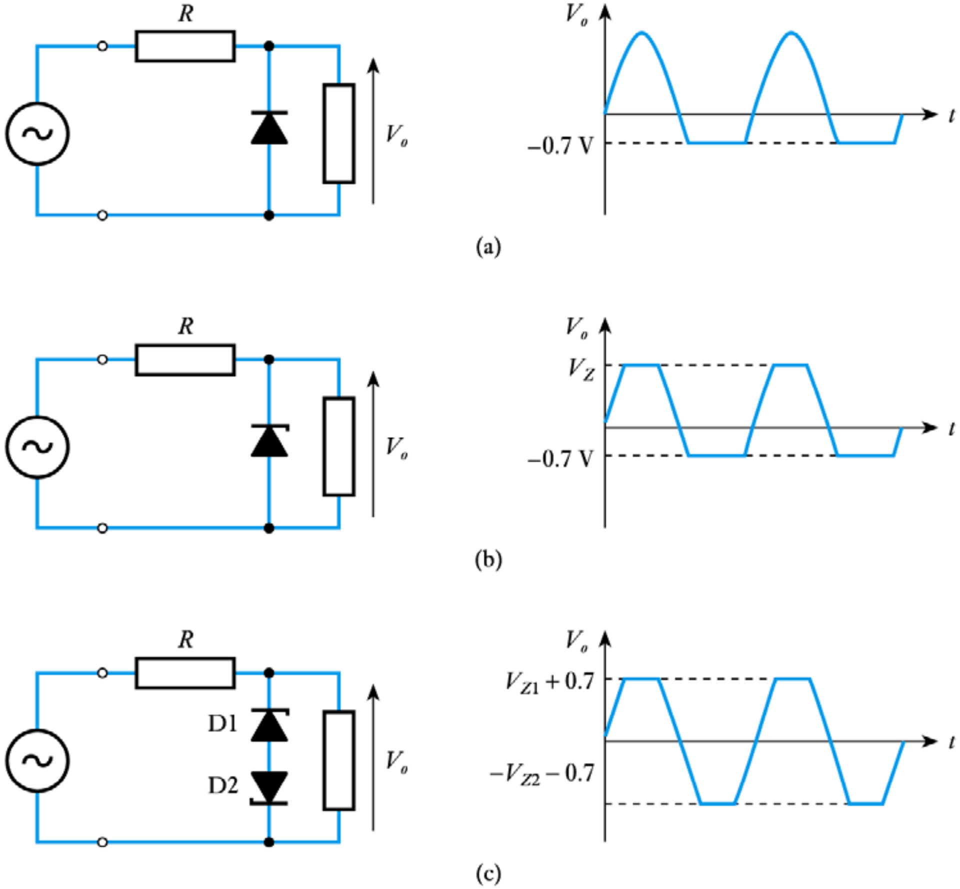


Diode half-wave rectifies the signal (no negative voltages)

Low pass filter $\omega_c = R_1 \cdot C_1 > \omega_s$ but less than carrier frequency
Removes carrier frequency

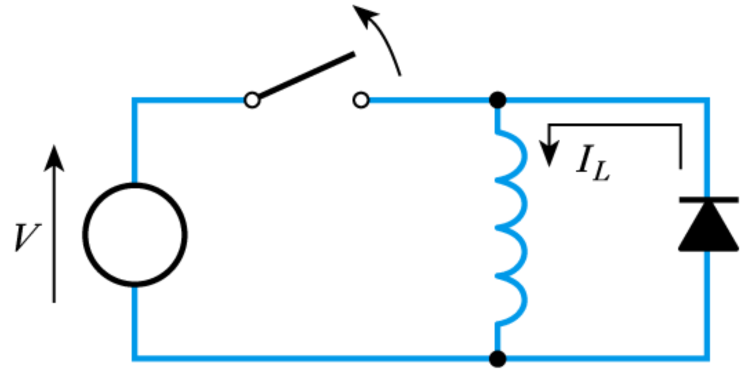
High pass filter removes DC

- **Signal clamping**
  - a simple form of **signal conditioning**
  - circuits limit the excursion of the voltage waveform
  - can use a combination of signal and Zener diodes



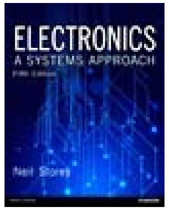
Input to a device where input voltage must be < V_Z

Catch diode



- used when switching inductive loads
- the large back e.m.f. can cause problems such as arcing in switches
- **catch diodes** provide a low impedance path across the inductor to dissipate the stored energy
- the applied voltage reverse-biases the diode, which therefore has no effect
- when the voltage is removed the back e.m.f. forward biases the diode which then conducts

Further Study



Video 17C Further Study

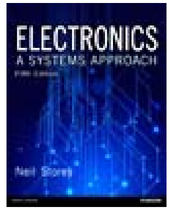
- The Further Study section at the end of Chapter 17 is concerned with the design of a mains power supply.
- The supply is to drive an appliance that requires a fairly constant input of 12V and takes a current that varies from 100 to 200 mA.

- Design such a unit and then look at the video.

Key points

- Diodes allow current to flow in only one direction
- At low temperatures semiconductors act like insulators
- At higher temperatures they begin to conduct
- Doping of semiconductors leads to the production of *p*-type and *n*-type materials
- A junction between *p*-type and *n*-type semiconductors has the properties of a diode
- Silicon semiconductor diodes approximate the behaviour of ideal diodes but have a conduction voltage of about 0.7 V
- There are also a wide range of special purpose diodes
- Diodes are used in a range of applications

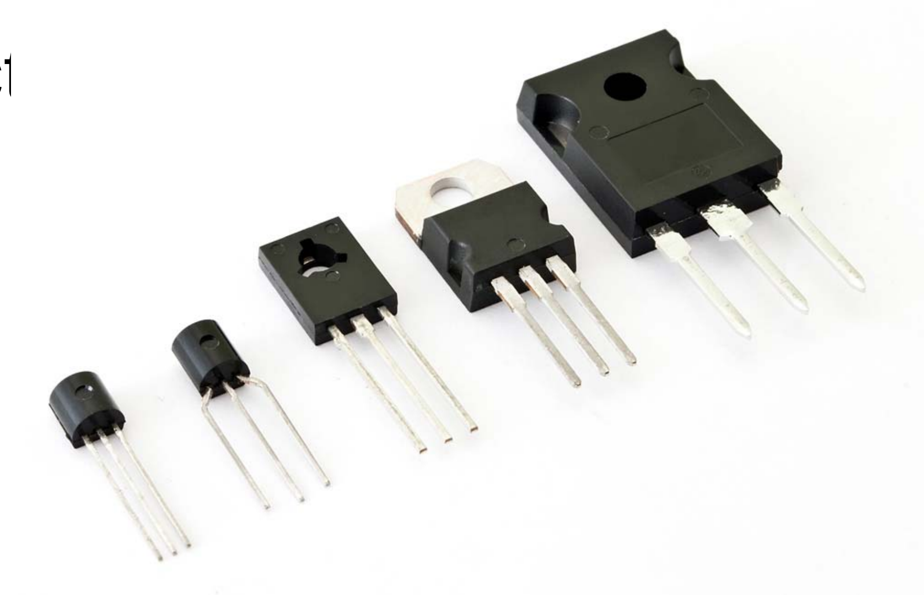
- Questions so far?

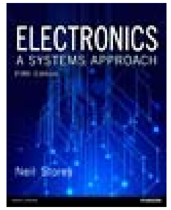


Chapter 18

Today: Field-effect transistors

- Introduction
- An overview of field-effect transistors
- Insulated-gate field-effect
- Junction-gate field-effect
- FET characteristics
- FET amplifiers
- Other FET applications
- FET circuit examples

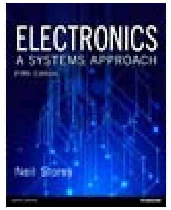




18.1

Introduction

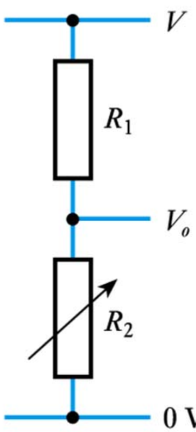
- **Field-effect transistors** (**FETs**) are probably the simplest form of transistor
  - widely used in both analogue and digital applications
  - they are characterized by a very high input resistance and small physical size, and they can be used to form circuits with a low power consumption
  - they are widely used in **very large-scale integration**
  - two basic forms:
    - **junction gate FETs**
    - **insulated gate FETs**



14.9

Simple amplifiers

- Amplifiers can also be formed using a ‘control device’
  - circuit is a potential divider with one resistor replaced with a variable resistor that controls I flowing through the resistors
  - If we could control (adjust) R_2 or the current from V to ground with the input voltage, then we have $V_o \propto V_i$ which is an amplifier



$$= V\,R_2/(R_1+R_2)$$

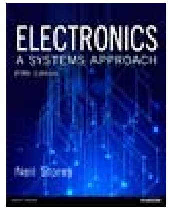
$$= V - I \cdot R_1$$

A potential divider

As R_2 decreases, V_o decreases
(or I through the system increases)
As $R_2 \to 0$, (I increases) and $V_o \to 0$

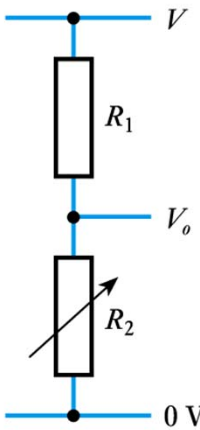
As R_2 increases, V_o increases
(or I through the system decreases)
When R_2 is >> R_1, $R_2/(R_1+R_2) \to R_2/R_2 = 1$
And $V_o \to V$

Simple amplifiers



14.9

- Amplifiers can also be formed using a 'control device'
  - circuit is similar to a potential divider with one resistor replaced with a variable resistor that controls I flowing through the resistors
  - 'control device' typically a **transistor**
  - $V_o = V\text{-}I{\cdot}R_1$ so that if the device controls I, it controls V_o

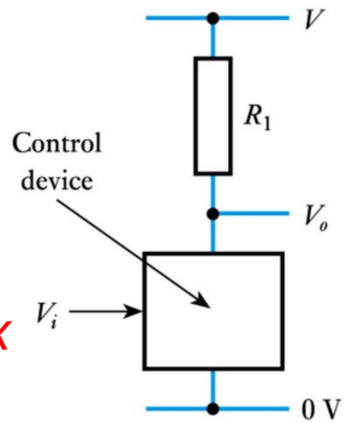


= V R₂ / (R₁+R₂)

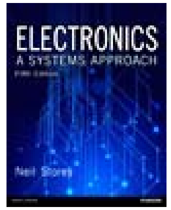
$V_o = V R_2 / (R_1+R_2)$

A potential divider

V_i controls R of box (or I thorough box)

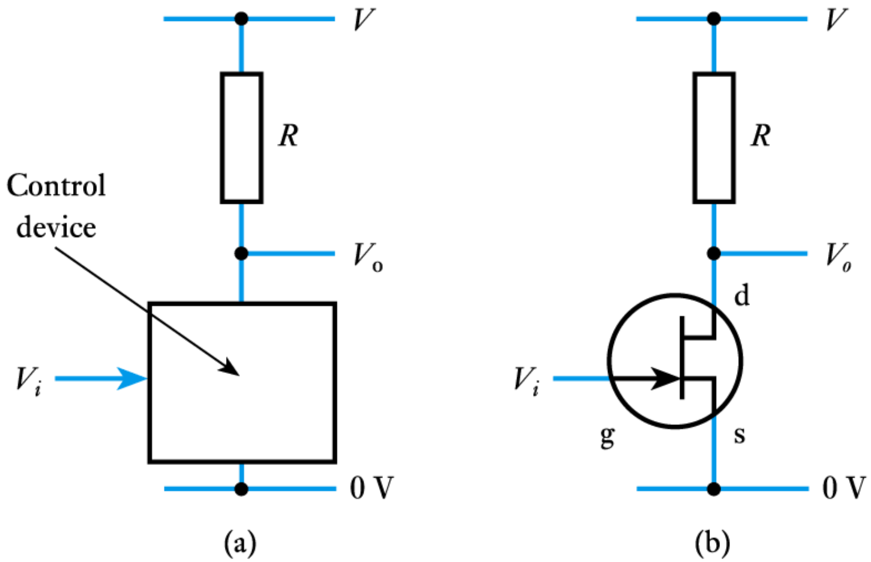


A simple amplifier

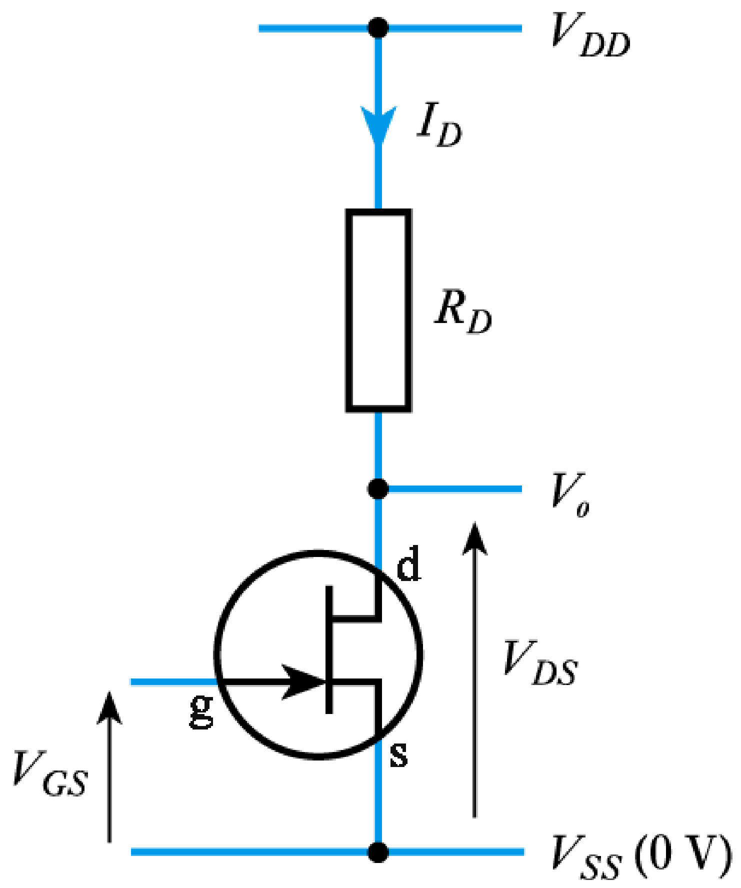


An overview of field-effect transistors

- Many forms, but basic operation is the same
  - a voltage on a control input produces an electric field that affects the current between two other terminals
  - when considering amplifiers we looked at a circuit using a 'control device'
  - a FET is a suitable control device



- **Notation**
  - – FETs are 3 terminal devices
    - drain (d)
    - source (s)
    - gate (g)
  - – the gate is the control input
  - – diagram illustrates the notation used for labelling voltages and currents



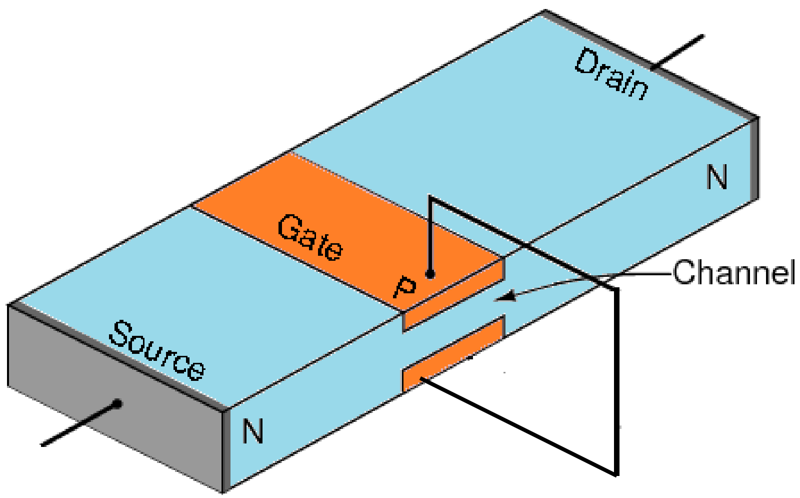
Why does this work? What's in the box?

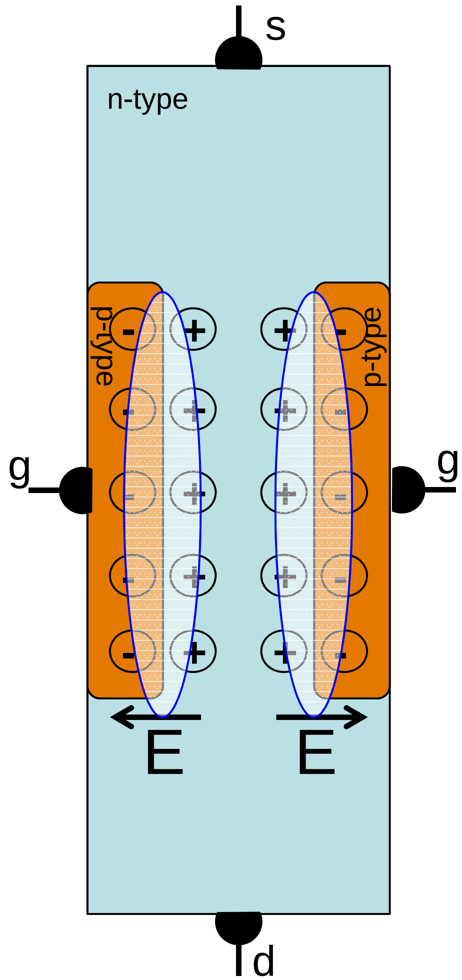
A diode—pn-junctions!

An n-type bar with 1 or 2 p-type inserts

Will get majority carriers diffusing across the junction that leave ionized dopants

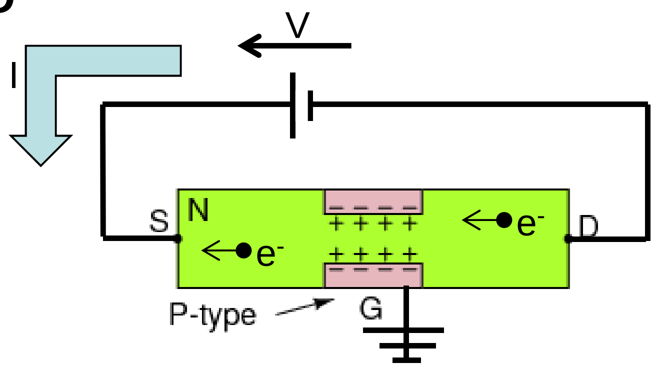
Creates electric fields and depletion regions





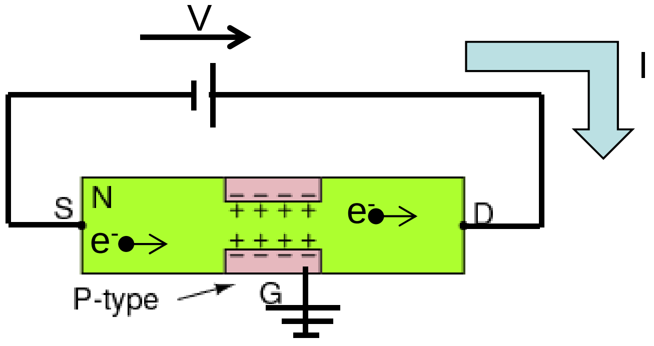
How do I adjust current with a control voltage?

- With a source-drain voltage (gate at ground)- majority charges carriers flow in the n-material (electrons)

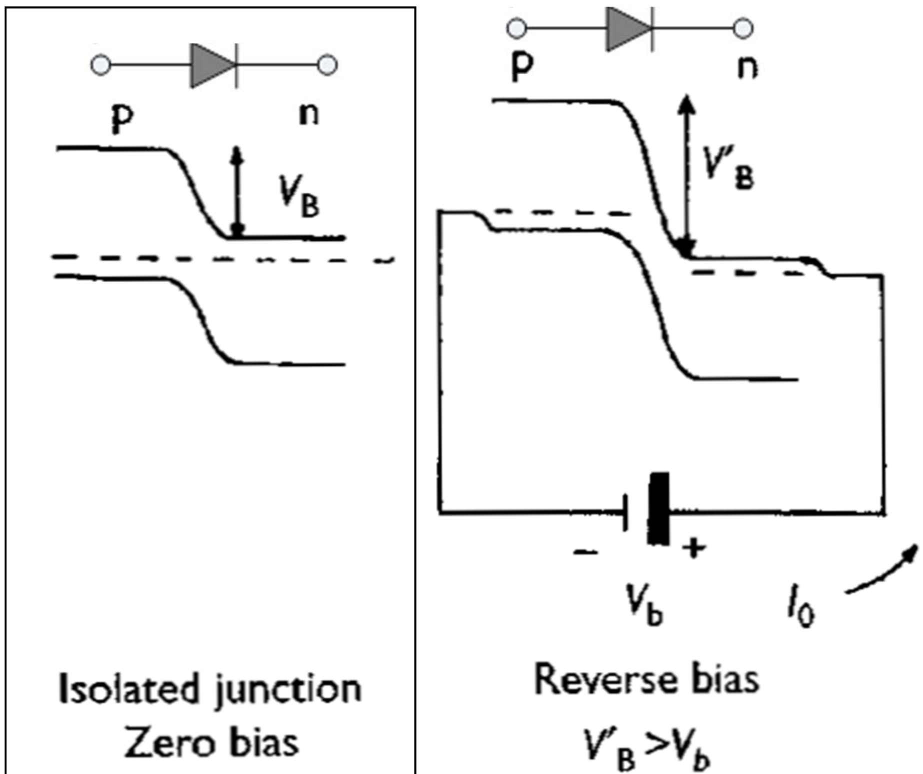


- Does not matter the direction

Current depends on V and the number of free charge carriers (enhanced in doped material)

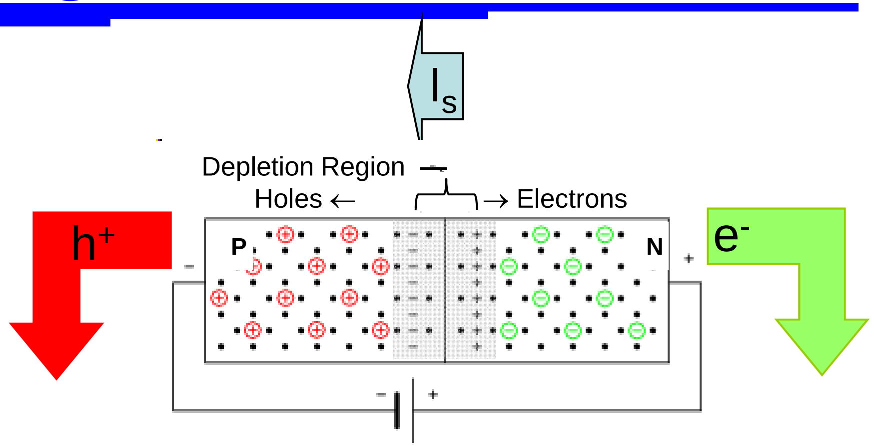


Reverse bias gate-source (p-n) to change the width of the *depletion* region



Reverse Bias-increase V_B

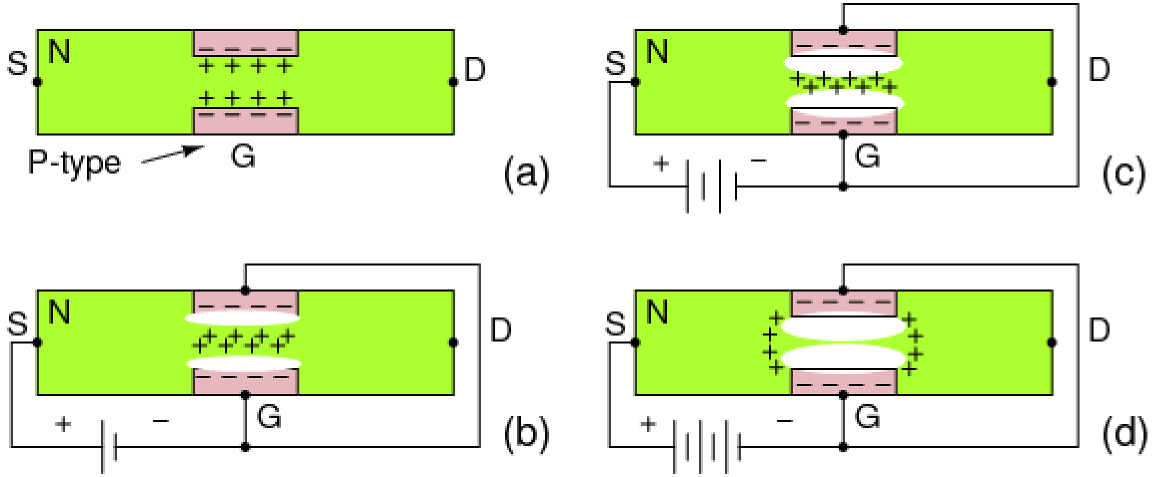
$$V'_B = V_B + |V_b|$$

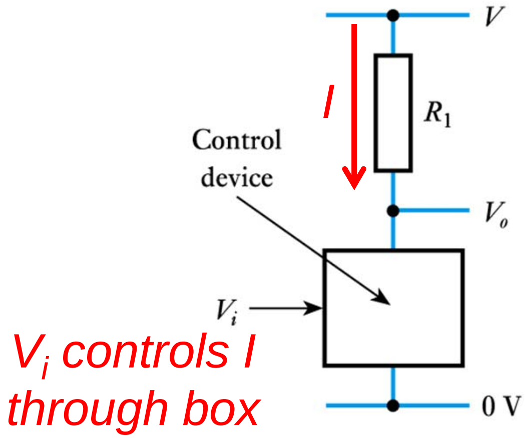


Reverse battery bias:

- *attract majority carriers to battery terminal away from junction.*
- ***Depletion region thickness increases.***
- *No sustained current flows*
- *Only random thermal events supply I_s*

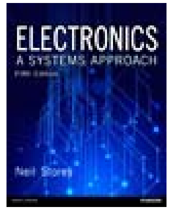
Adjust gate-source voltage to adjust resistance





i.e. A simple amplifier

- Increasing the reverse bias on the pn-junction (a→d in figure)
- The wider the ***depletion*** region (white) becomes
- The thinner the conduction channel (green) becomes
- Fewer free charge carriers in depletion region to carry current
- Higher resistance (V_{bias} controls I between source & drain)



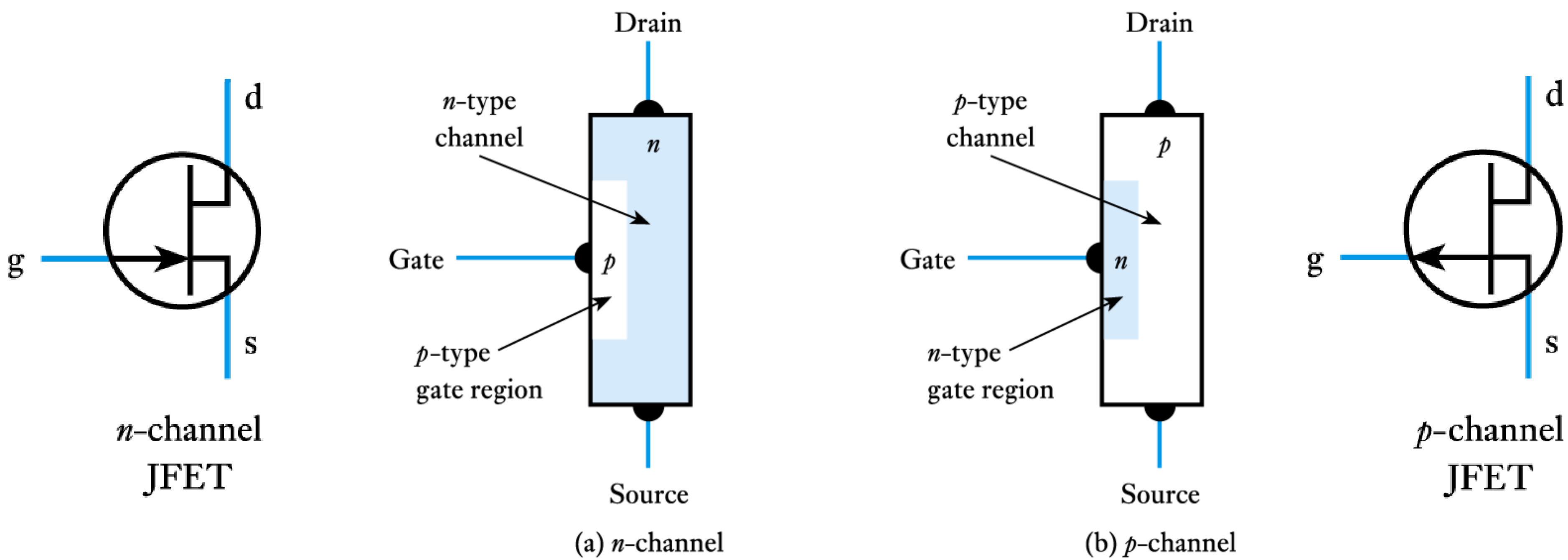
18.4

Junction-gate field-effect transistors

- Sometimes known as a **JUGFET**
- Here we will use another common name – the **JFET**
- Here the gate is a reverse-biased *pn* junction
- Since the gate junction is always reverse-biased no current flows into the gate and it acts as if it were insulated

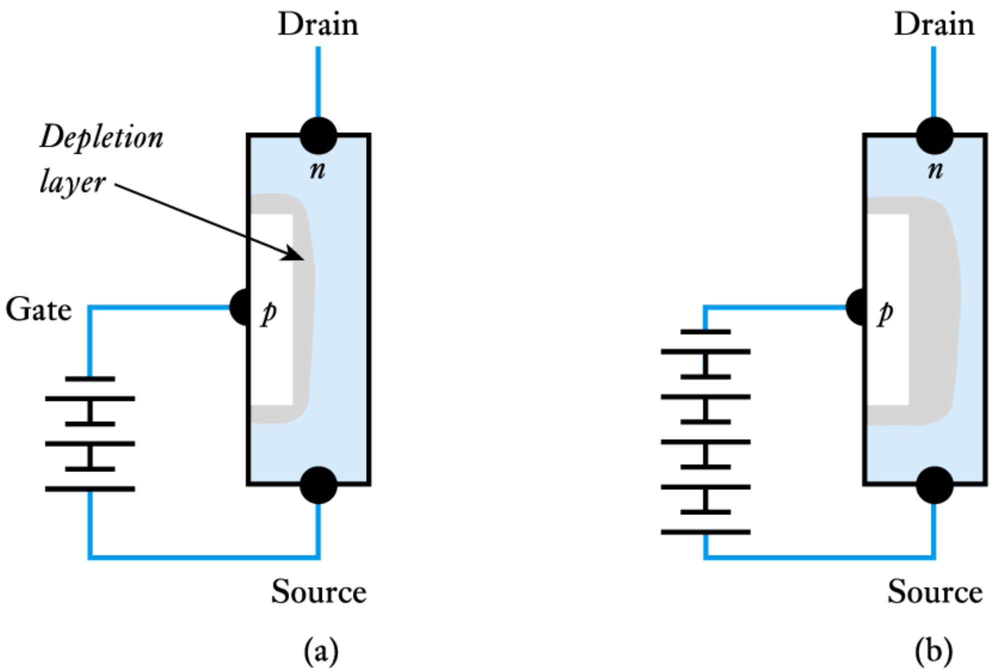
JFET

- **Construction (1 insert)**
  - – two polarities: *n*-channel and *p*-channel

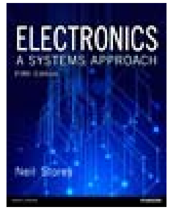


JFET

– the effect of varying the gate voltage (n-channel device)



– The greater the reverse bias, the narrower the conduction channel and the lower the drain-source current



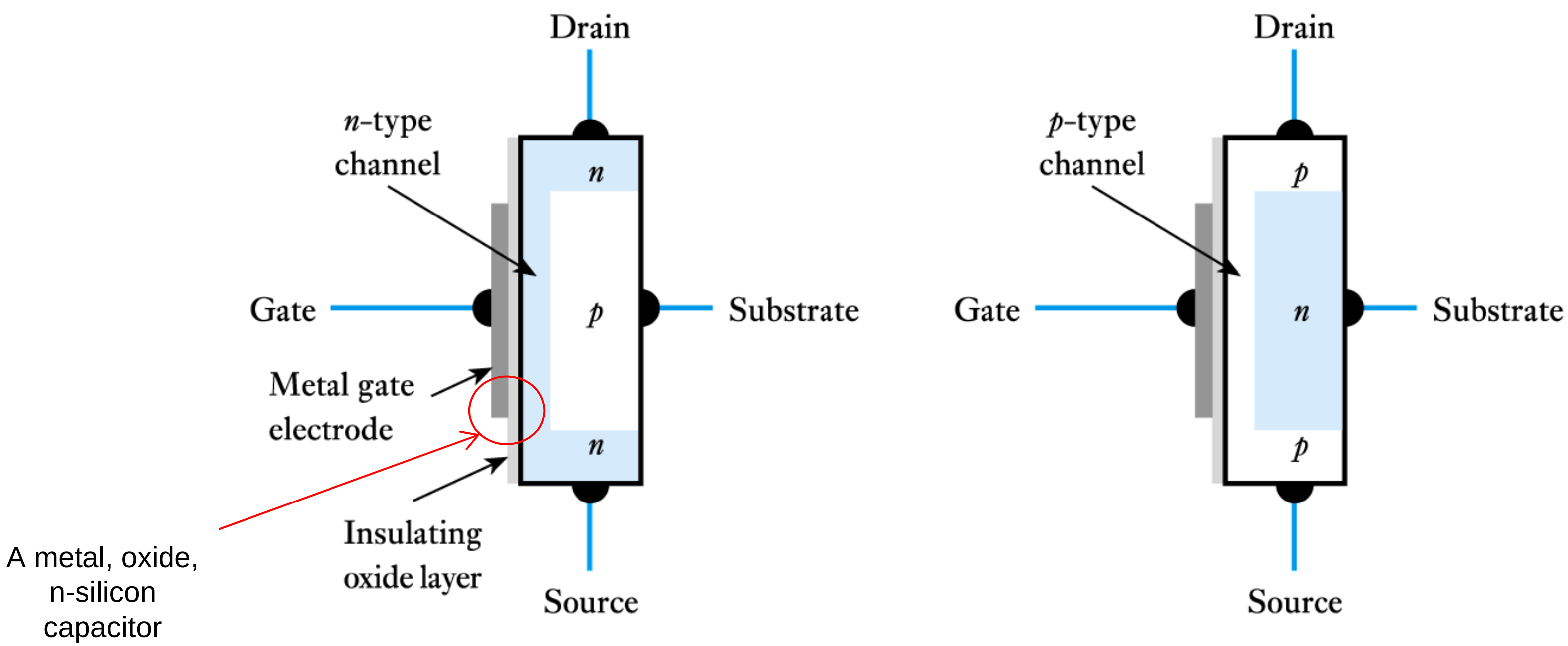
18.3

Insulated-gate field-effect transistors

- Such devices are sometimes called **IGFETs** (insulated-gate field-effect transistors) or sometimes **MOSFETs** (metal oxide semiconductor field-effect transistors)
- Digital circuits constructed using these devices are usually described as using **MOS technology**
- Here we will describe them as MOSFETs

DE-MOSFET

- **Construction**
  - – two polarities: *n*-channel and *p*-channel



(a) *n*-channel (b) *p*-channel

DE-MOSFET

- **Operation**
  - Gate voltage controls the thickness of the channel.
  - Consider an *n*-channel device
    - making the gate more *positive* attracts electrons to the gate and makes the electron (n) channel *thicker* – reducing the resistance of the channel. The channel is said to be **enhanced**
    - making the gate more *negative* repels electrons from the gate and makes the n-channel *thinner* – increasing the resistance of the channel. The channel is said to be **depleted**

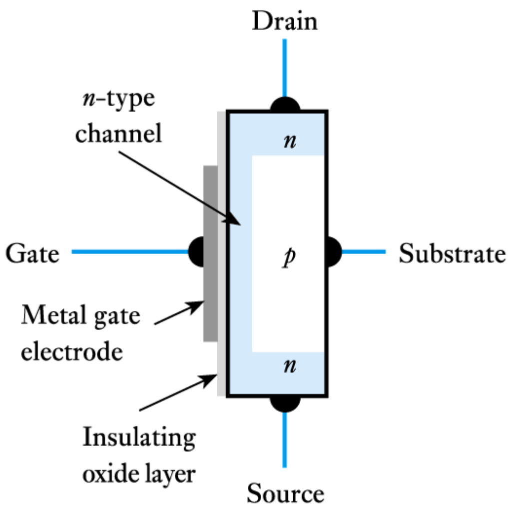
DE-MOSFET

– The effect of varying the gate voltage

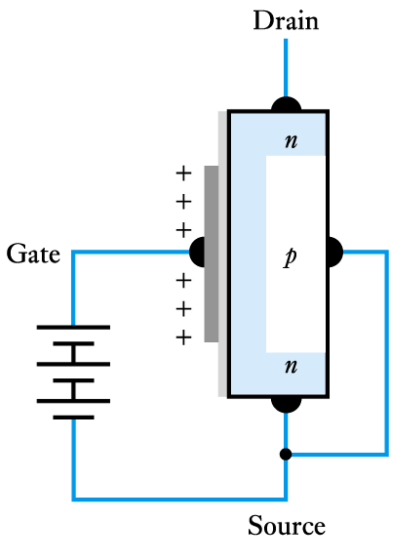
Un-biased

Enhanced channel ($V_G > V_S$)

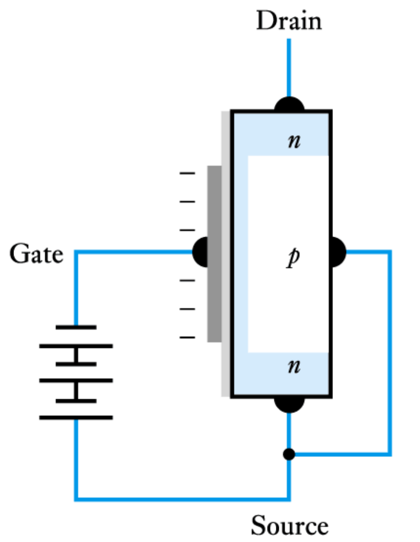
Depleted channel ($V_G < V_S$)



(a) n-channel



(a) positive gate voltage

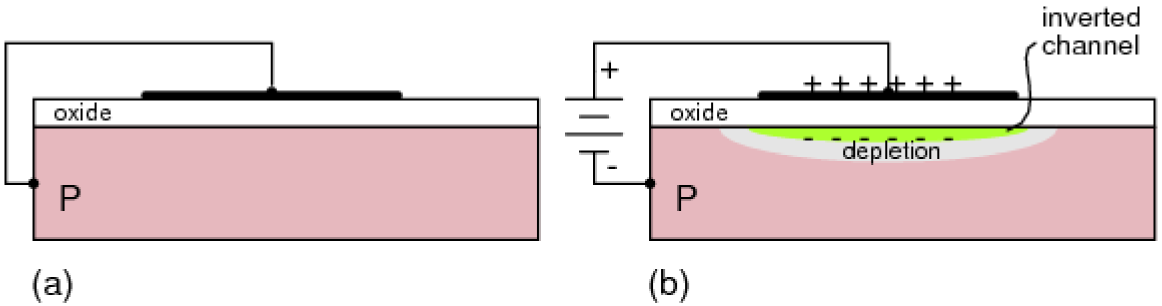


(b) negative gate voltage

- Devices as described are termed depletion-enhancement MOSFETs or simply **DE MOSFETs**
- Some MOSFETs are constructed so that in the absence of any gate voltage there is no channel
  – Such devices can be operated in an enhancement mode, but not in a depletion mode (since there is no channel to deplete)
  – These are called **Enhancement MOSFETs**
- Both forms of MOSFET are available as either *n*-channel or *p*-channel devices

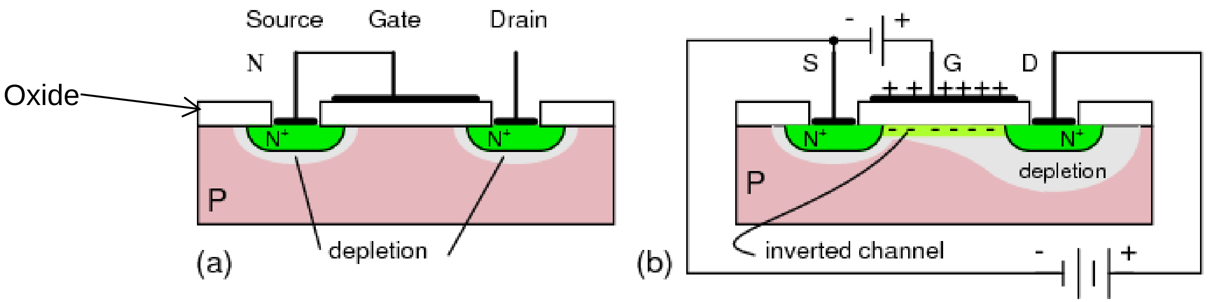
An enhancement MOSFET

- With no voltage on plate, just have MOS capacitor



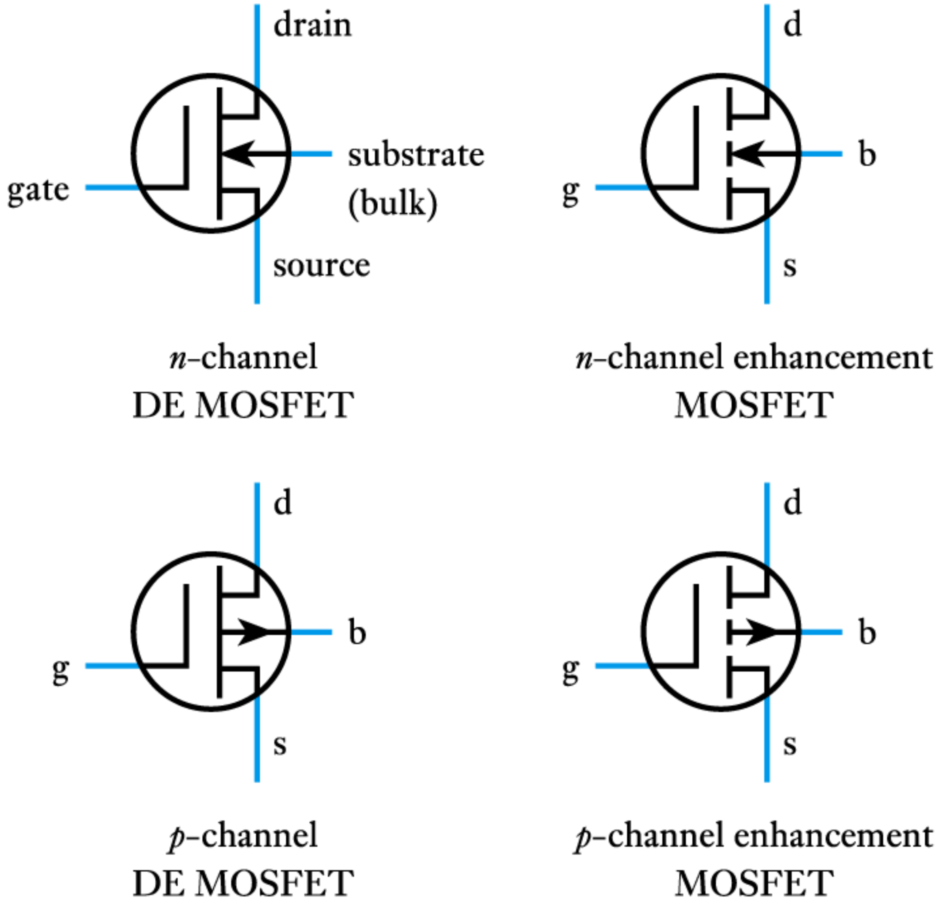
- Charge plate positive, attract electrons from the p-type Si towards the oxide dielectric (just like a capacitor).
- This creates an enriched electron channel under the oxide
- This will also create a depletion region that isolates the enhanced channel from the bulk silicon substrate.

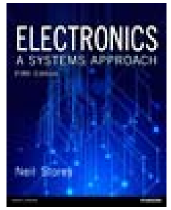
To get the voltage controlled current:



- Separate n-type materials are used for S and D and are embedded in the p-type material
- The separate pn-junctions allow diffusion of majority charge carriers, forming electric fields and isolated depletion regions
- Put the $+V_{GS}$ to create an enhanced electron channel between the two pn-junctions, allowing current to flow between them
- Resistance of channel depends on strength of the V_{GS} potential

- **MOSFET circuit symbols**



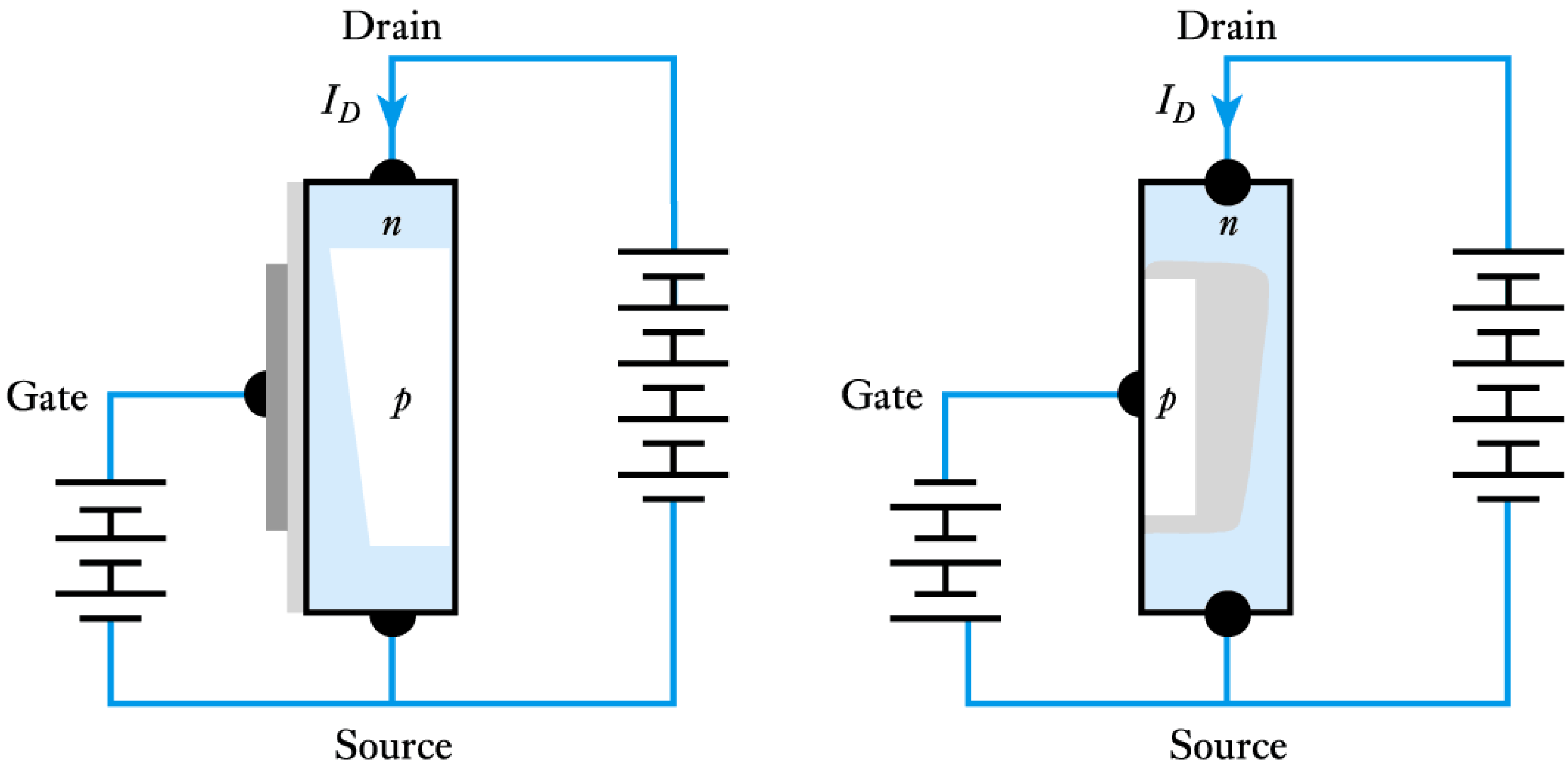


18.5

FET characteristics

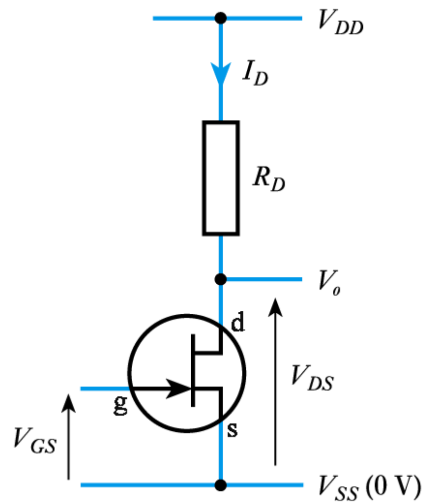
- While MOSFETs and JFETs operate in different ways, their characteristics are quite similar
- **Input characteristics**
  - in both MOSFETs and JFETs the gate is effectively insulated from the remainder of the device (no current in)
- **Output characteristics**
  - consider *n*-channel devices
  - usually the drain is more positive than the source
  - the drain voltage affects the thickness of the channel

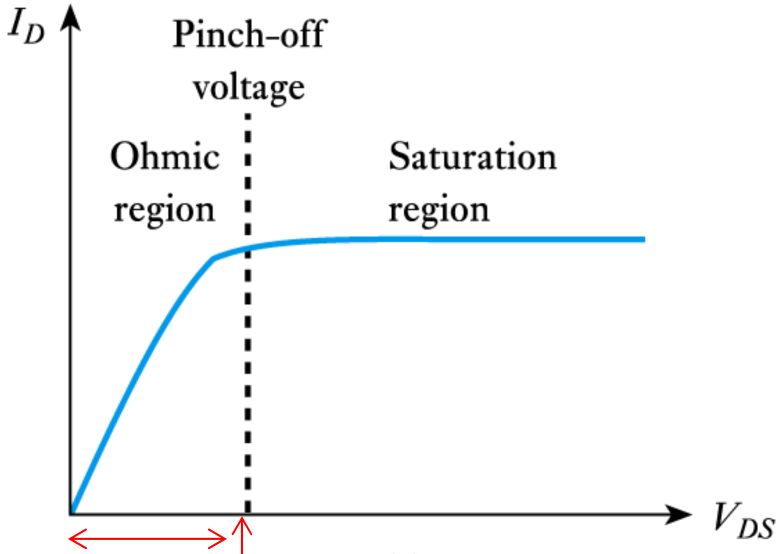
Effectively get a bias set up between the potential on the drain and the gate.
MOSFET $V_D > V_G \rightarrow$ depleted channel, $V_G > V_S \rightarrow$ enhanced channel
JFET $V_{GD} > V_{GS} \rightarrow$ larger reverse bias at drain end $\rightarrow$ larger depletion region
Tapers the channel.



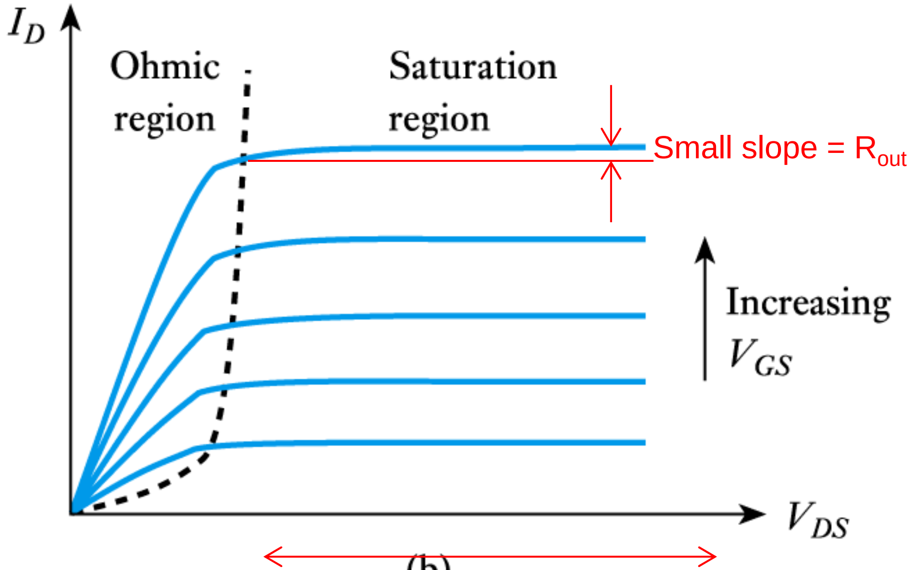
(a) MOSFET (b) JFET

▪ FET output characteristics





(a)



(b)

Here channel has resistance set by V_{GS}

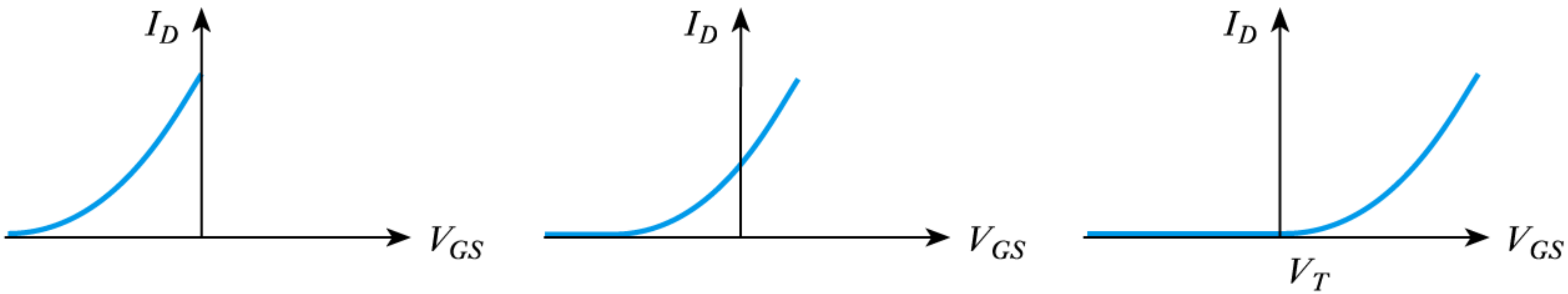
Above here the channel thickness is ≈ 0 at drain

Here I_D ~independent of the applied voltage & controlled by V_{GS}

Want to look at output versus input.

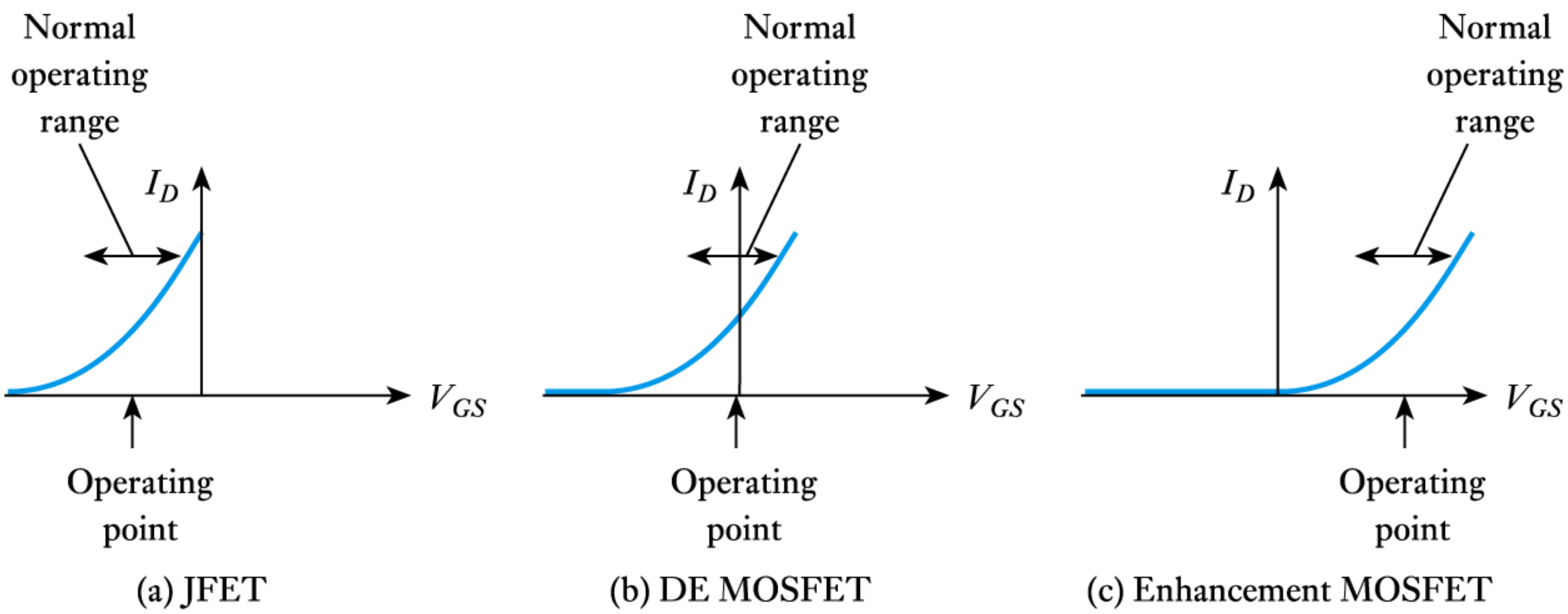
In saturation region, $V_{in} = V_{GS}$; output = I_D.

- **Transfer characteristics**
  - similar shape for all forms of FET – but with a different offset
  - not a linear response (≈parabolic), but over a small region might be considered to approximate a linear



(a) JFET (b) DE MOSFET (c) Enhancement MOSFET

Normal operating ranges for FETs



- When operating about its **operating point** we can describe the transfer characteristic by the *change* in output that is caused by a certain *change* in the input
  - This corresponds to the slope of the earlier curves
  - This quantity has units of current/voltage, which is the reciprocal of resistance (that is *conductance*)
  - Since this quantity describes the transfer characteristics it is called the **transconductance**, $\boldsymbol{g_m}$ (units $1/\Omega$ = Siemens)

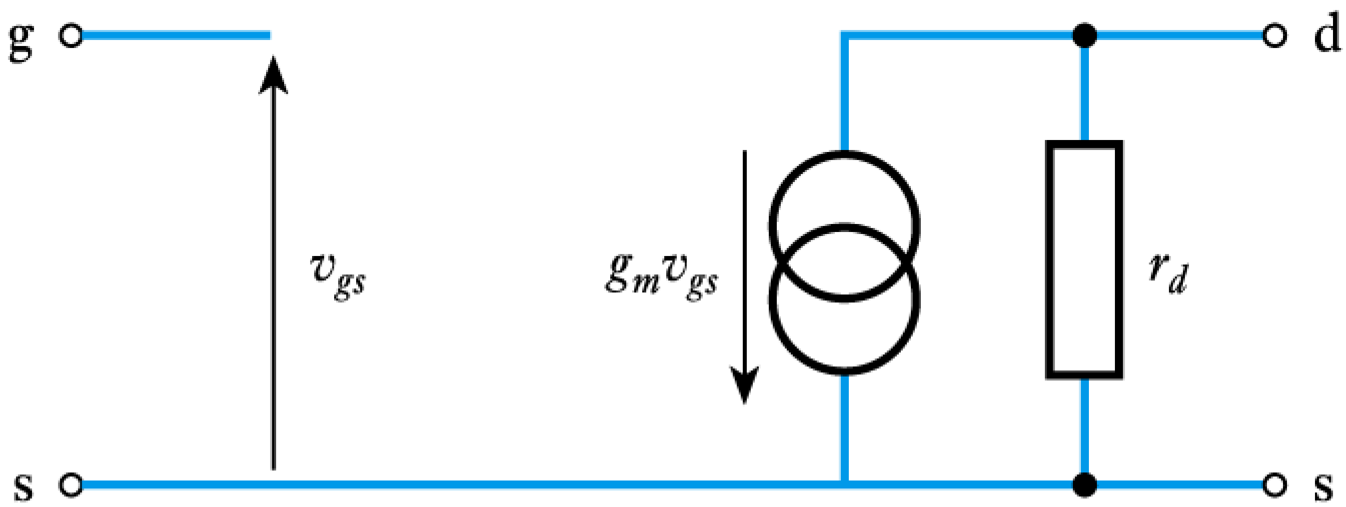
Note:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \quad \& \quad g_m \neq \frac{I_D}{V_{GS}}$$

Not a DC transfer device!

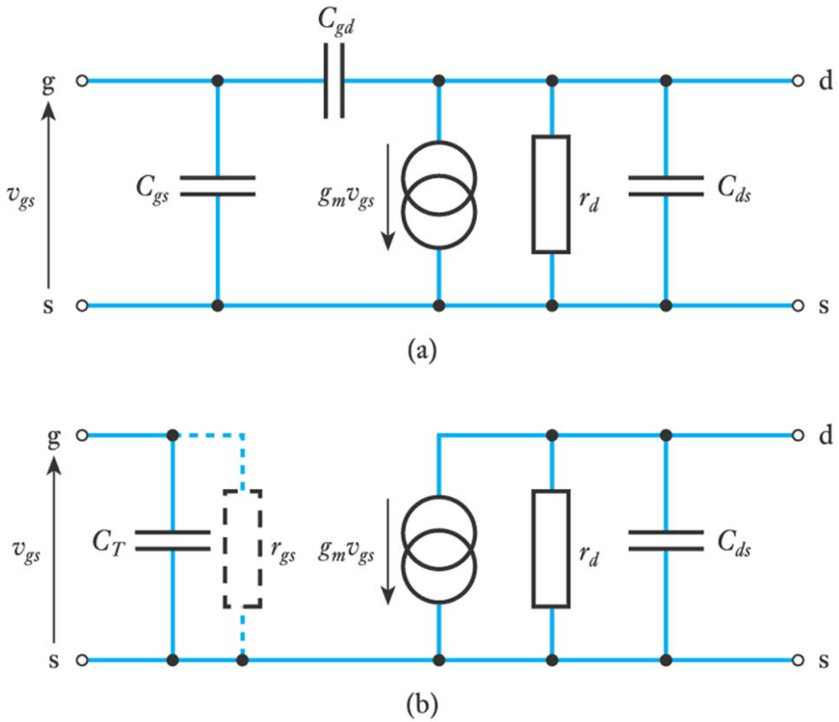
Since output is a current, I_D, model as a Norton output
Current "downward" out of phase with input

- **Small-signal (AC) equivalent circuit of a FET**
  - – models the behaviour of the device for small variations of the input about the operating point

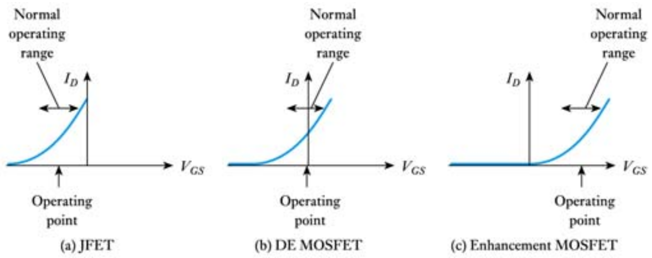


What happened to the DC voltages?

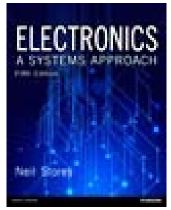
- **FETs at high frequencies**
  - at high frequencies more sophisticated models are used



FET amplifiers

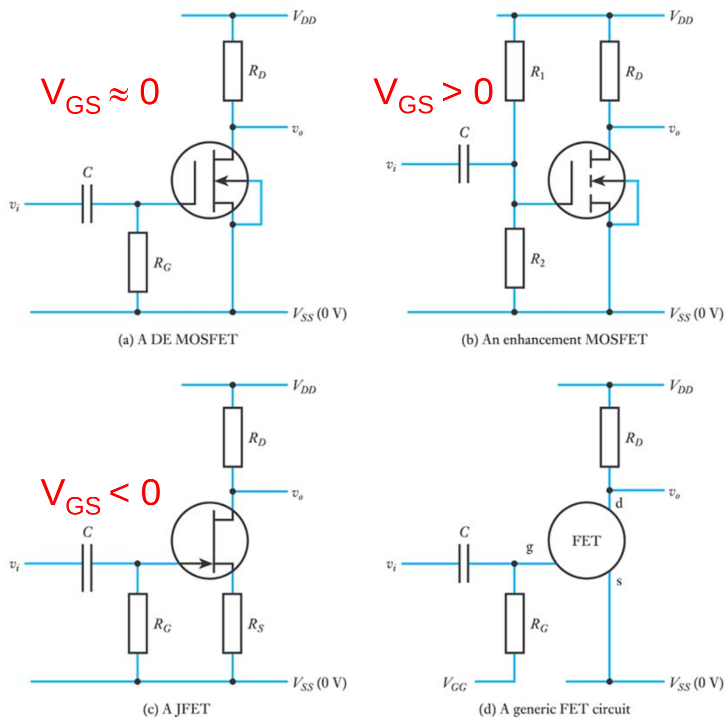


Video 18A

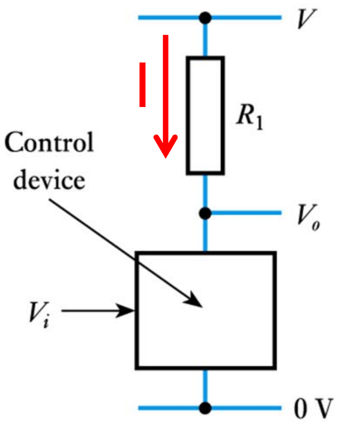


18.6

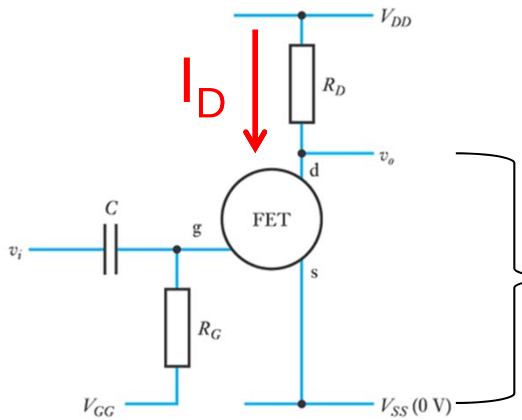
- Simple amplifiers can be formed using any kind of FET
  - Figure (a) shows a circuit using a **DE MOSFET**
  - Figure (b) uses an **enhancement MOSFET**
  - Figure (c) uses a **JFET**
  - Figure (d) is a generic circuit that could use any FET
  - These are **common source amplifiers**



Gain of device



A simple amplifier



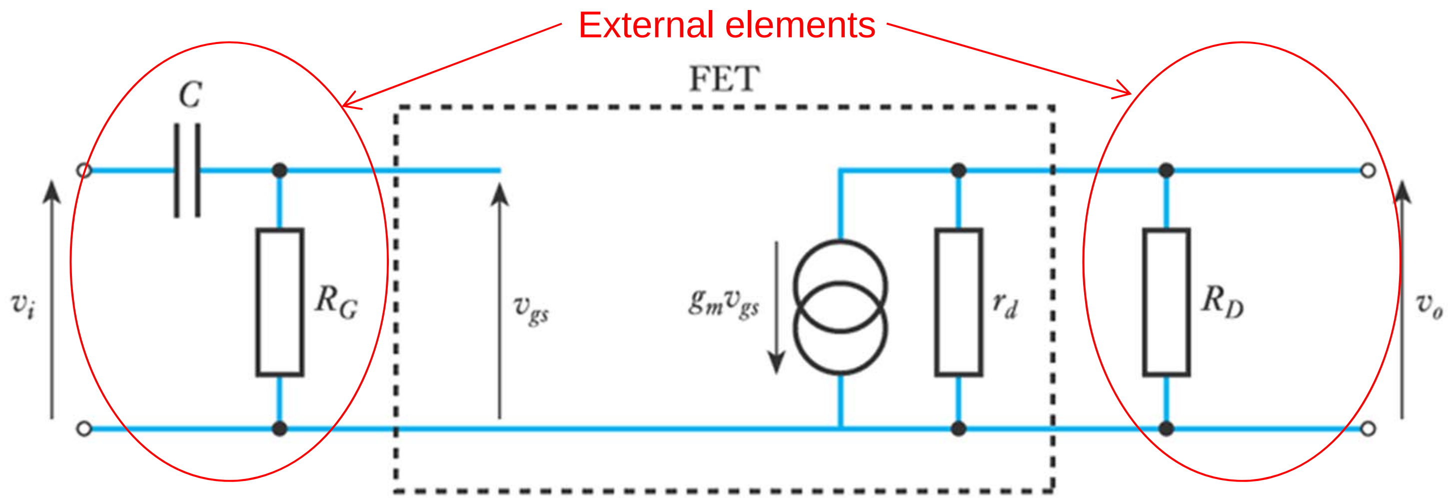
(d) A generic FET circuit

So, the FET is the control device and $V_{output} = V_{DD} - I_D \cdot R_D$

- When $V_i = V_{GS}$ increases, I_D increases
  - Almost as if the resistance of the control device gets smaller (it doesn't, R_o= constant)
- Then most of the voltage, V_{DD}, drops across R_D
  - Thus, Vo gets smaller
- Inverting amplifier
- V_{GS} decreases $\Rightarrow$ I_D decreases $\Rightarrow$ V_o increases

Equivalent circuit of a FET amplifier

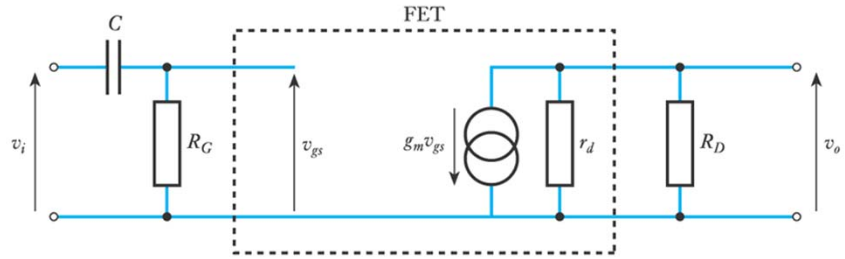
Video 18B



- This circuit can represent any of the FET amplifiers above (by choosing an appropriate value of R_G)
  - This is a **small signal-equivalent circuit**
  - Note that R_D goes to *ground*, since the supply voltage V_{DD} is a virtual earth point for small signals

Small-signal voltage gain

- From the equivalent circuit we can derive the small-signal voltage gain



V = I*R $\Rightarrow$ $$v_o = -g_m v_{gs}(r_d \,//\, R_D)$$

$$= -g_m v_i(r_d \,//\, R_D)$$

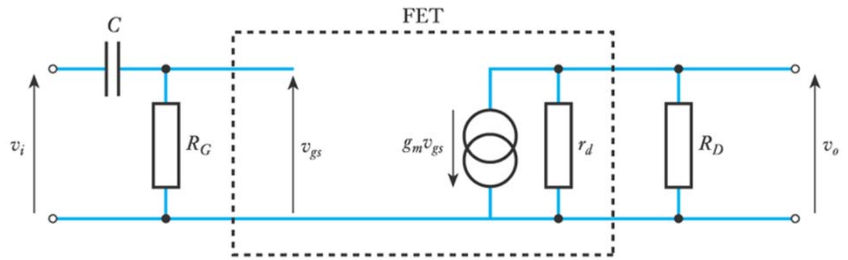
therefore

$$\frac{v_o}{v_i} = -g_m(r_d \,//\, R_D)$$

- Also

$$r_i \approx R_G \qquad\qquad r_o \approx r_d \,//\, R_D$$

- In many cases $r_d >> R_D$ so r_d can often be ignored
- If this is the case



$$\text{voltage gain} = \frac{v_o}{v_i} \approx -g_m R_D$$

$$r_i \approx R_G$$

$$r_o \approx R_D$$

Biasing considerations

- The biasing arrangement determines the operation of the circuit
  - This is its **quiescent** state
- The quiescent output voltage $v_{o(quies)}$ is given by

$$V_{o(quies)} = V_{DD} - I_{D(quies)} R_D$$

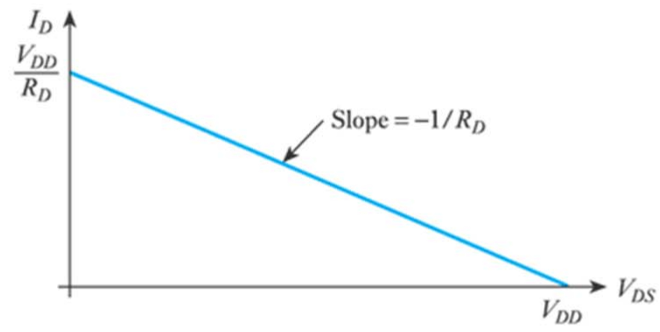
- However, since the FET is not linear, determining the quiescent conditions is not straightforward

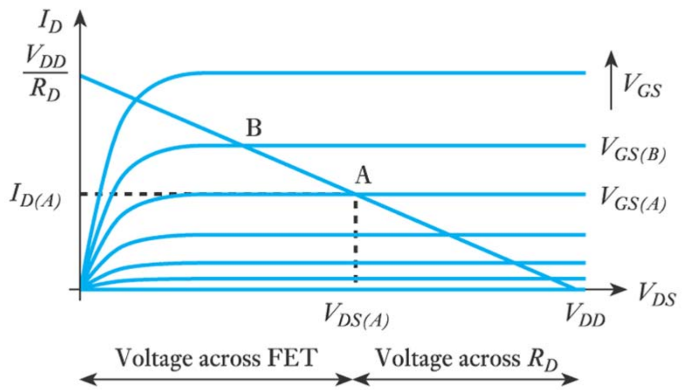
$V_{output} = V_{DS} = V_{DD} - I_D \cdot R_D$

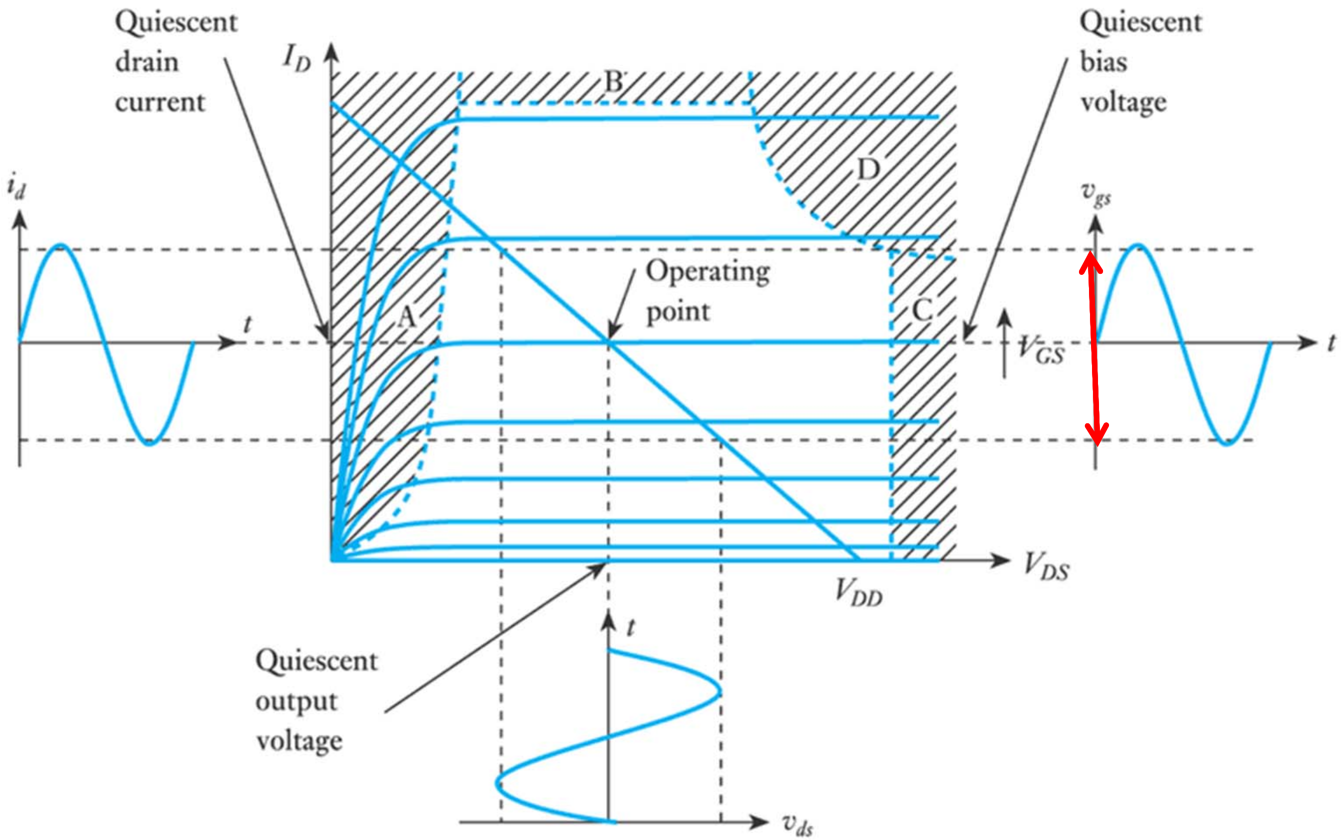
When $I_D = 0 \Rightarrow V_{DS} = V_{DD}$

When $V_{DS} = 0 \Rightarrow V_{DD} = I_D \cdot R_D$

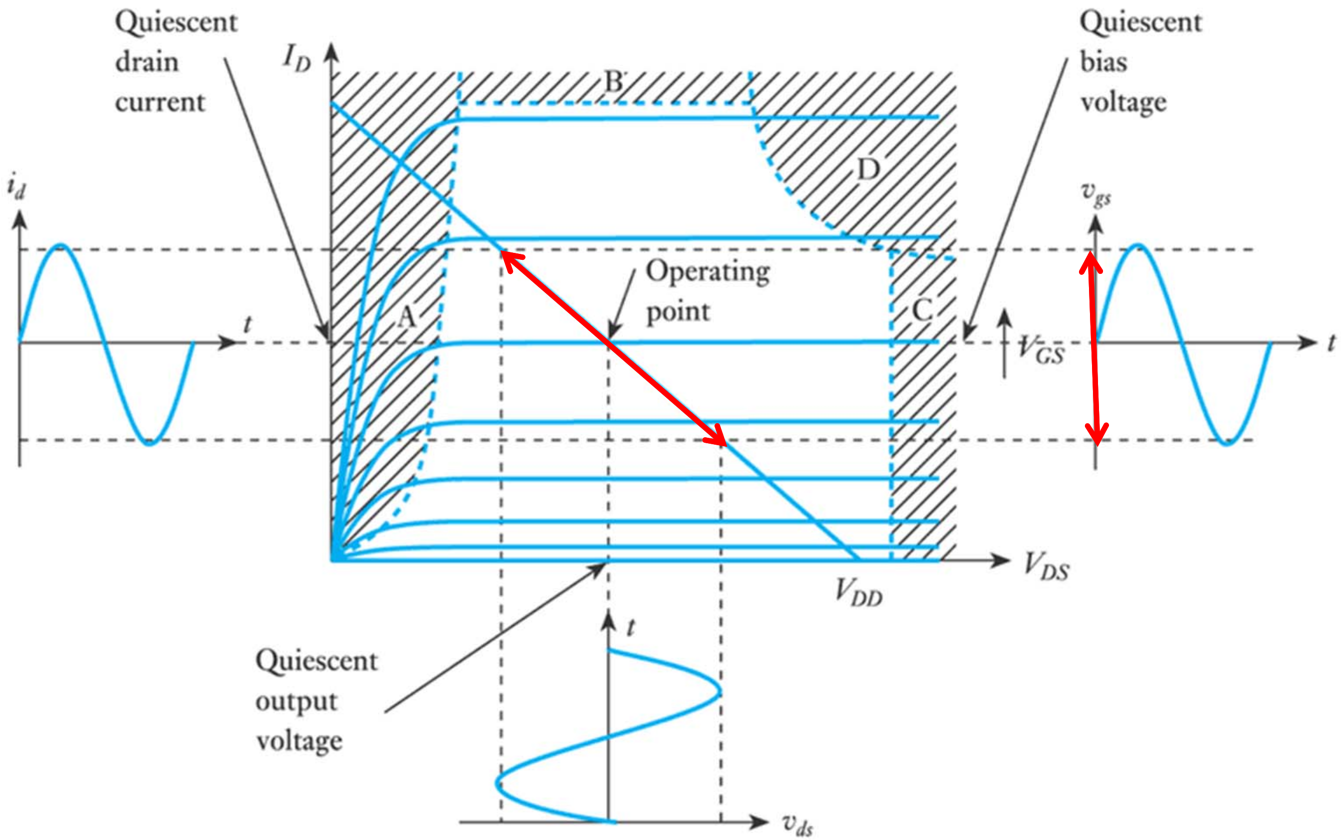
- One approach is to use a **load line**



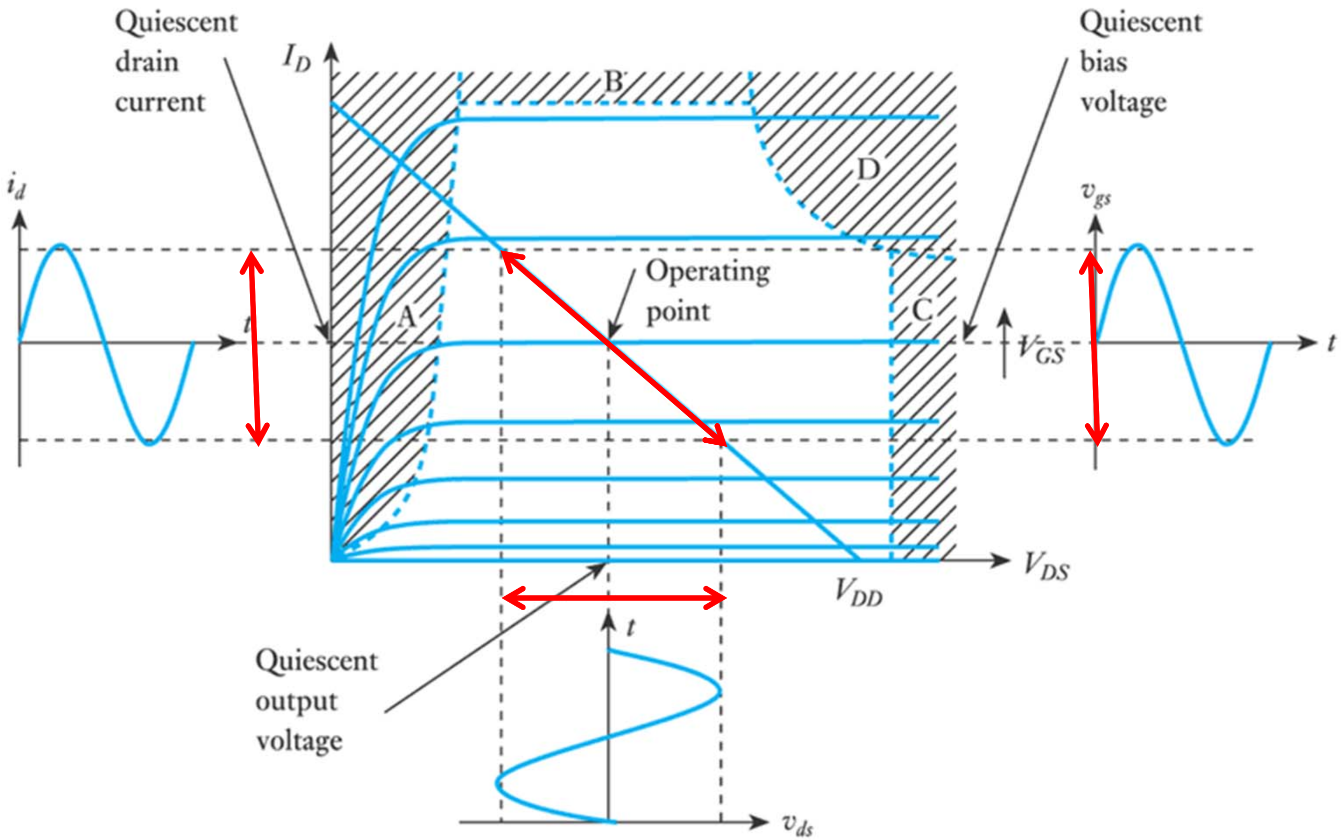




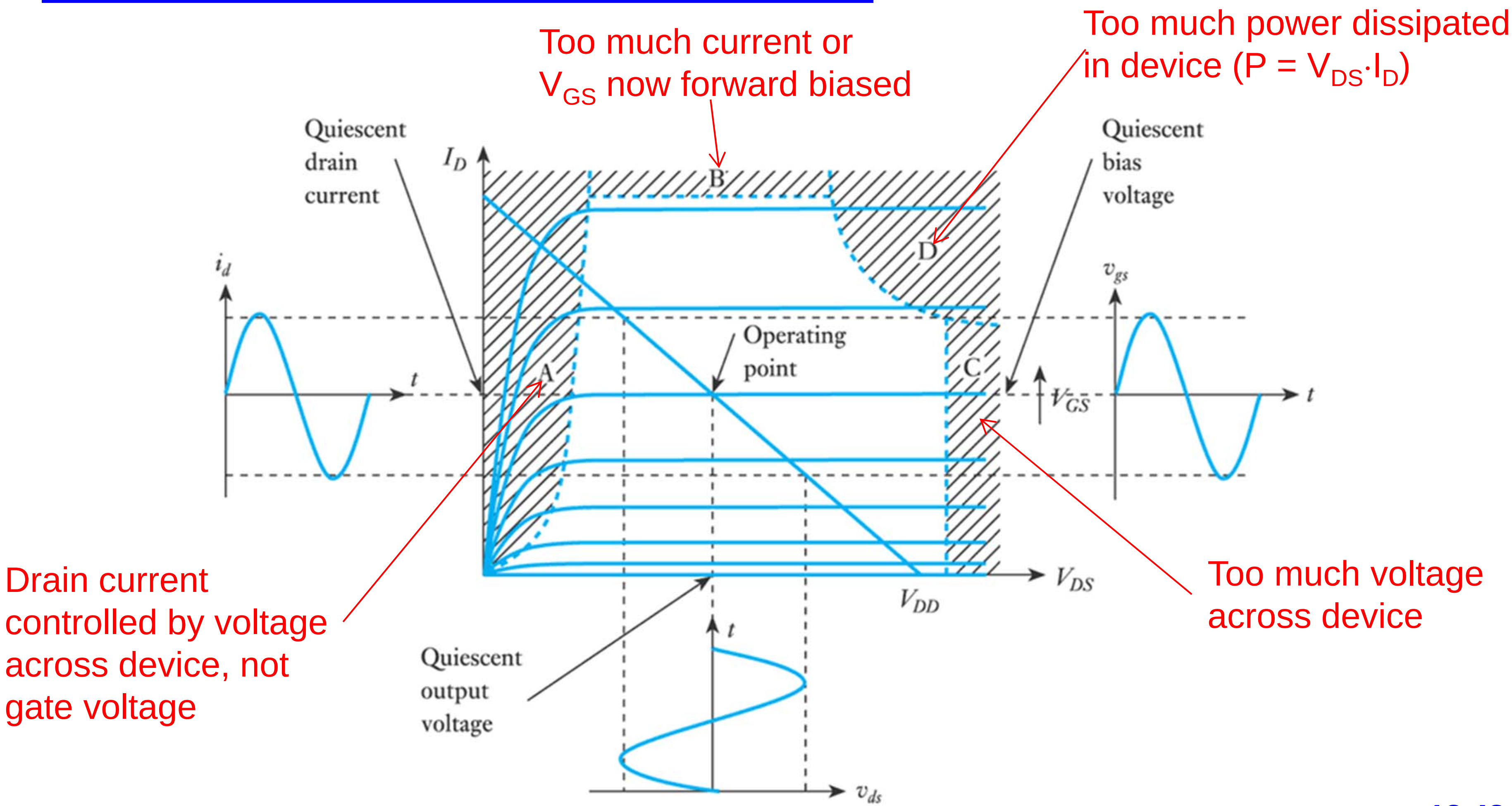
Quiescent
drain
current
I_D
B
D
A
Operating
point
C
Quiescent
bias
voltage
i_d
t
v_{gs}
V_{GS}
t
V_{DS}
V_{DD}
Quiescent
output
voltage
t
v_{ds}



Quiescent
drain
current
I_D
B
D
i_d
t
A
Operating
point
C
Quiescent
bias
voltage
v_{gs}
V_{GS}
t
V_{DS}
V_{DD}
Quiescent
output
voltage
t
v_{ds}



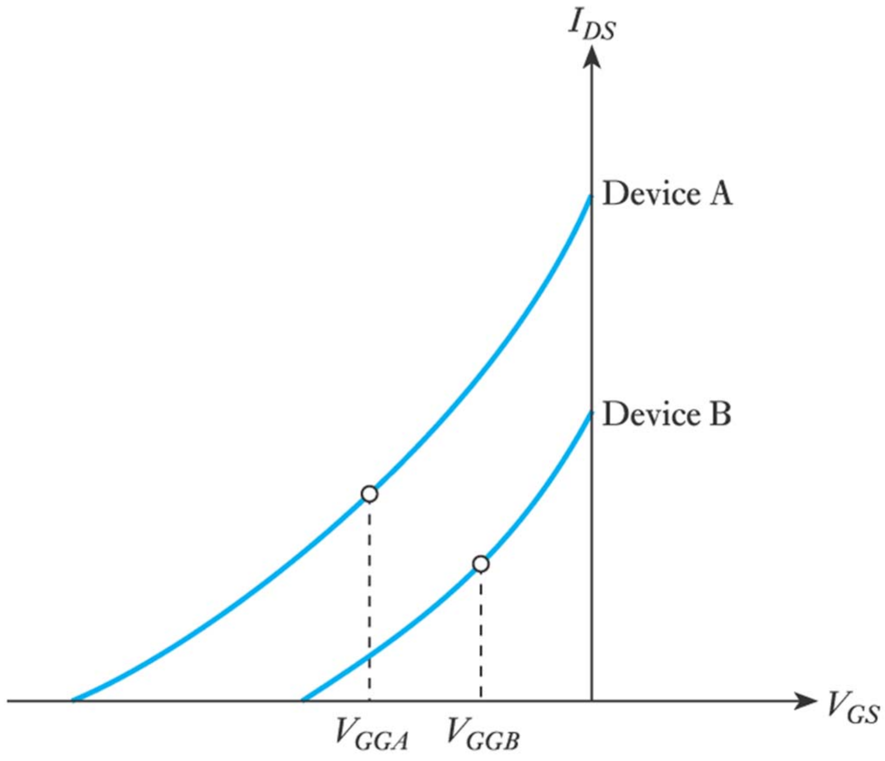
Quiescent
drain
current
I_D
B
D
i_d
A
Operating
point
C
v_{gs}
Quiescent
bias
voltage
t
V_{GS}
t
V_{DS}
V_{DD}
t
Quiescent
output
voltage
v_{ds}



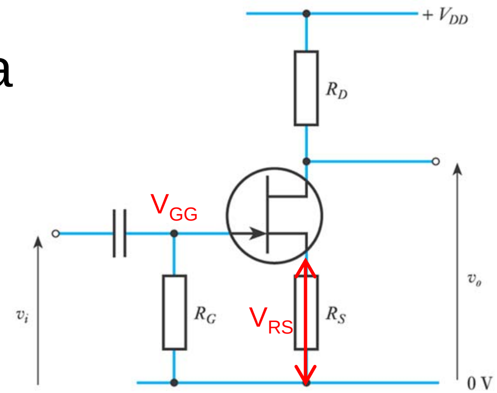
Too much current or
V_{GS} now forward biased
Too much power dissipated
in device ($P = V_{DS} \cdot I_D$)
Quiescent
drain
current
I_D
B
D
Quiescent
bias
voltage
i_d
v_{gs}
t
Operating
point
A
C
V_{GS}
t
V_{DS}
V_{DD}
Drain current
controlled by voltage
across device, not
gate voltage
Too much voltage
across device
t
Quiescent
output
voltage
v_{ds}

Device variability

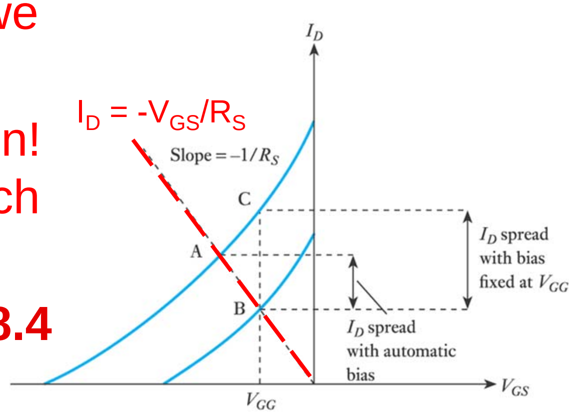
- FETs, like all active devices, suffer from variability



- The effects of device variability on the quiescent conditions of a circuit can be tackled using feedback
  - for example, the use of **‘automatic’ bias**
  - As we change V_{GS} we move along the $-1/R_S$ line when we have feedback
  - Stable, but large loss in gain! (I_D does not change as much for a change in V_{GS})
  - see **Examples 18.3 and 18.4** of the course text



(a) Circuit



(b) Effect on drain current

I_D increases

$V_{RS} = I_D \cdot R_S$ increases

V_{GG} the same so

V_{GS} more negative

So I_D decreases