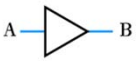
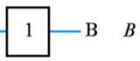
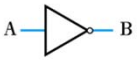
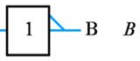
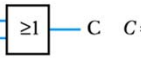
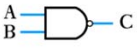
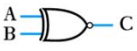
Chapter 24

Last time:
Digital systems-combinational logic

- Binary quantities and variables
- Logic gates
- Boolean algebra
- Combinational logic
- Boolean algebraic manipulation
- Algebraic simplification
- Karnaugh maps
- Propagation delay and hazards
- Number systems and binary arithmetic
- Examples of combinational logic design

Combinational logic building blocks

- The symbols shown earlier for the various logic gates are the '**distinctive shape**' symbols
- Other symbols are also used such as those described in IEC 617 (shown under 'Alternative symbol' here)

Function	Symbol	Alternative symbol	Boolean expression	Truth table
Buffer			$B = A$	A B 0 0 1 1
NOT			$B = \overline{A}$	A B 0 1 1 0
AND			$C = A \cdot B$	A B C 0 0 0 0 1 0 1 0 0 1 1 1
OR			$C = A + B$	A B C 0 0 0 0 1 1 1 0 1 1 1 1
NAND			$C = \overline{A \cdot B}$	A B C 0 0 1 0 1 1 1 0 1 1 1 0
NOR			$C = \overline{A + B}$	A B C 0 0 1 0 1 0 1 0 0 1 1 0
Exclusive OR			$C = A \oplus B$	A B C 0 0 0 0 1 1 1 0 1 1 1 0
Exclusive NOR			$C = \overline{A \oplus B}$	A B C 0 0 1 0 1 0 1 0 0 1 1 1

- **Further design examples**
  - The text contains further combinational logic design examples:
  - **Example 24.28:** A 4-input multiplexer

Key points

- Logic circuits are usually implemented using logic gates
- Circuits in which the output is determined solely by the current inputs are termed combinational logic circuits
- Logic functions can be described by truth tables or using Boolean algebraic notation
- Boolean expressions can often be simplified by algebraic manipulation, or using techniques such as Karnaugh maps
- Binary digits may be combined to form digital words that can be processed using binary arithmetic
- Several codes can be used to represent different forms of information

Further Study

Video 24H Further Study

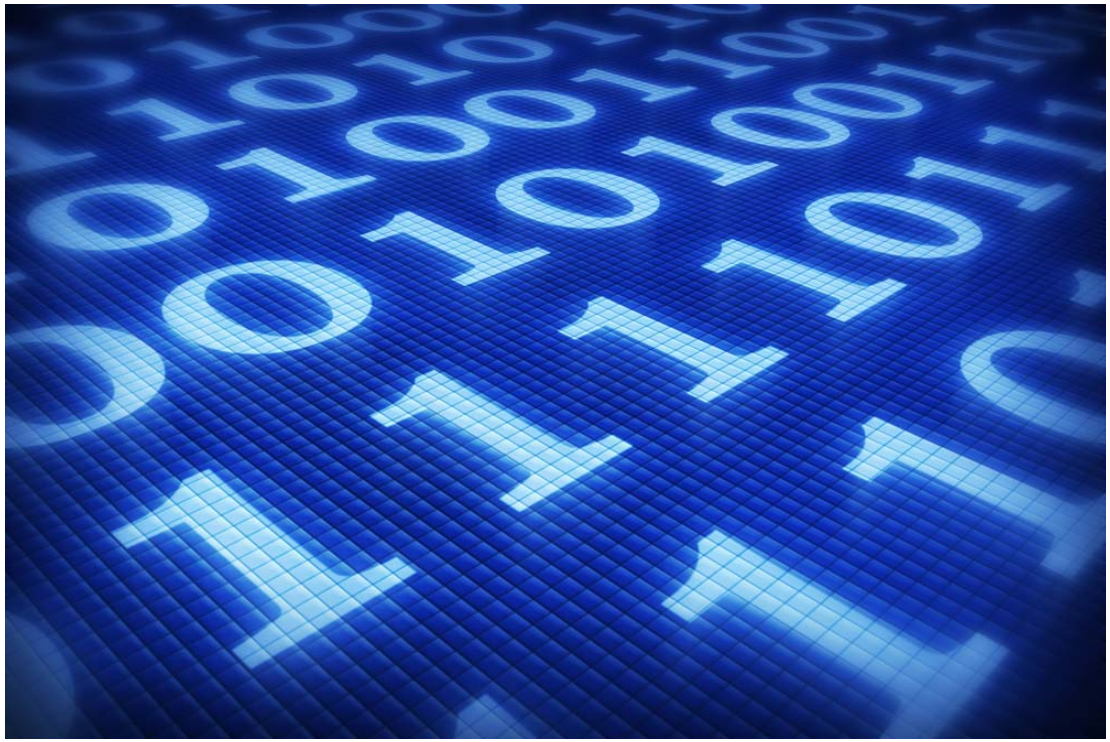
- The Further Study section at the end of Chapter 24 is concerned with the design of fault tolerant arrangements, such as those used within critical systems within aircraft.

- Your task is to design a simple ‘voting’ arrangement, that allows a system to continue working correctly even in the event of a fault.
- Try the design and then look at the video.

Chapter 25

Sequential logic

- Introduction
- Bistables
- Monostables or one-shots
- Astables
- Timers
- Memory registers
- Shift registers
- Counters



Introduction

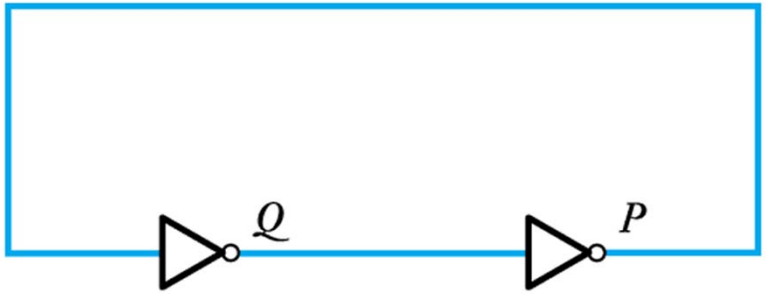
Video 25A

25.1

- Sequential logic is built with combinational logic elements
- Combines the characteristics of combinational logic with **memory**
- When constructing sequential logic circuits our building blocks are often some form of **multivibrator**
  - A term used to describe a range of circuits
    - these have two outputs that are the inverse of each other
    - the output are labelled Q and $\overline{Q}$
    - three basic forms:
      - **Bistables (flip-flops or latches)**
      - **Monstables (one-shots)**
      - **Astables (digital oscillators)**

Bistables

- **A regenerative switching circuit**



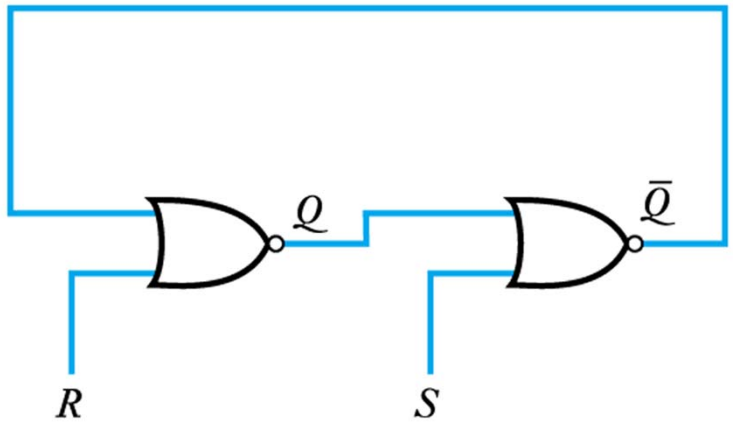
- This arrangement has two stable states
  - It will stay in whichever state it finds itself
- It is a form of bistable – though not a very useful one

S going high **S**ets Q to 1
R going high **R**e-sets Q to 0
Re-setting or setting several times does not affect Q

- **The *S-R* Latch**

NOR

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0



With R and S = 0

$\overline{Q}$ =0, Q=1→$\overline{Q}$ =0 or

$\overline{Q}$ =1, Q=0→$\overline{Q}$ =1

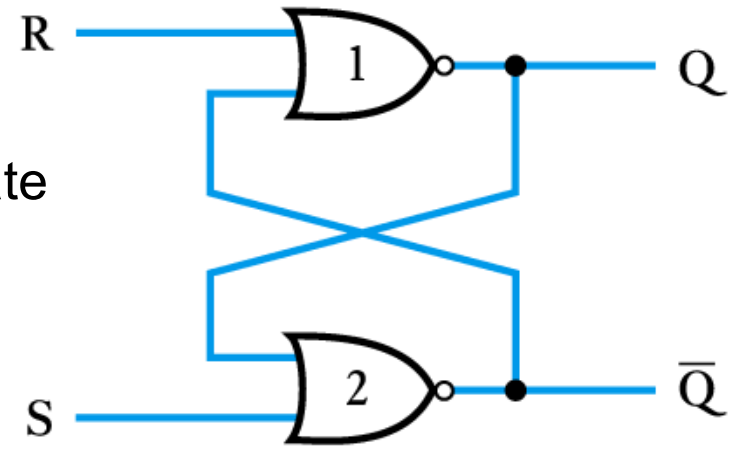
If S↑ 1 briefly, $\overline{Q}$ ↓0
and Q switches to 1

- Replacing the inverters with NOR gates produces a more useful circuit
  - The circuit still has two stable states
  - But now the inputs can switch it between these states

S going high sets Q to 1
R going high re-sets Q to 0
Re-setting or setting several times does not affect Q

The *S*-*R* latch (SET-RESET latch)

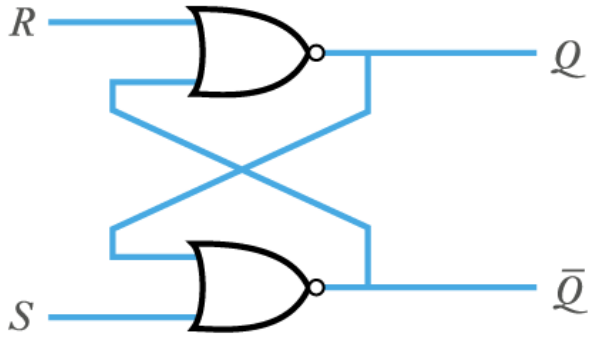
- More often drawn like this
  - when $R = S = 0$
    - Circuit stays in current state
  - when $S = 1$, $R = 0$
    - Q is **SET** to 1 ($\overline{Q} = 0$)
  - when $S = 0$, $R = 1$
    - Q is **RESET** to 0 ($\overline{Q} = 1$)
  - when $S = 1$, $R = 1$
    - Both outputs at 0 – not allowed



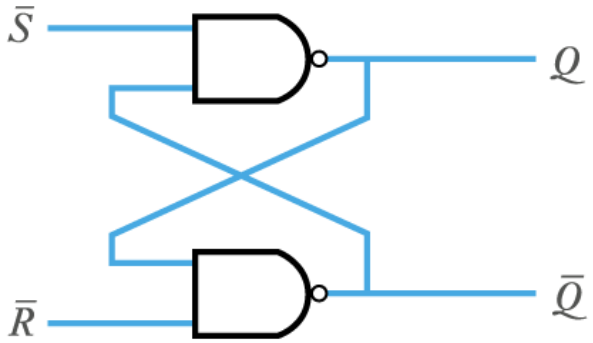
Active Low

Š going low sets Q to 1
Ř going low re-sets Q to 0
Re-setting or setting several times does not affect Q

- An *S*-*R* latch can also be produced using NAND gates
  - produces an **active-low circuit (Š or Ř = 0 set/reset)**



(a) An S–R latch using two NOR gates.

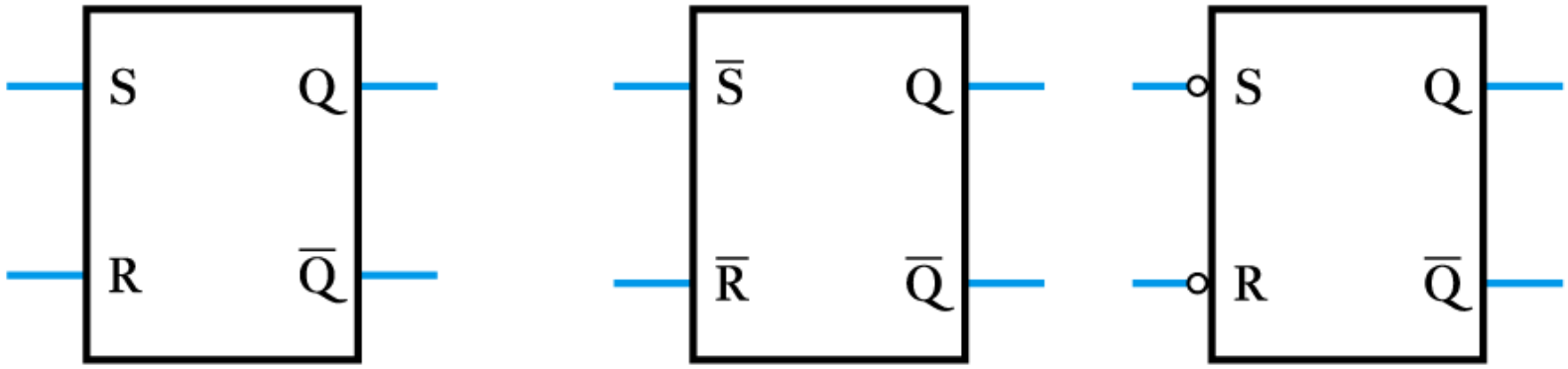


(b) An S–R latch using two NAND gates.

R=S=0 → Memory State
R=0, S=0 →1 sets Q=1
R=0 →1, S=0 re-sets Q=0
R=S=1 undetermined

Ř= Š =1 → Memory State
Ř=1, Š=1 →0 sets Q=1
Ř=1 →0, Š=1 re-sets Q=0
Ř=Š=0 undetermined

- ***S-R* latch logic symbols**

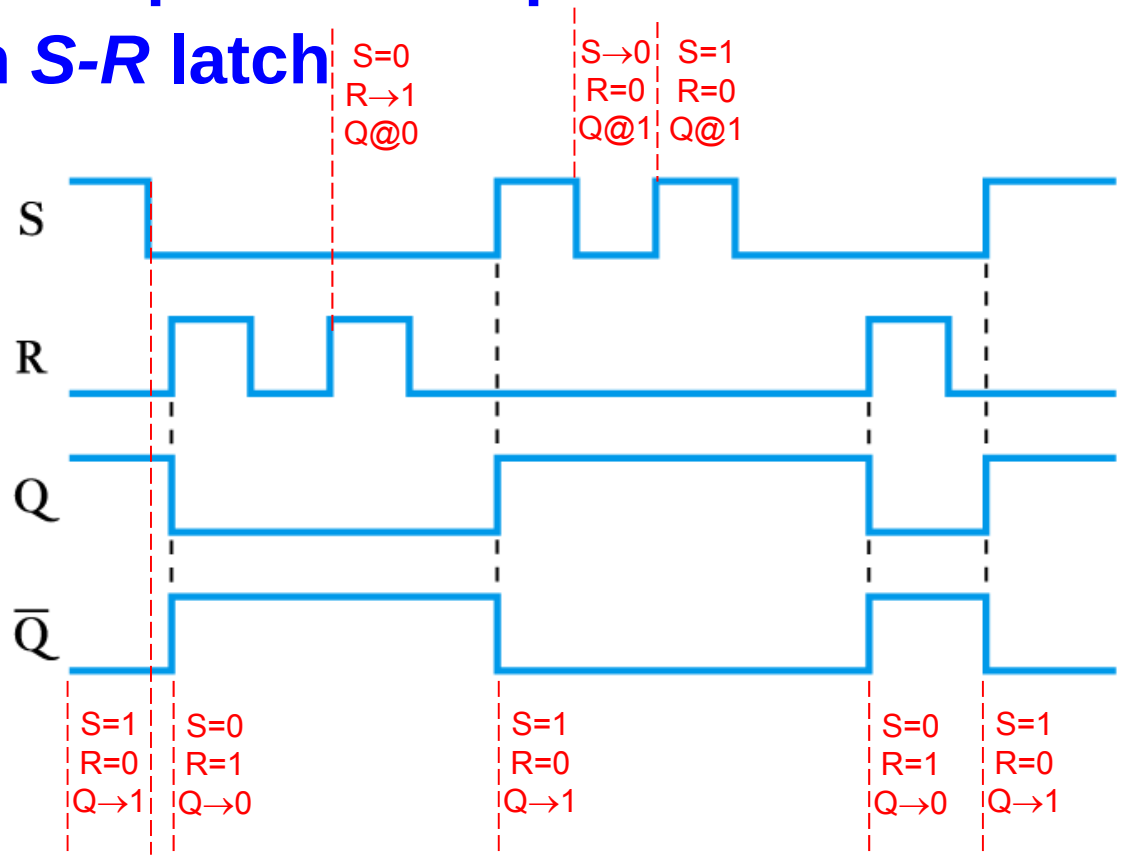


(a) Active high inputs

(b) Active low inputs

S going high sets Q to 1
R going high re-sets Q to 0
Re-setting or setting several times does not affect Q

- **Sample input and output waveforms for an *S-R* latch**

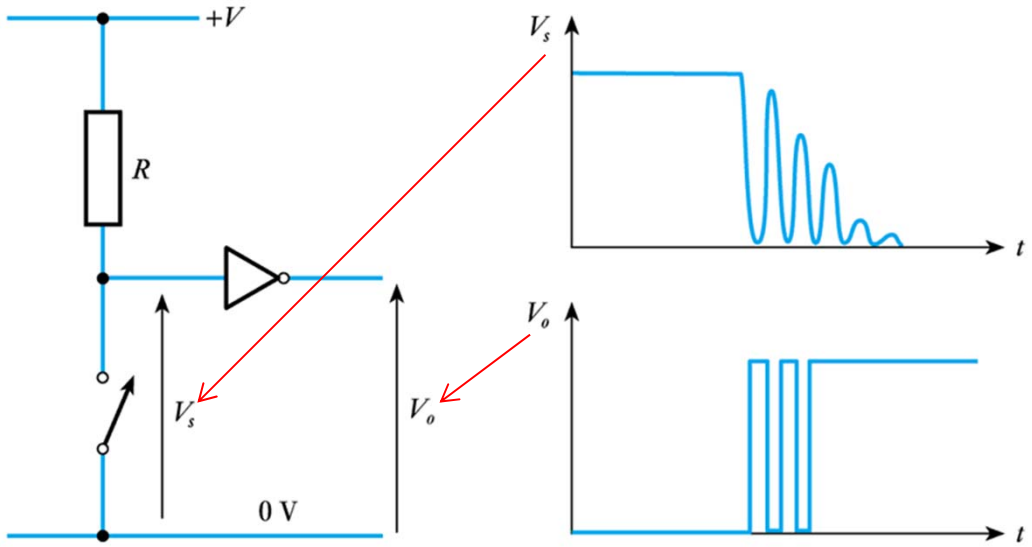


So What?

- **A design example** - see **Example 25.1** in course text

Use of an *S-R* latch in switch debouncing

- All mechanical switches suffer from switch bounce
- Switch makes and breaks contact several times

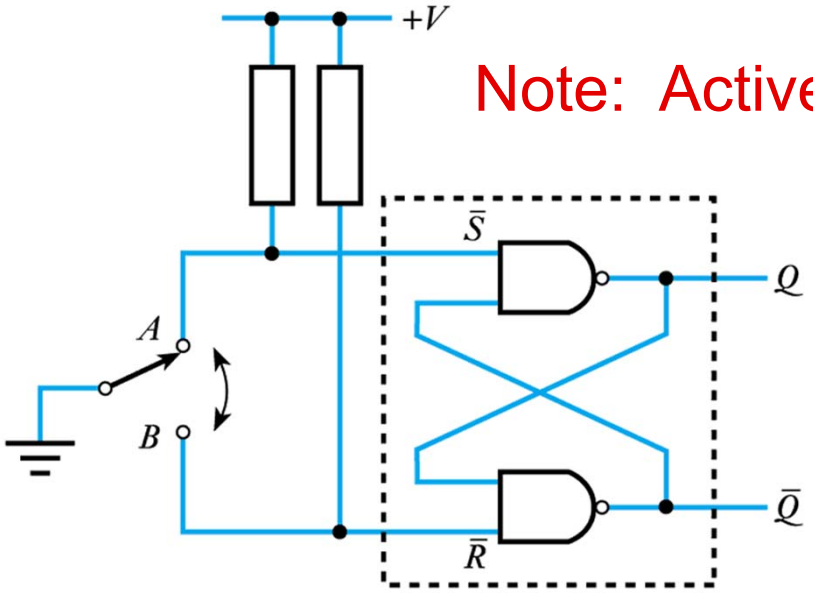


Š going low sets Q to 1

Ř going low re-sets Q to 0

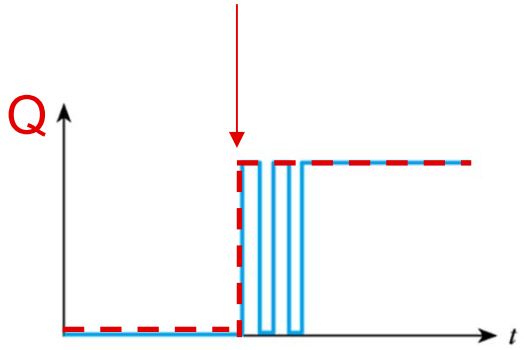
Re-setting or setting several times does not affect Q

- **A design example (continued)**
  - Problem can be tackled using an *S*-*R* bistable and a changeover switch (when A breaks contact, line goes low)



Note: Active Low Latch

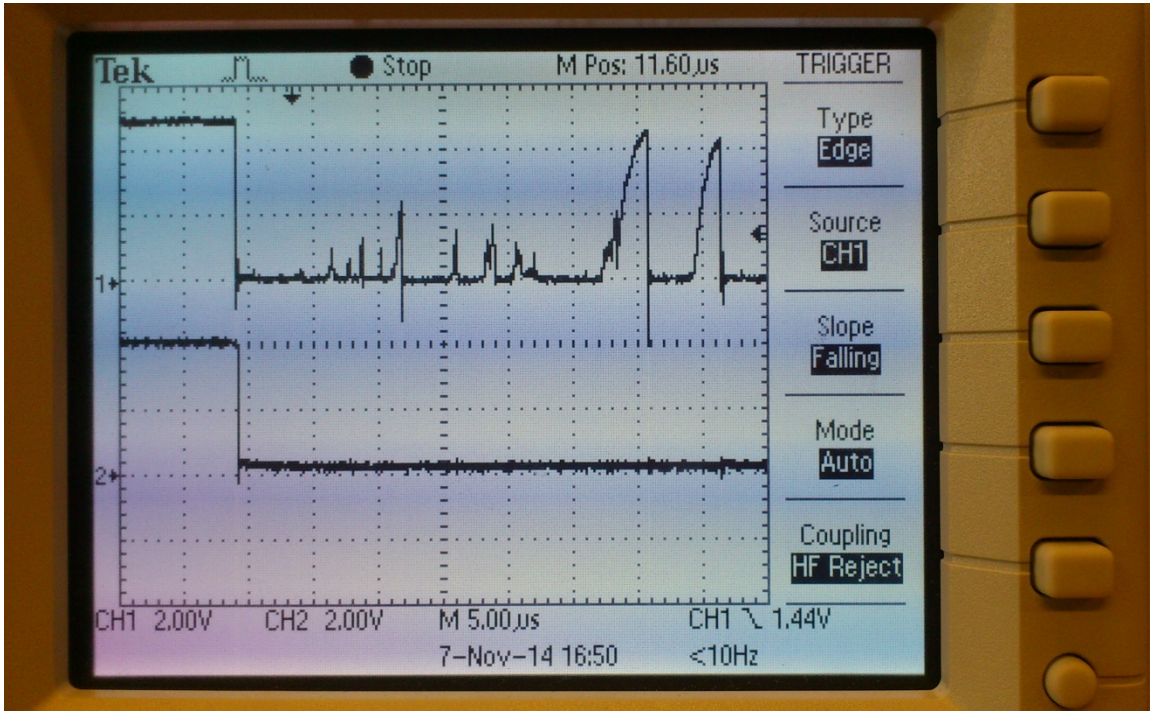
Switch B→A



Sometimes the lecture topics really happen!!

Top trace-at switch

Bottom-at output of the latch

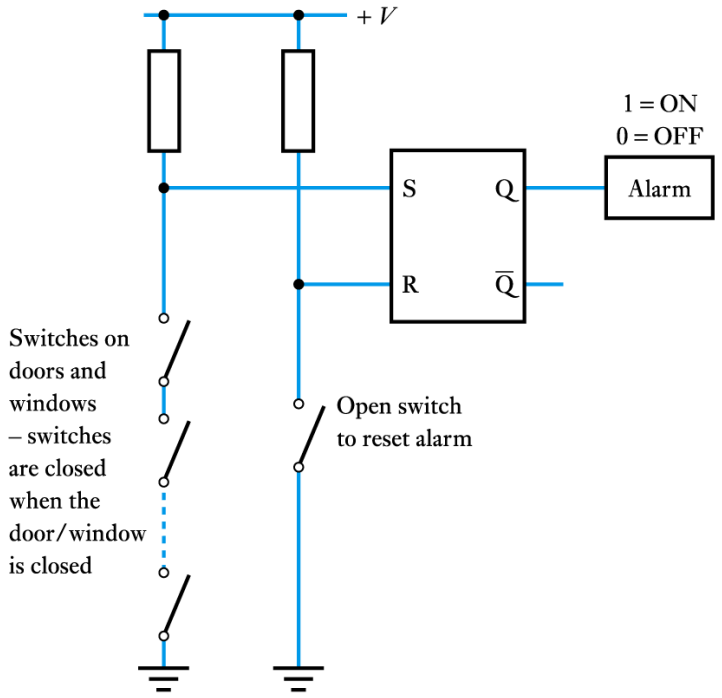


Picture by Lise Kvalø

- **A design example -** see **Example 25.2** in course text

A Burglar Alarm

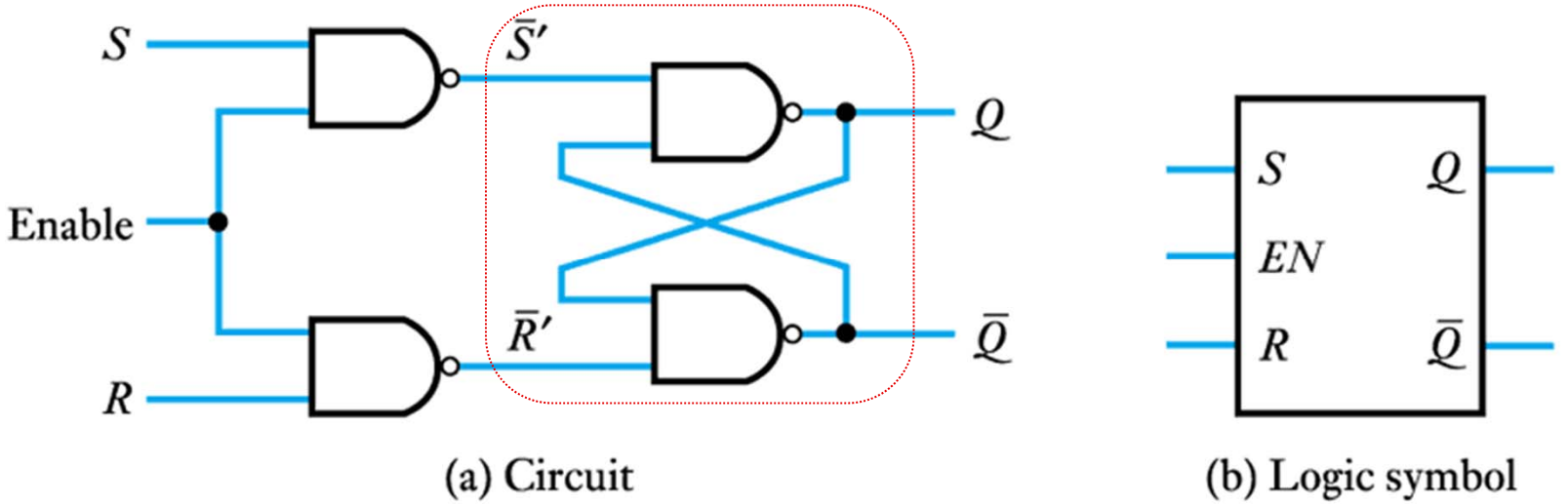
- Close all doors and window (closing switches)
- open reset switch to initialise system
- opening any of the door/window switches will activate alarm.
- alarm will continue if switch is then closed
- alarm is silenced by opening reset switch



In the fine tradition of this course, let's look at variations on a theme!

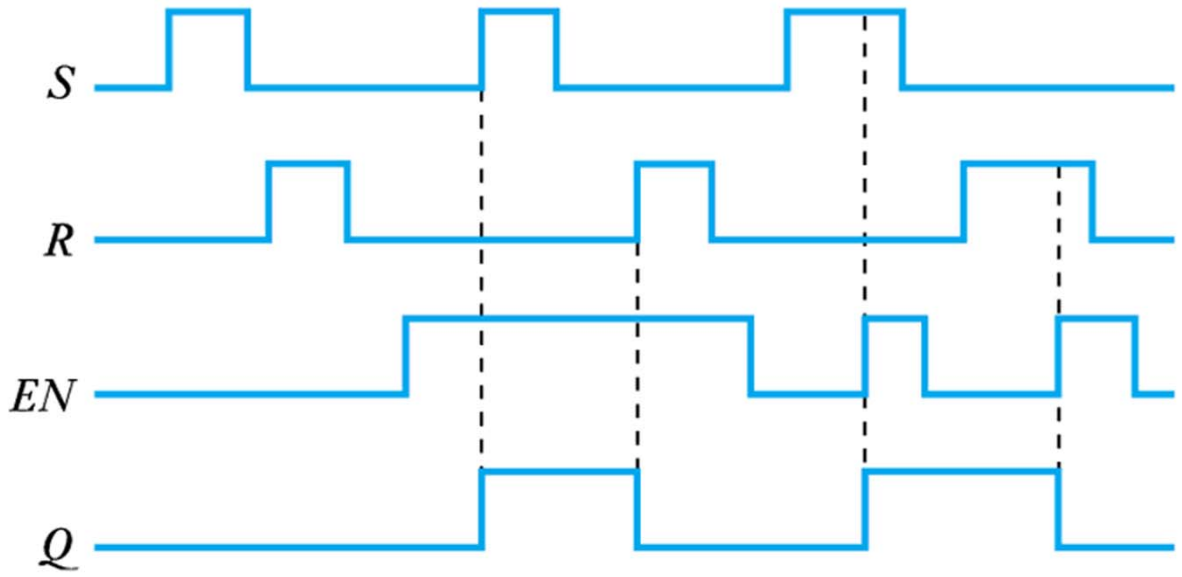
- **The gated *S-R* latch.**

Note: Active Low Latch

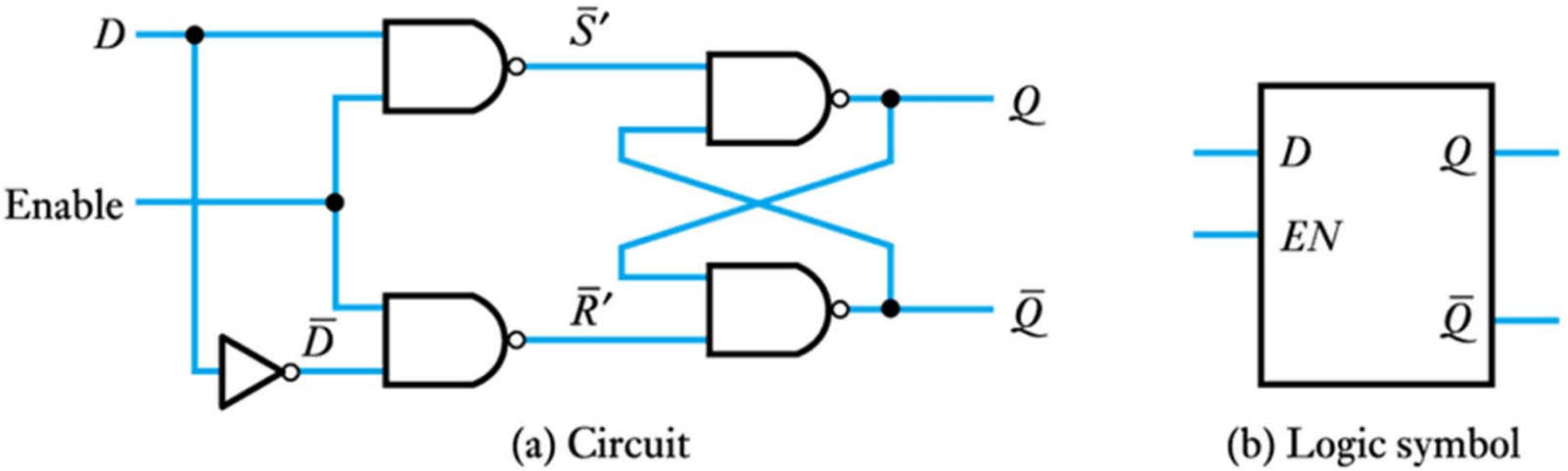


Start with Q=0, and S, En and R all 0 → Memory state
If R or S go High, but En stays low, Nothing happens!

- **Sample input and output waveforms for a gated *S*-*R* latch**

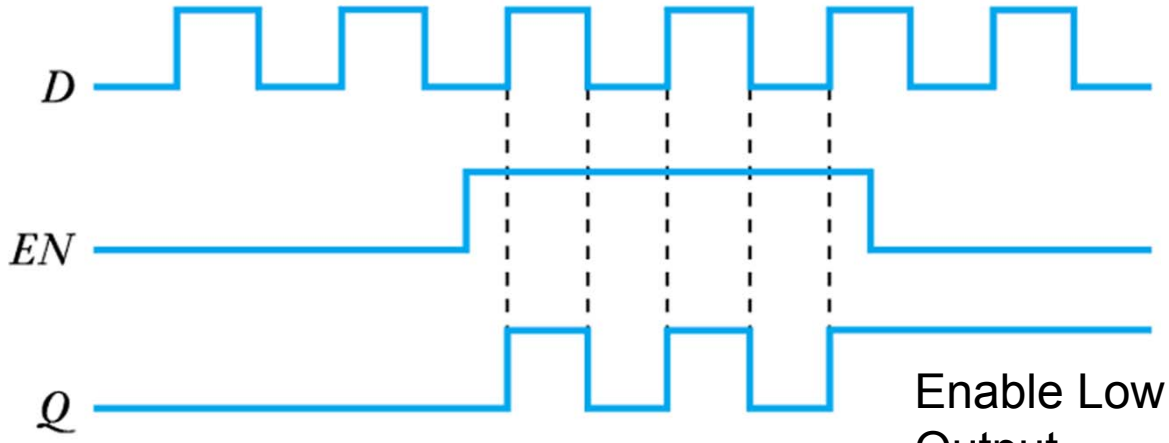


- **The *D* latch-a particular type of enabled latch with one external input, D**



- **Sample input and output waveforms for a *D* latch.**

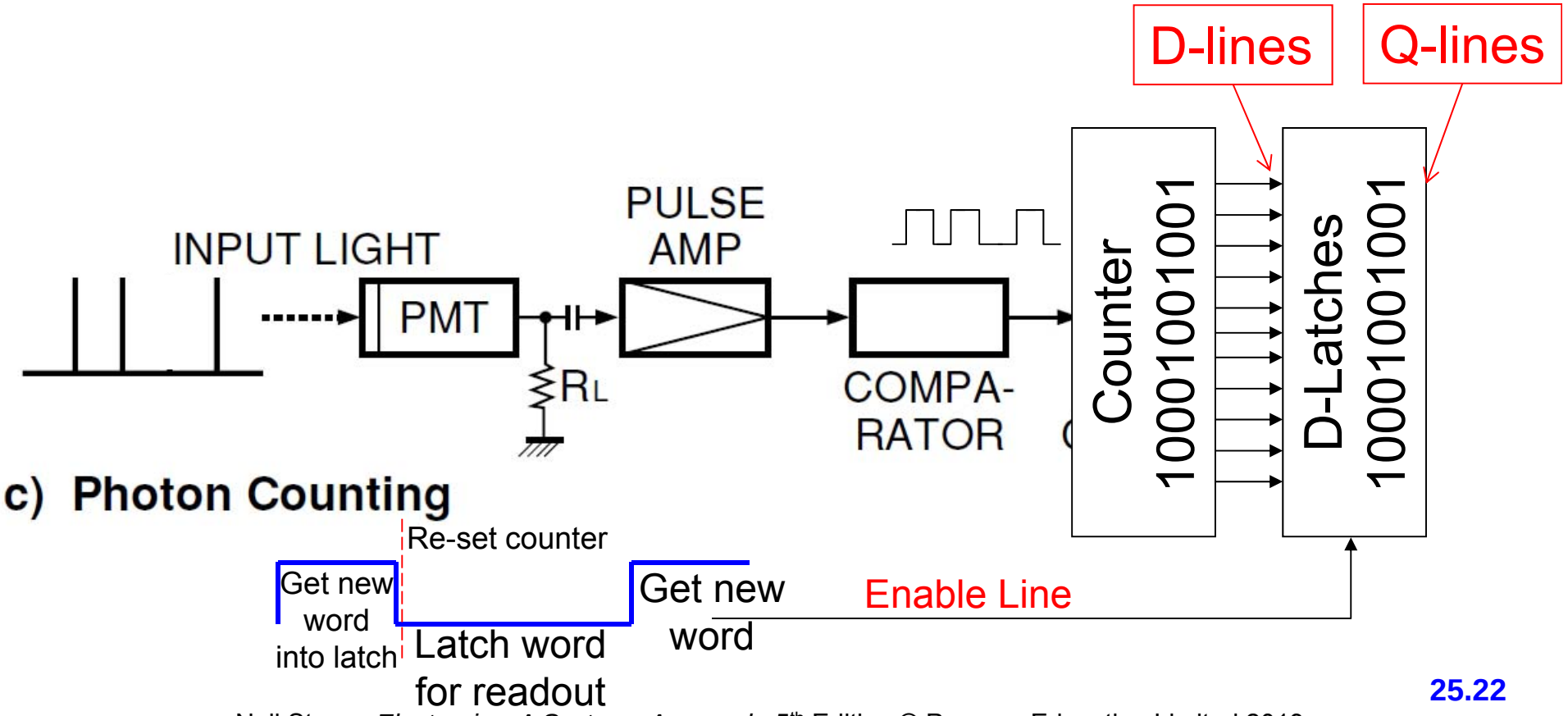
Use to Latch (or hold) value of D
Use in a parallel group to Latch value of a word



Enable High
Output
Tracks Value of D

Enable Low
Output
Holds Value of D

- Fundamental Storage Register



So far, you now already know how to build:

- Photo-tube—voltage divider
  - Potential difference accelerates electrons

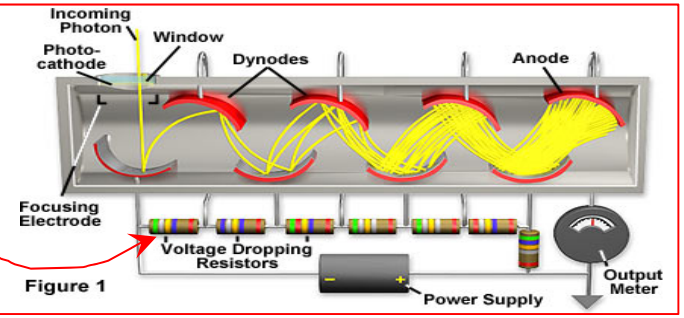
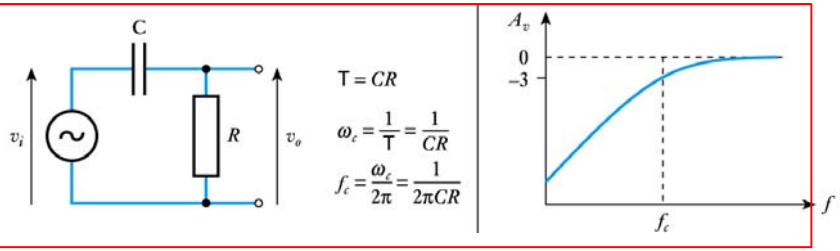


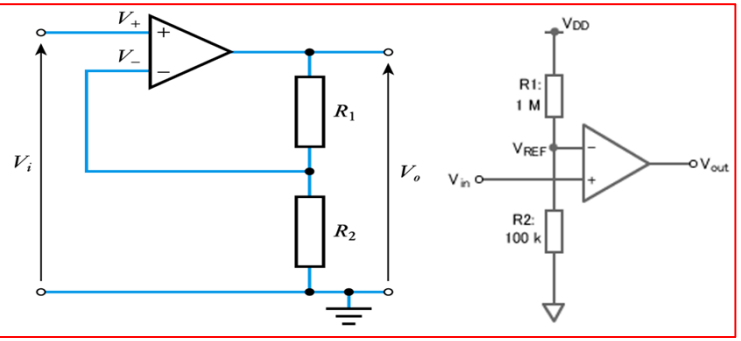
Figure 1

- R-C high-pass filter
  - Only the pulse passes



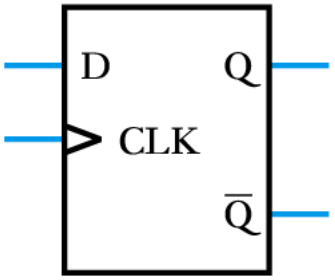
- Pulse amplifier $G = \frac{V_o}{V_i} = \frac{R_1 + R_2}{R_2}$

  and comparator (V_{out}=V_{DD} when $V_{in} > V_{ref}$)

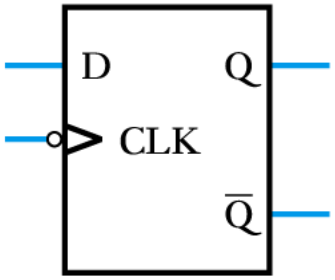


Edge-triggered devices

- It is often necessary to synchronise many devices
- This can be done using a **clock input**
  - such devices respond on a particular transition of the clock.
  - these are called **edge-triggered devices** or **flip-flops**
  - can have **positive-edge** or **negative-edge** triggered devices

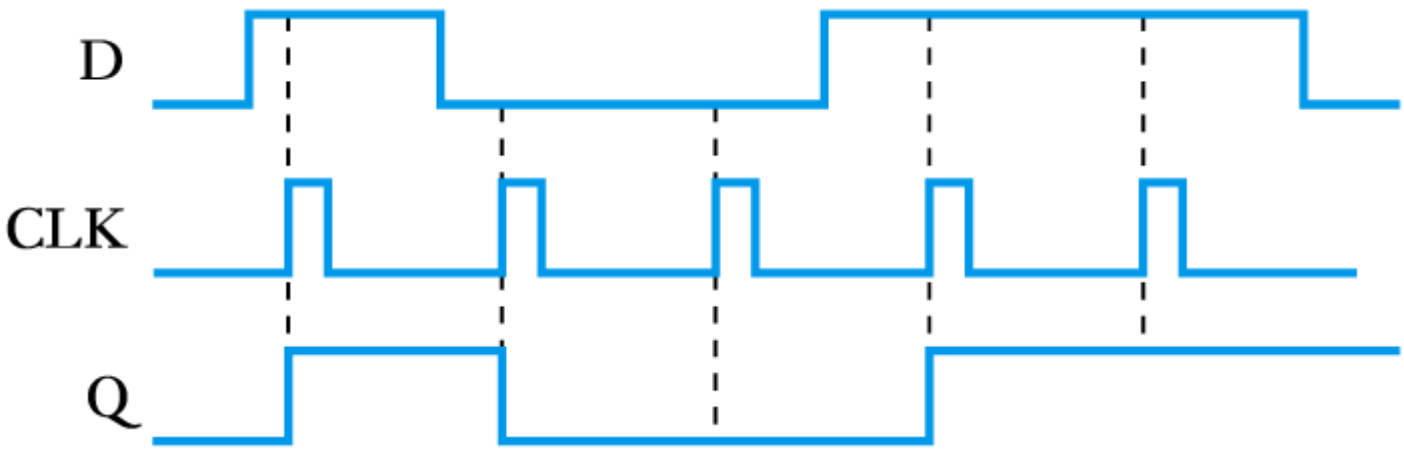


(a) Positive edge-triggered

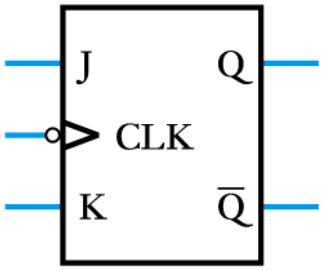


(b) Negative edge-triggered

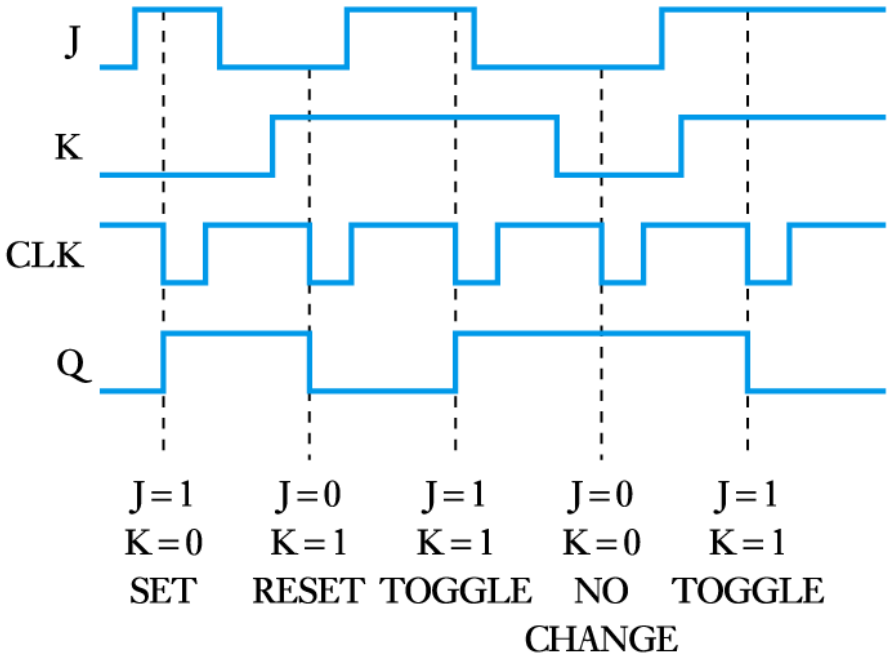
- **The *D* flip-flop**
  - Symbol as in previous slide
  - Behaviour of positive-edge triggered device as below
  - *Q* becomes equal to *D* *at the time* of the trigger event



- **The J-K flip-flop**
  - Similar to S-R flip-flop but *toggles* when J = K = 1

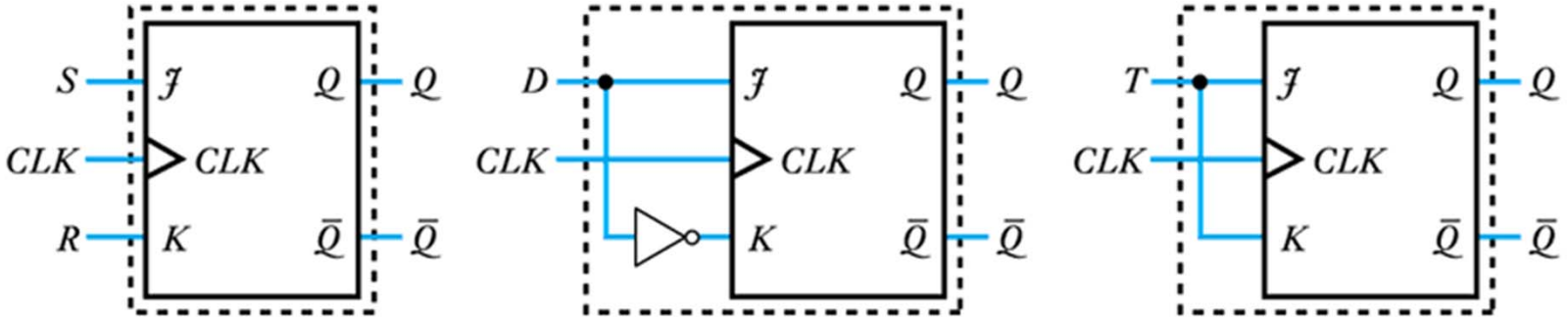


(a) Logic symbol



(b) Sample input and output waveforms

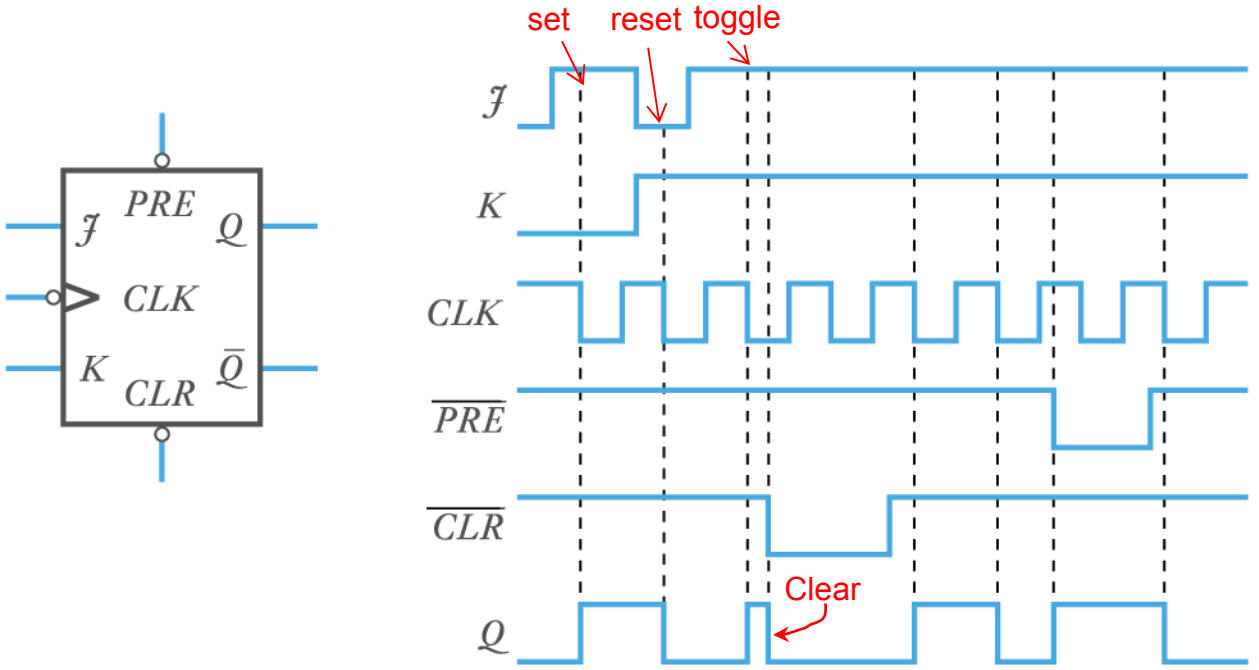
- **Use of a J-K flip-flop to reproduce other flip-flop functions (hence it is widely used due to its versatility)**



When toggle T=1
Each clock pulse changes Q

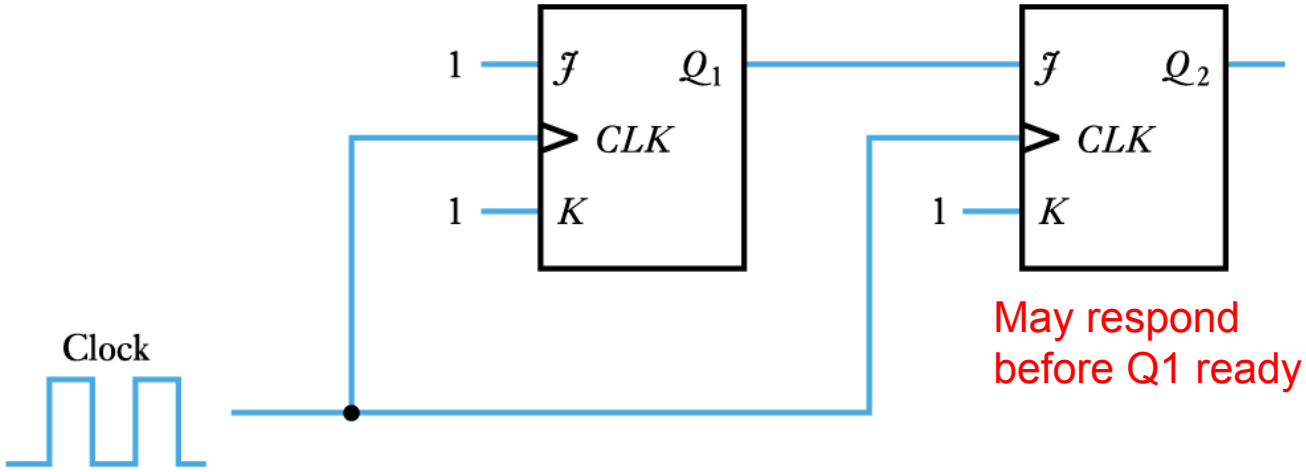
Before, J&K set/reset output Q only at the moment of an appropriate transition of the clock signal (*CLK*).

- **Asynchronous inputs**
  - Some flip-flops have asynchronous inputs (that clear/ reset independently of the clock)

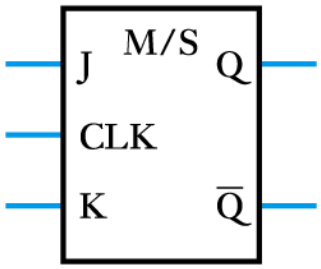


(a) Logic symbol (b) Sample input and output waveforms

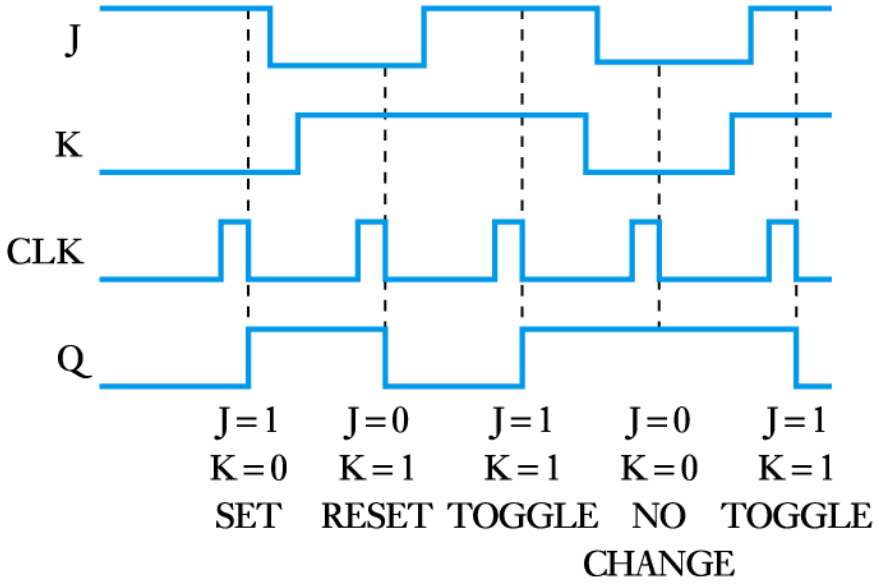
- **Propagation delays and races**
  - Real logic gates take a finite time to react
  - Some circuits (as below) can suffer from **race hazards** where the operation of the circuit is uncertain
    - In this circuit the output depends on which devices is fastest



- **Pulse-triggered or master/slave bistables**
  - These overcome race hazards by responding to the state of the inputs shortly *before* the clock trigger



(a) Logic symbol



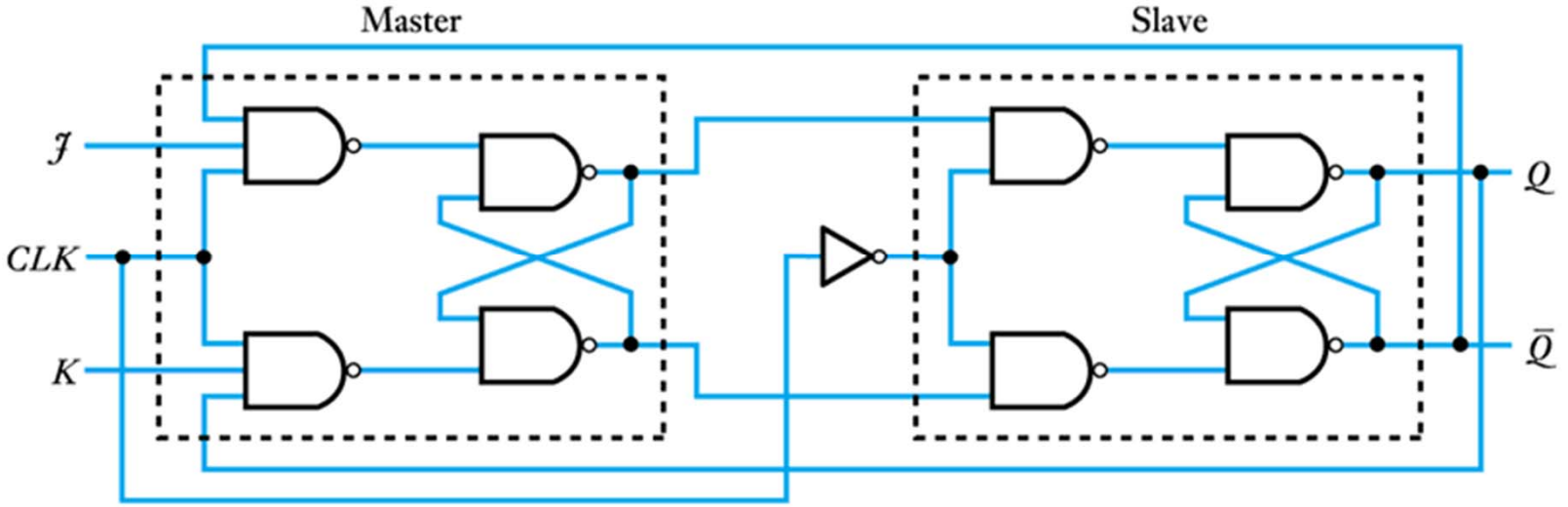
(b) Sample input and output waveforms

CLK=1 determines what outputs should be, but outputs change only on CLK↓0

Disable S (it holds its output steady)
Enable M moment later
(it updates it outputs to match inputs)

Disable M (it holds it outputs steady)
Enable S moment later
(it updates outputs to match M)

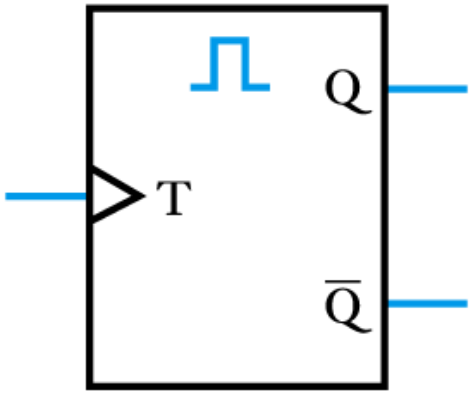
- **Circuit of a basic J-K master/slave flip-flop**



Master-latch and inverter delays timed so slave is disabled shortly before the master is enabled, preventing race condition

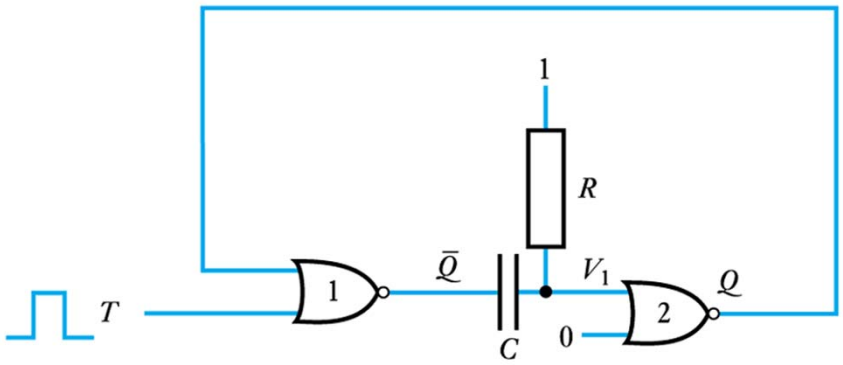
Monostables or one-shots

- Monostables are another form of multivibrator
  - while **bistables** have two stable output states
  - **monostables** have one stable & one metastable states
    - when in its stable state $Q = 0$
    - when an appropriate signal is applied to the trigger input (T) the circuit enters its metastable state with $Q = 1$
    - after a set period of time (determined by circuit components) it reverts to its stable state
    - it is therefore a **pulse generator**

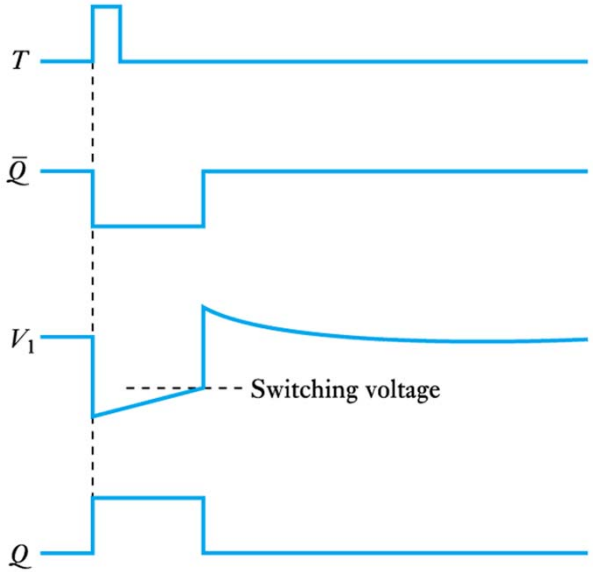


Circuit symbol

A simple monostable

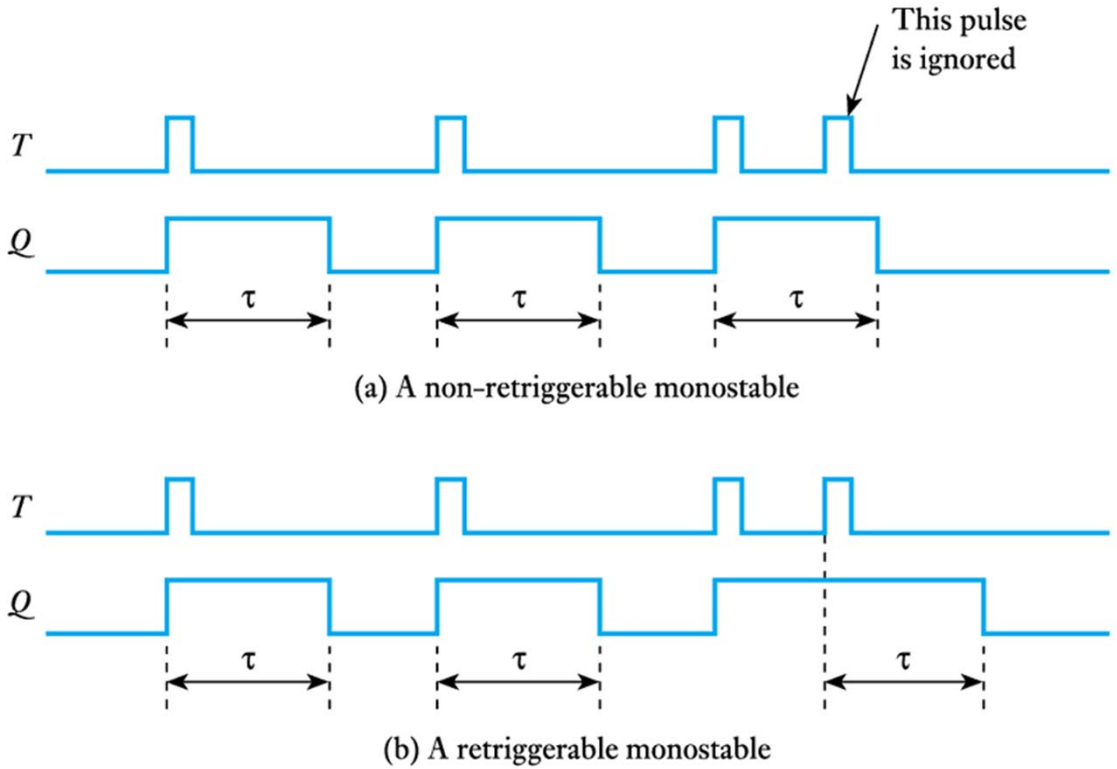


(a) Logic circuit



(b) Waveform diagram

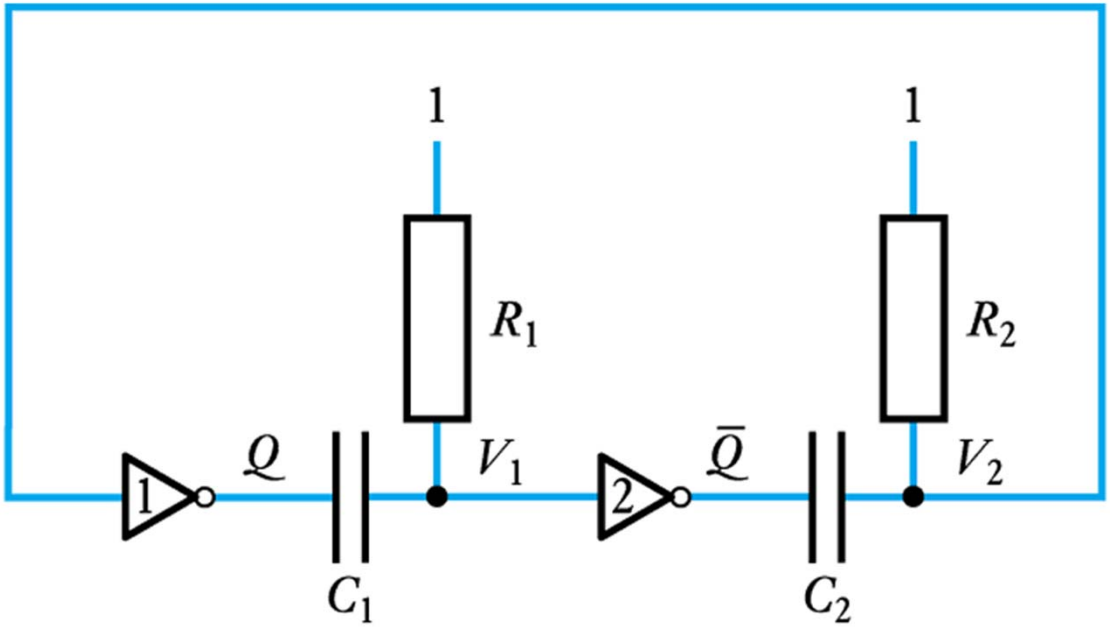
- Monostables can be **retriggerable** or **non-retriggerable**



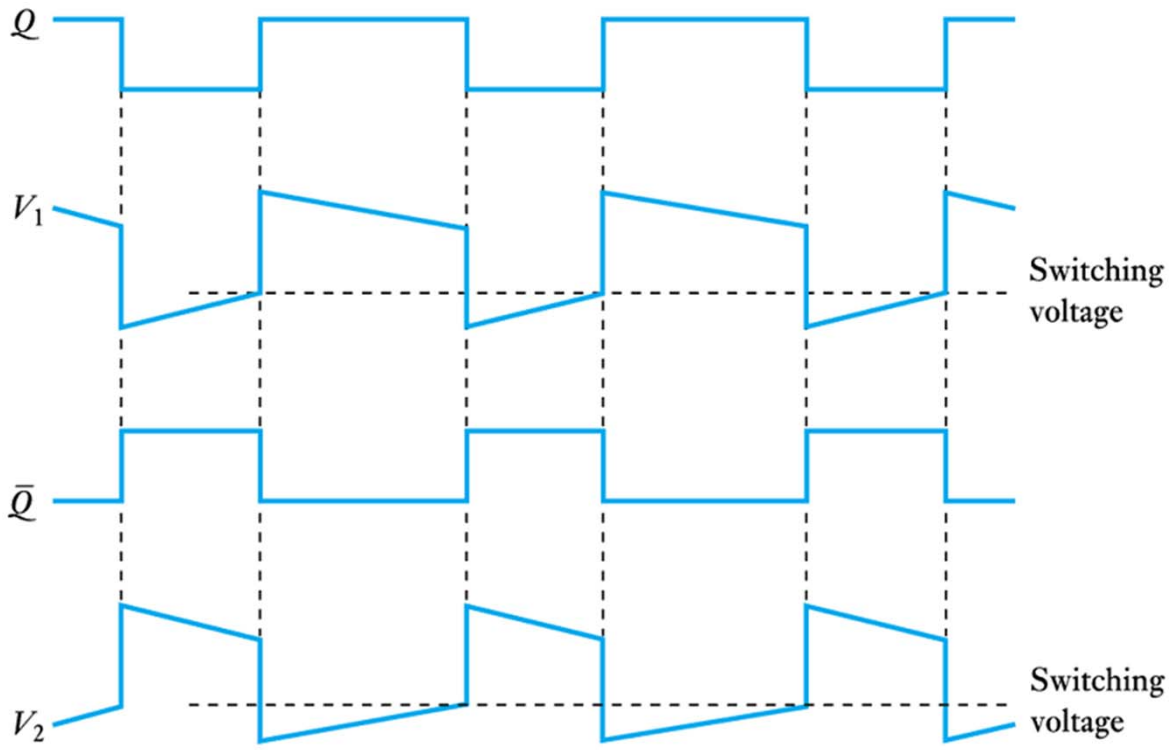
Astables

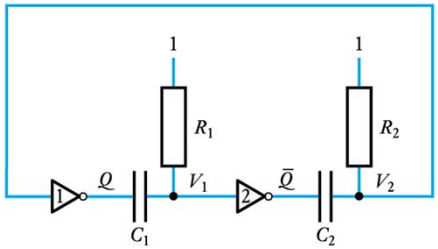
- The last member of the multivibrator family is the **astable**
  - this has two metastable states
  - has the function of a **digital oscillator**
  - circuit spends a fixed period in each state (determined by circuit components)
  - if the period in each state is set to be equal, this will produce a square waveform

- **A simple astable arrangement**



- **Waveforms of the simple astable circuit**



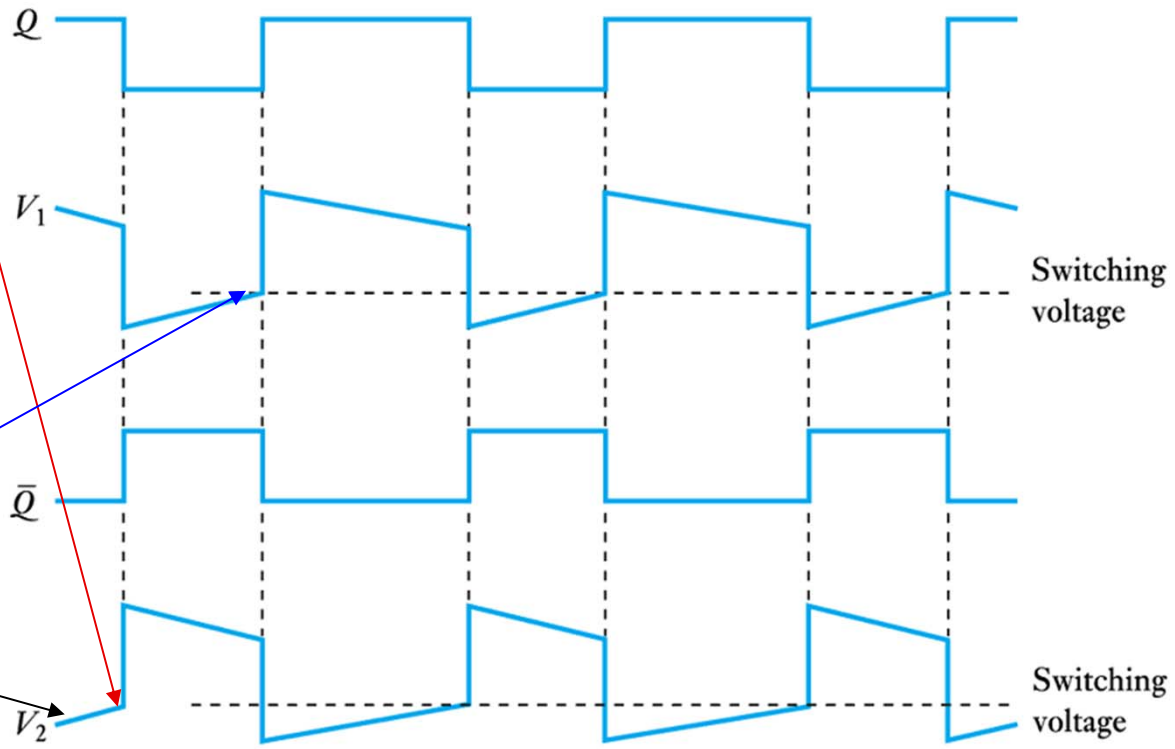


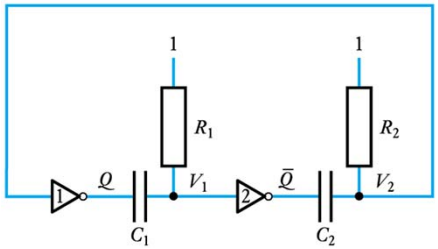
- **Waveforms of the simple astable circuit.**

(2) V_2 hits trigger point, switches Q low → V_1 Low but charging sets !Q high

(3) V_1 hits trigger point switches !Q low → V_2 Low but charging sets Q high

(1) !Q low→V_2 Low but charging keeps Q high





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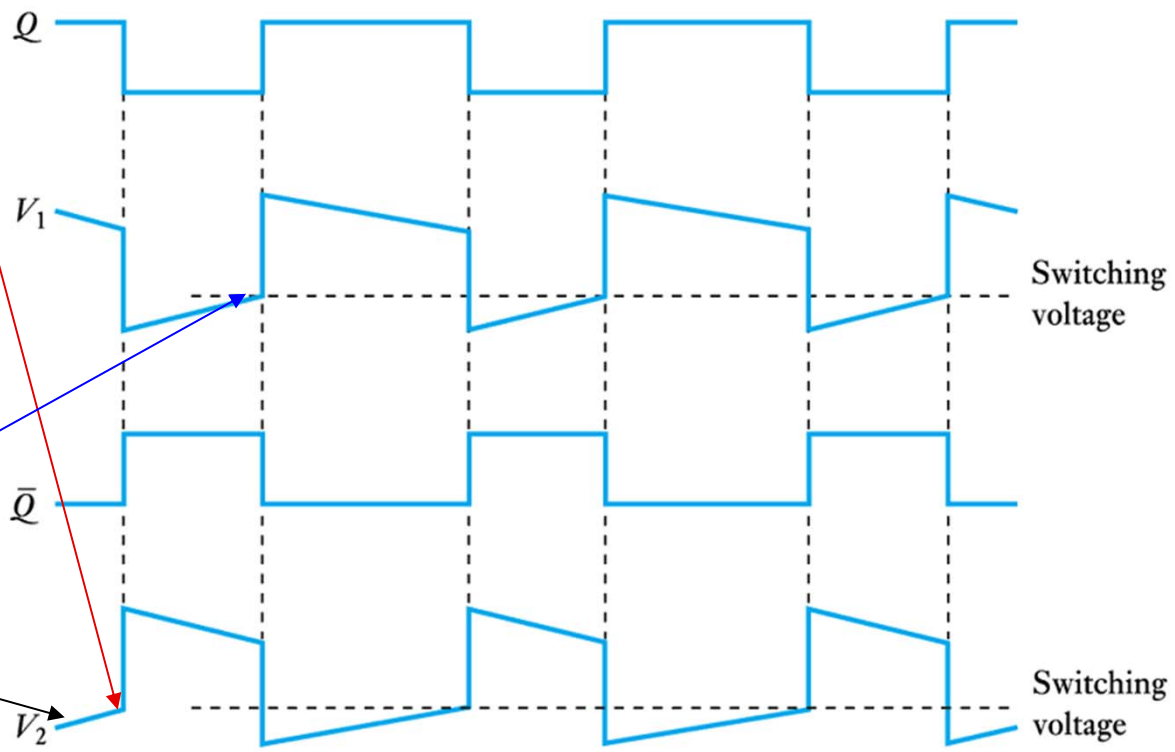
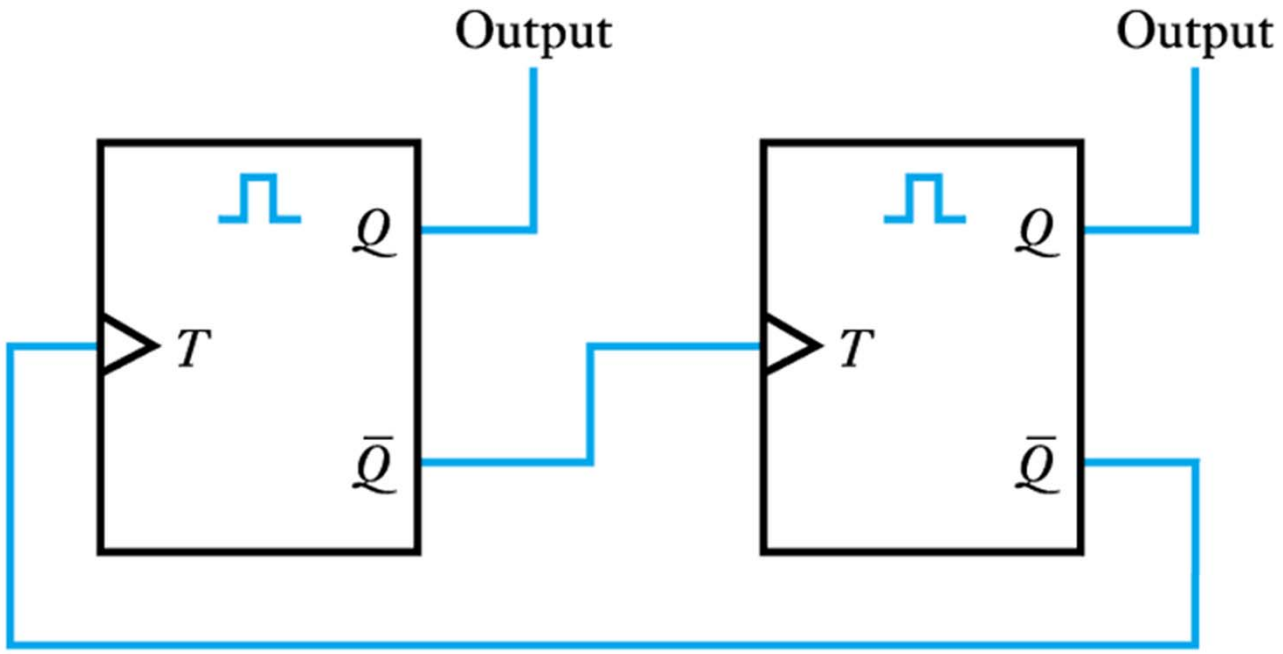


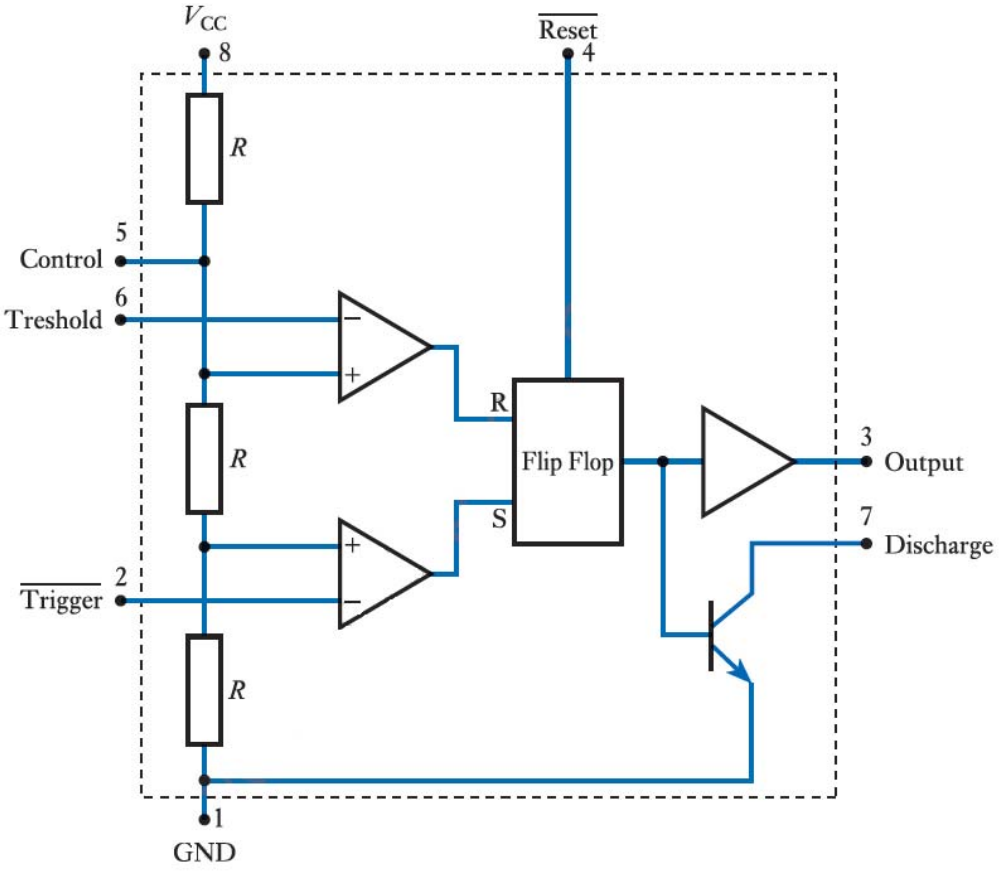
- **An astable formed by two monostables**



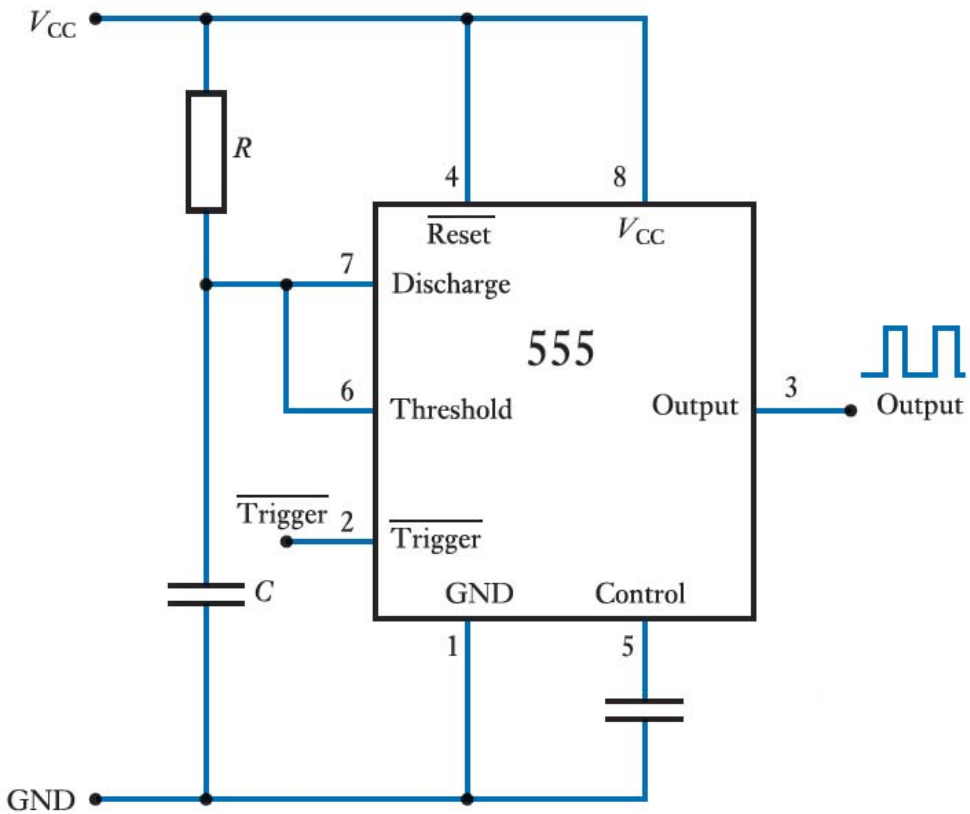
Timers

- The **integrated circuit timer** can produce a range of functions
  - including those of a monostable or astable
  - various devices
  - one of the most popular is the **555 timer**
  - can be configured using just a couple of external passive components
  - internal construction largely unimportant – all required information on using the device is in its data sheet

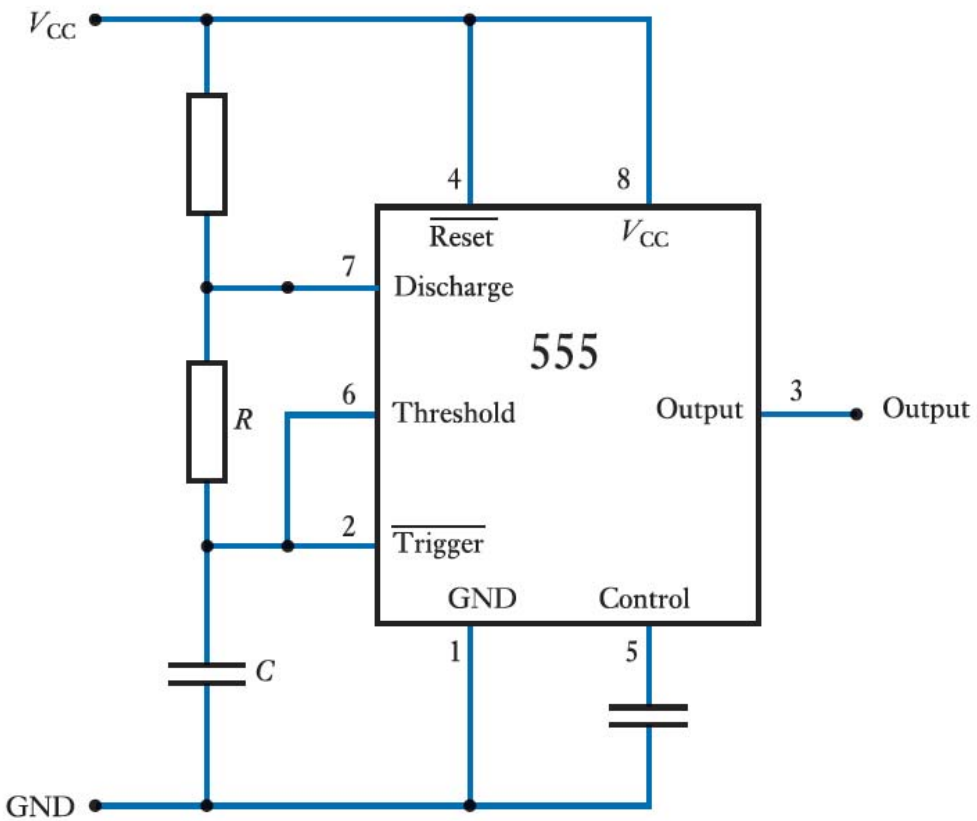
- A simplified circuit diagram of the **555 timer** is shown here
  - It consists basically of a flip-flop, two comparators, a switching transistor and a resistive network.



- The diagram here shows the 555 configured as a monostable.
  - It can be seen that only a couple of external components are needed.



- Here the 555 is shown configured as an astable
  - Again very few additional components are required.



Key points

- Sequential logic circuits have the characteristic of memory
- Among the most important groups of sequential components are the various forms of multivibrator
  - Bistables-flip flops and latches
  - Monostables-one shots
  - Astables-digital oscillators and timers