1) **Physical logic gates take a finite time to respond to changes in their input signals. What name is given to this time?**

a) Hold time.
b) Rise time.
c) Set-up time.
d) Propagation delay time.

Since a gate takes a finite time to respond to an input signal, its output will be delayed relative to that input. Should that input signal and the output of this gate be used as inputs for another logic gate, the signal from the first gate will have a propagation delay time relative to the original signal. Should the delay be substantial, it could result in the new gate being driven by the current, un-delayed signal and the old state of the system from the previous gate that has not yet been able to update its outputs due to its finite response time.

2) **Express the binary number 1001 in decimal.**

a) 9
b) 11
c) 13
d) 15

Since the number 1001 represents $1 \cdot 2^3 + 0 \cdot 2^2 + 0 \cdot 2^1 + 1 \cdot 2^0 = 8 + 0 + 0 + 1 = 9_{10}$

3) **Express the decimal number 57 in binary.**

a) 111010
b) 111001
c) 110011
d) 111101

Converting from decimal to binary, one can use the method:

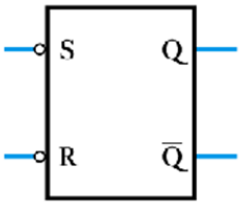
57 ÷ 2 = 28 + remainder 1
28 ÷ 2 = 14 + remainder 0
14 ÷ 2 = 7 + remainder 0
7 ÷ 2 = 3 + remainder 1
3 ÷ 2 = 1 + remainder 1
1 ÷ 2 = 0 + remainder 1 *taking the remainders from bottom to top gives* 111001_2

4) **Which of the following is not a form of multivibrator?**

a) Astable
b) Bistable
c) Tristable
d) Monostable

Combinational and sequential logic use only 2 logic levels, 0 and 1. Thus a multivibrator can only switch between these states. Sometimes the term tristable is used for a logic device that can turn its outputs off (0) but set them to a high impedance so as not to appear to other devices on a bus. However, this is not a different logic state, but a feature of the "0".

5) The S-R latch shown here has active high inputs.



a) True
b) False

The circles on the inputs show that this device has active low inputs.

6) A J-K flip-flop has two control inputs. What happens to the Q output on the active edge of the clock if both control inputs are asserted at this time.

a) The *Q* output remains unchanged.
b) The *Q* output is set to 1.
c) The *Q* output toggles to the other state.
d) The *Q* output is reset to 0.

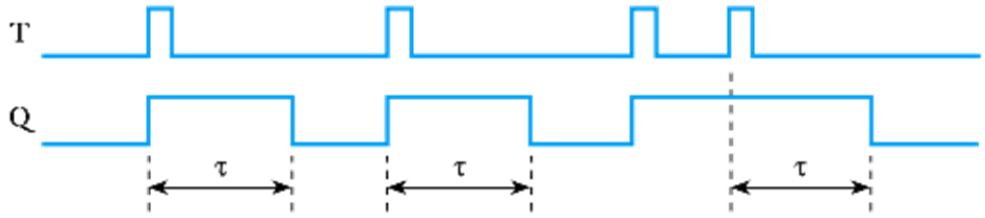
"Asserted" means that both inputs are held high, or in the "1" logic state. In this condition, the clock will toggle the output (if it had been1, it will be switched to 0; if it had been 0, it will be switched to 1)

7) A master/slave bistable is formed using two bistable connected in series.

a) True
b) False

This is true. The outputs are determined by the first (master) flip-flop while the clock is high, but the outputs of the second (second) flip-flop only change when the clock makes the transition from high to low. The slave is disabled before the new signals arrive at the master, so the output of the slave is steady until the clock makes the transition from high to low. In this way, the "race" condition, where a downstream device may be enabled while the output of the previous gate is in transition.

8) What type of monostable produces waveform of the form shown here?



a) A retriggerable monostable

b) A non-retriggerable monostable

Here we can see that the device is normally at 0, but when it is triggered, it changes its state from 0 to 1 for a set time period, τ, before returning to its default state, 0. This is a monostable device. On the last clock pulse we can observe that the device can be re-triggered. That is, if it is triggered before it has reset to 0, it will remain high from the second trigger for time period, τ. If the device had ignored the second trigger and returned to 0 a time τ after the first trigger, it would be a non-retriggerable monostable.

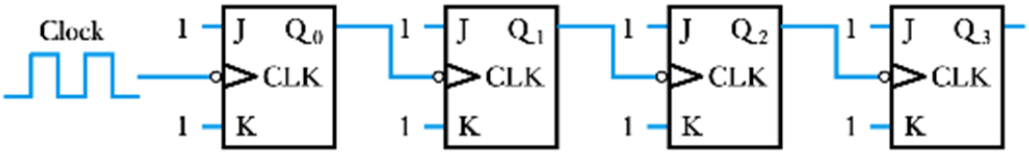
9) An astable has two metastable states and produces the function of a digital oscillator.

a) True

b) False

An astable device combines two devices so that the first one sends the second one into a metastable state, but that metastable state switches the first one into its metastable state…and so on and so on. Thus, the output of a device will oscillate between 0 and 1.

10) What is the function of the following circuit?



a) A four-bit shift register.

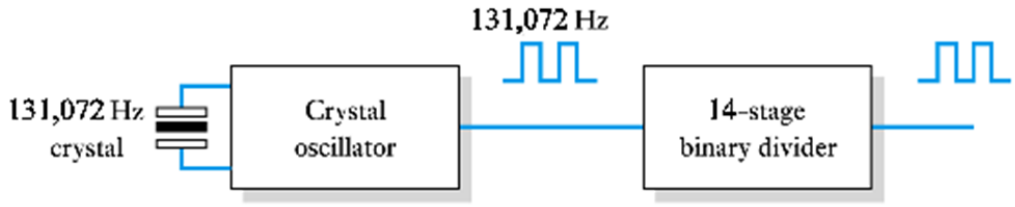
b) A four-bit memory register

c) A four-bit ripple counter.

This is a series of flip-flops in toggle mode. Whenever the toggle goes from 1 to 0 (1→0), the output will change to the opposite state it had. So, initially at 0, when the first clock pulse goes from high to low (1→0), the output of Q_0 will switch from 0 to 1. On the second clock pulse falling edge (1→0), the output Q_0 will also toggle from 1→0, but this will ripple on, triggering the second flip-flop Q_1 output to go from 0 to 1. On the third clock pulse falling edge (1→0), Q_0 will go from 0 to 1, but Q_1 will remain at 1 since its clock (which is Q_0) has not made a transition from 1→0 (it made the transition 0→1 which will not act as trigger).

Looking at Q_0 and Q_1, on clock pulse 0 they read Q_1=0, Q_0=0; on clock pulse 1 they read Q_1=0, Q_0=1, and on clock pulse 2 they read Q_1=1, Q_0=0. On clock pulse 3, they would read Q_1=1, Q_0=1. That is, the pair gives the binary word that represents the number of clock pulses. We can assume Q2 and Q3 will follow this, so it is a 4-bit ripple counter.

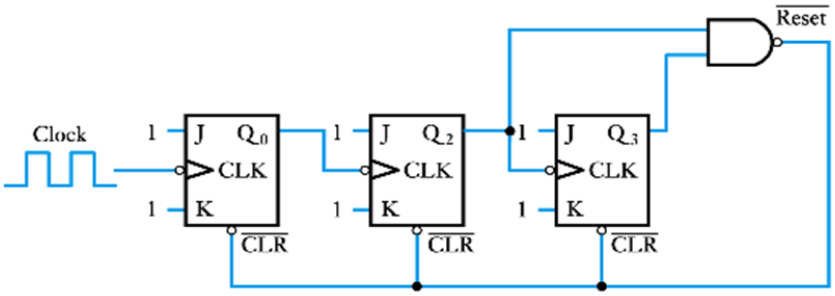
11) What is the frequency of the output of the following circuit?



a) 1 Hz
b) 4 Hz
c) 8 Hz
d) 16 Hz

A 14 stage binary divider will divide by 2^{14}=16384. This means the output will be 131072 Hz/16384=8 Hz

12) What is the function of the following circuit?



a) A modulo-6 counter.
b) A modulo-8 counter.
c) A modulo-10 counter.
d) A modulo-12 counter.

A three-stage counter without any reset circuitry will count from zero to seven and then repeat (giving a modulo-8 counter). The presence of the reset circuitry in this arrangement detects the count of 6 and then resets the circuit to zero. Thus the circuit counts from zero to five and then repeats, and is thus a modulo-six counter.

13) In synchronous counters the clock input of each of the bistables are connected together so that each changes state at the same time.

a) True
b) False

To avoid the delay in the ripple counter, where the clock transition 1→0 has a propagation delay to the output Q_0, which then ripples into the inputs that, after a propagation delay, determine Q_1, one could connect all the toggle inputs to the same clock. We would then need additional circuitry to detect which inputs should change and which should remain the same, and adjust the J inputs of the different flip-flops accordingly. Thus, only the first, LSB flip-flop is operated in toggle mode, the others are in J-K flip-flop mode.

14) **What is the cause of storage time in a bipolar transistor?**

a) The 'memory effect' of the device.
b) The inertia of the majority charge carriers.
c) The time taken to remove excess charge stored in the base region as a result of saturation.
d) The inertia of the minority charge carriers.

When used as a logical switch, the base of the transistor going high would create a large V_{BE} that would effectively allow a very large collector current, I_C to flow. The transistor is fully on, and the output voltage $V_o=V_{CE}$ is approximately 0.1 V, the saturation voltage of the amplifier. However, when the transistor is fully on, or saturated (which produces the lowest output voltage, a condition we want to produce a clear logical 0), a surplus of minority charge carriers is injected into the base region (more that can be swept to the collector). This results in a build-up of charge in the base, and this requires a longer time to clear. Thus, the time for the transistor to switch on ($V_o=1\downarrow 0$) is relatively short, but once it switches off, it takes some time to clear the excess charge before the transistor shuts off, allowing $Vo=0\uparrow 1$.

15) What is meant by the fan-out of a logic gate?

a) The number of other gates that can be connected to the gate's output.
b) The physical distance between the output pins on the device.
c) The number of other gates that can be connected to one of the gate's inputs.
d) The amount of cooling required by the gate.

This is just the terminology used to describe the output of a device "fanning-out", or spreading out, to the inputs of several other gates. The number of gates an output can drive is called the device's "fan-out".

16) Which of the following statements is incorrect?

a) TTL devices have logic levels of about 3.4 V and 0.2 V.
b) TTL logic has very low power consumption and is therefore widely used in highly integrated components.
c) TTL logic normally operates from a single 5 V supply.
d) Standard TTL devices have a propagation delay that is dominated by the storage time of the bipolar transistors used.

Remembering our table comparing TTL to CMOS logic, we see that TTL gates take between 1 and 22 mW each. However, CMOS gates, switching between 0 and 1 at a MHz rate, take only 1 mW each. Thus, some gates in low power TTL can be as low as CMOS (but at speeds < 1MHz), but that is for only a single gate type in a single sub-species of TTL (that does not lend itself well to large-scale integration), and most TTL is much higher power consumption.

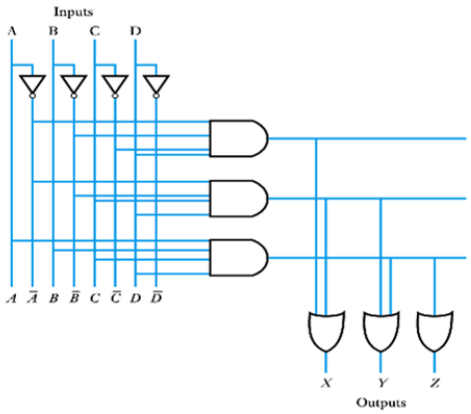
17) What should be done with an unused TTL input that is required to be at logical 1?

a) It should be connected directly to the positive supply rail.
b) It should be connected directly to the zero volt supply rail.
c) It should be left disconnected.
d) It should be tied to the positive supply rail through an appropriate resistor.

Here it is important to realise that TTL uses bi-polar transistors that operate by injecting or drawing out current from the base of the transistor. Thus the inputs and outputs have current flowing. For many TTL devices the inputs source current and therefore will float high by themselves. On the other hand, these inputs represent a high impedance path to ground and should therefore be tied high to stop them picking up noise. Although connecting these through a so-called "pull-up" resistor to the positive supply rail is not strictly necessary, it is a good idea to do so as it prevents noise on the power supply line from accidentally causing an "over-voltage" condition on the input ($V_{input} > V_{supply}$ of the device). In addition, some TTL devices are "open collector" and do not source current, and these need to be connected to the power supply through a resistor to prevent drawing too much current through the device.

CMOS on the other hand, uses FET transistors that have currents that are over a 1000 times smaller, and can be considered voltage driven devices. Since there are basically no currents flowing, these devices can be tied directly to the power supply or ground without resistors.

18) In the following PLA, which output implements the logic function ABCD?



a) X b) Y **c) Z**

X and Y are both OR'ing together two signals, so it can't be them (otherwise it would have a + sign with two mini-terms). Only Z has a single input to the OR gate, and tracing this back we see that it comes from the AND gate that has inputs A, B, C and D.

19) The cells in a FPGA may contain registers, look-up tables and memory.

a) True b) False

A FPGA device has the basic logic gates already combined into more complex functions, allowing a higher level design.

20) Which of the following statements is incorrect?

a) Some PLDs are programmed using electrically operated switches.
b) Some PLDs are programmed using mechanical switches.
c) Some PLDs are programmed using anti-fuses that are selectively joined.
d) Some PLDs are programmed using fuses that are selectively blown.

Modern PLD's (anything on the market today) will have fused or electrically alterable links.

21) Communications within a microprocessor take place over a number of serial buses.

a) True **b) False**

By within the microprocessor, we mean the communication between the central processor and the memory and the I/O devices. Now even if the I/O is serial (keyboard or mouse), it is generally buffered in a parallel register and all communication is done on a parallel bus.

22) Which of the following statements is incorrect?

a) Static RAM stores information by energizing or de-energising inductors.
b) RAM is volatile.
c) RAM is memory that can be written and read quickly.
d) Dynamic RAM stores information by charging or discharging capacitors.

Static RAM is implemented using bi-stable devices that will maintain their state so long as power is maintained. Thus, while static, it is volatile (goes away when the power is turned off). There is a Non-Volatile RAM available, with which we are all familiar from cameras, telephones and memory sticks. However, this is a type of EEPROM. Once upon a time (up to about 1975) there was magnetic core memory, a type of RAM that relied on magnetizing ferrite cores one direction or the other using a current. Some had bead-style ferrite cores wrapped around a wire, while others had a coil wrapped around a ferrite ring. Perhaps one could, in the broadest sense call this latter programming by energizing or de-energizing inductors, but technically one stores the information by magnetizing the ferrite cores. So the best answer above would be A.

23) Which of the following statements is incorrect?

a) EPROMs can be erased using an ultraviolet light source.
b) ROM devices are non-volatile.
c) EEPROMs can be written to (programmed) as well as read from.
d) ROM devices must be programmed by the chip manufacturer.

ROM devices can be programmed the same way as PLD's or EEPROMS.

24) How many address lines would be found on a 128-kbyte memory device (assuming that this is arranged as an array of 8-bit registers)?

a) 13 b) 15 **c) 17** d) 19

You could view this question as how large of a binary word would I need to count up to 128,000. This is then the size of the bus needed to address 128,000 different addresses. Since the memory is arranged as an array of 8-bit registers (8 bits=1byte), then addressing 128,000 of these 8-bit registers would allow us to address 128,000 bytes of data.

Now with 10 address lines I could address 2^{10} = 1024 locations, and every addition power of 2 (which would add a new address line). With 16, I could address 2^{16}= 65536, and 17 would get be two times more, or 131,027. So I would need at least 17 address lines to count to 128k.

25) A signal contains components with frequencies up to 10 kHz, although no useful information is contained at frequencies above 6 kHz. What is the minimum frequency at which the signal should be sampled?

a) 6 kHz. b) 12 kHz. c) 14.4 kHz. **d) 20 kHz.**

In order to prevent aliasing of frequencies, I would have to sample at twice the largest frequency in my signal, not the largest frequency in which I am interested.

26) When using anti-aliasing filters it is normal to sample somewhat below the Nyquist rate to allow for the non-ideal characteristics of the filters.

a) True **b) False**

No, sampling at the Nyquist rate would require a perfect filter. In order to allow a larger distance between the highest frequency I desire and the Nyquist, I would sample at a higher rate than the Nyquist to allow for non-perfect filters and to avoid phase shifts. Thus, audio recordings are filtered (have a f_c) at 22 kHz, the upper limit of most human hearing, but are sampled at a rate of 44 kHz or more.

27) What is the resolution of a 12-bit data converter?

a) 0.00024% b) 0.0041% **c) 0.024%** d) 0.41%

*Think of a signal ramping from 0 to 1V that I want to digitize. A 12-bit converter will allow me to break that signal up into 2^{12}=4096 steps. That is the highest voltage will give a count of 4095 and the lowest will give a value of 0. Thus, the smallest step size is 1V/4096steps = 0.244 mV/step. As a percentage of full scale, that would be 0.00024 V/1V *100 = 0.024%.*

28) What is meant by the "droop" of a sample and hold gate?

a) The voltage by which the input quantity is lowered during sampling.
b) The rate of decay of the output voltage.
c) The voltage difference between the output voltage and the actual voltage being sampled.
d) The time taken to take a sample.

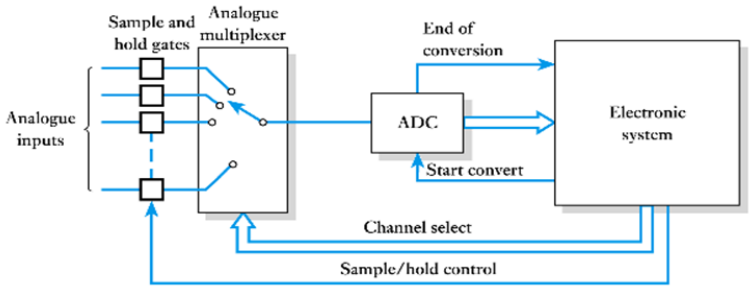
A sample and hold on either an ADC or a DAC will allow the voltage to charge a capacitor before isolating the capacitor with high impedances (an op amp or FET). However, the voltage will decay with a time constant τ=RC during the time this voltage is being sampled. The amount it decays is termed the "droop" of the sample and hold gate.

29) An analogue multiplexer is a form of electrically controlled switch, based on the use of analogue switches.

a) True b) False

This is true. The analogue switch may be constructed from FET or bipolar transistors used as an analogue switch, however, one can buy a "ready-made" device with multiple analogue switches, or an n-pole analogue multiplexer

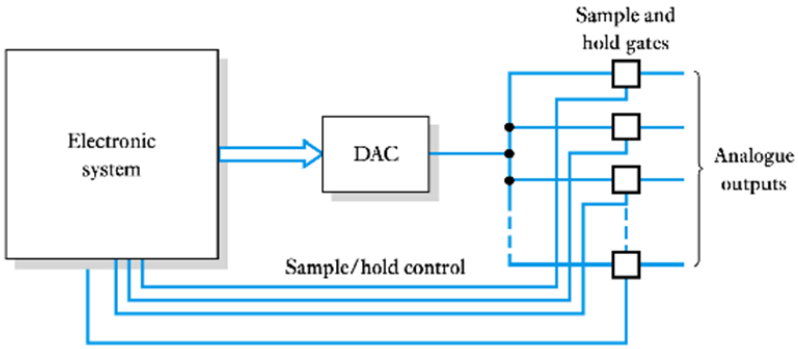
30) What is the primary function of the sample and hold gates in the following arrangement?



a) To allow all the inputs to be sampled simultaneously.
b) To buffer the input signals.
c) To prevent the ADC from distorting the input signals.
d) To block unwanted input signals.

The sample and hold gates may be triggered simultaneously, and then each one, in turn, digitized by the ADC. Since the ADC will take some time to convert, the sample and hold gates cannot be updated until the last gate has been converted. However, the sequential list of digital words from the ADC will represent the voltages present at the sample and hold gated at the time of the trigger.

31) What is the primary function of the sample and hold gates in the following arrangement?



a) To prevent variations in the load from affecting the output voltage.
b) To hold the outputs constant between updates of the outputs.
c) To allow the outputs to be updated simultaneously.
d) To buffer the output signals.

Since the DAC can only convert one signal at a time, and it takes a finite amount of time to do each conversion, sampling the output with a sample and hold gate will keep the output constant until it is updated again.