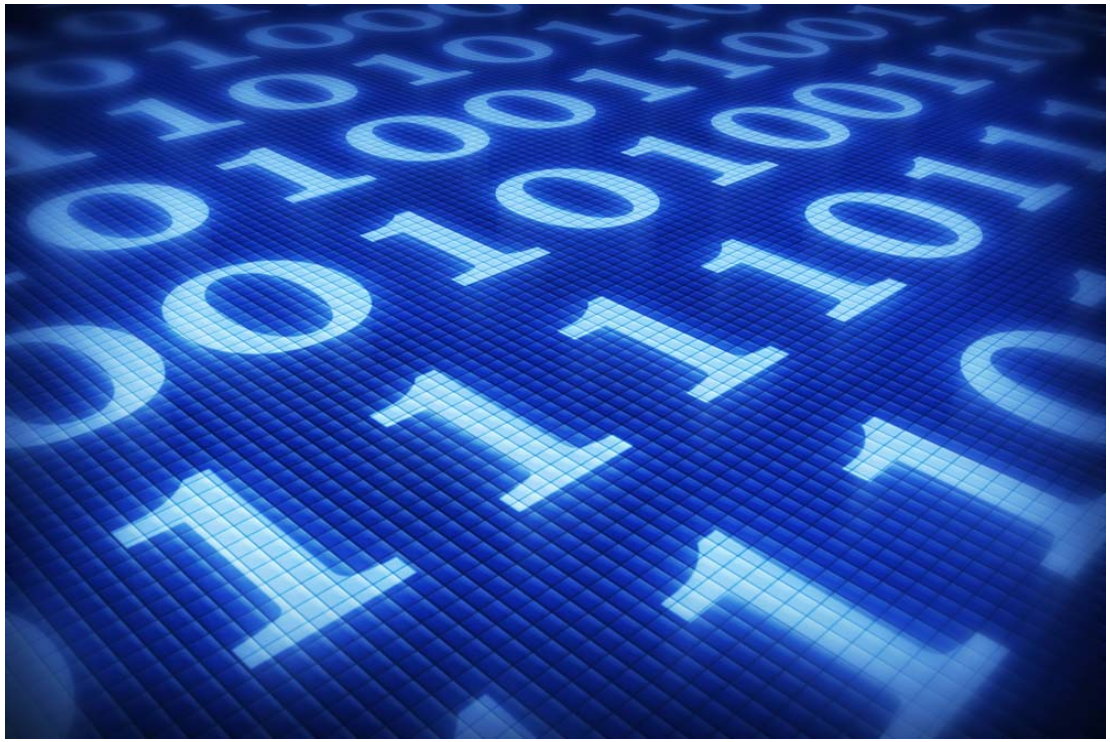
Chapter 25

Last time: Sequential logic

- Introduction
- Bistables
- Monostables or one-shots
- Astables
- Timers
- Memory registers
- Shift registers
- Counters



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Introduction

Video 25A

25.1

- Sequential logic is built with combinational logic elements
- Combines the characteristics of combinational logic with **memory**
- When constructing sequential logic circuits our building blocks are often some form of **multivibrator**
  - A term used to describe a range of circuits
    - these have two outputs that are the inverse of each other
    - the output are labelled Q and $\overline{Q}$
    - three basic forms:
      - **Bistables (flip-flops or latches)**
      - **Monstables (one-shots)**
      - **Astables (digital oscillators)**

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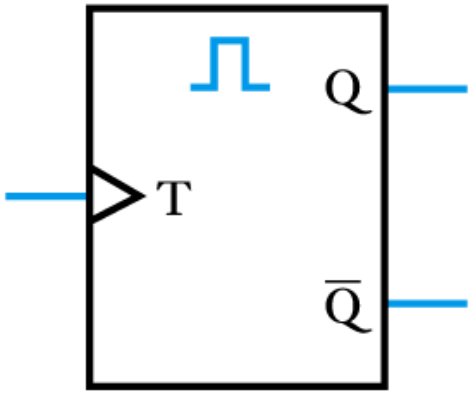
Monostables or one-shots

- Monostables are another form of multivibrator
  - while **bistables** have two stable output states that we can switch between
  - **monostables** have one stable & one metastable states
    - when in its stable state $Q = 0$
    - when an appropriate signal is applied to the trigger input (T) the circuit enters its metastable state with $Q = 1$
    - after a set period of time (determined by circuit components) it reverts to its stable state
    - it is therefore a **pulse generator**



Circuit symbol

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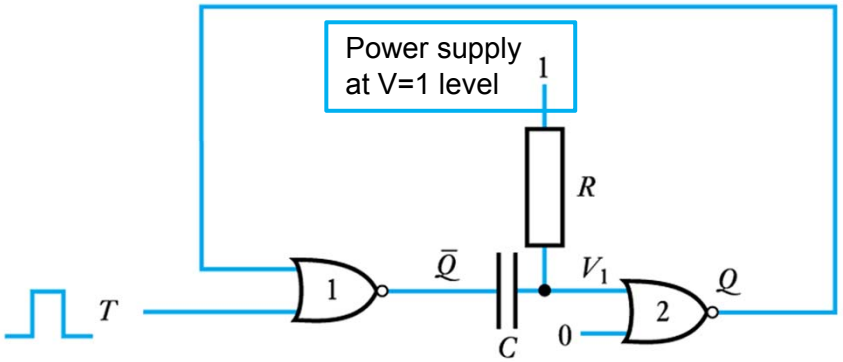
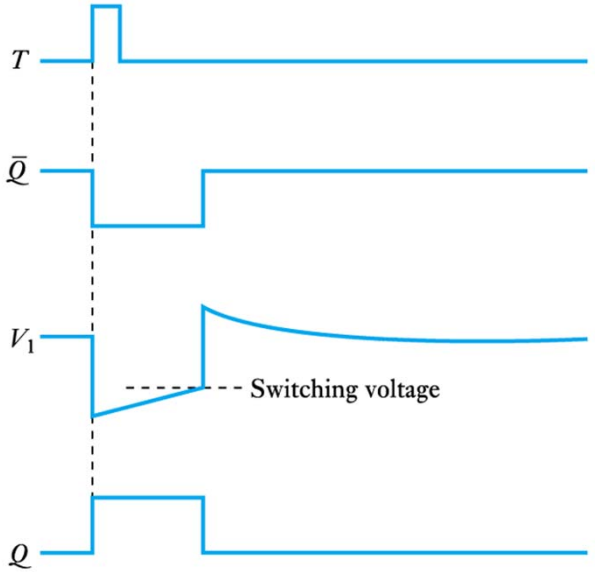
Initially in stable state:
T low and Q low ⇒ !Q high
No current flows across R
(both sides of C at same voltage, ΔV_c=0)
V_1 floats high keeping Q low

A simple monostable

Then trigger to metastable:
T goes high briefly ⇒ !Q goes low
Capacitor initially has no charge
and so no voltage across it
So V_1 drops to 0 ⇒ Q goes high, keeping !Q low
Current flows through R,
charging the capacitor
V_1 increases until Q goes low
System returns to stable state



(a) Logic circuit



(b) Waveform diagram

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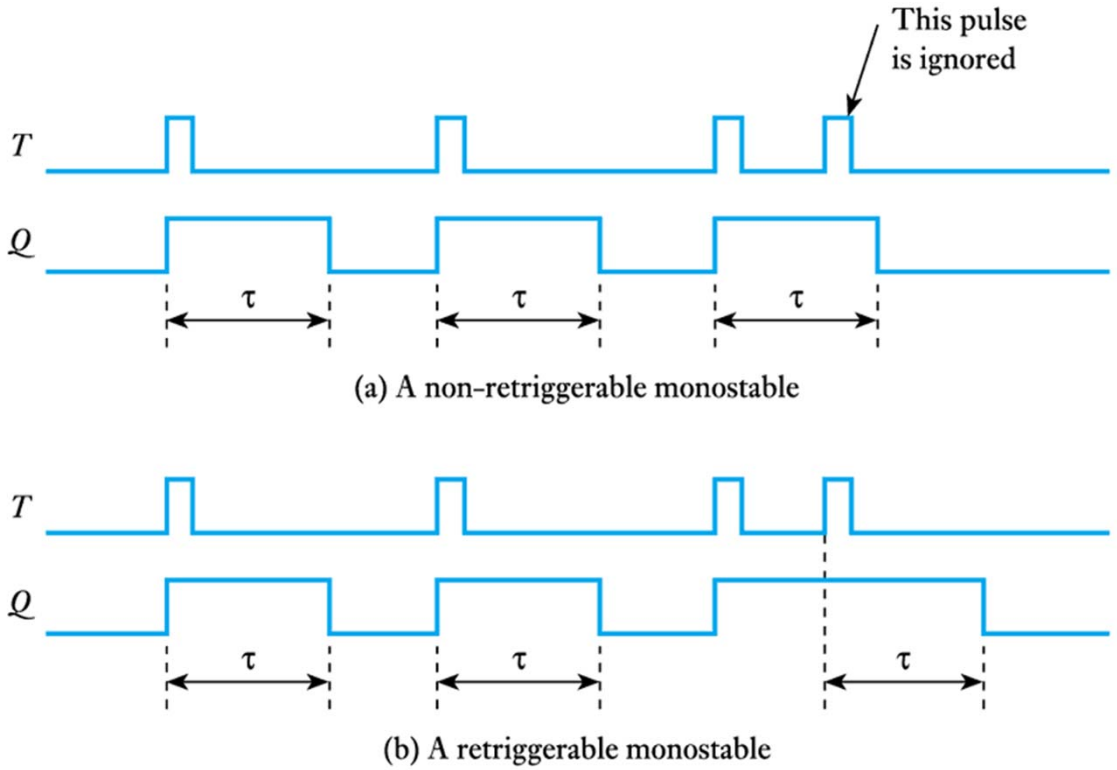
- Monostables can be **retriggerable** or **non-retriggerable**



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Astables

- The last member of the multivibrator family is the **astable**
  - this has two metastable states
  - has the function of a **digital oscillator**
  - circuit spends a fixed period in each state (determined by circuit components)
  - if the period in each state is set to be equal, this will produce a square waveform

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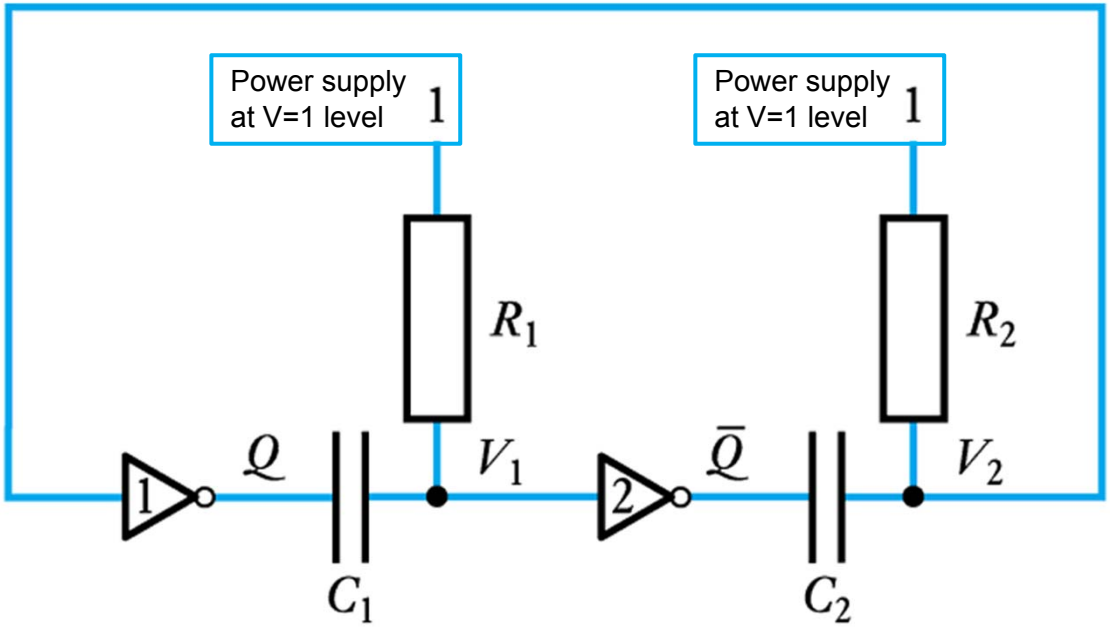
A simple astable arrangement



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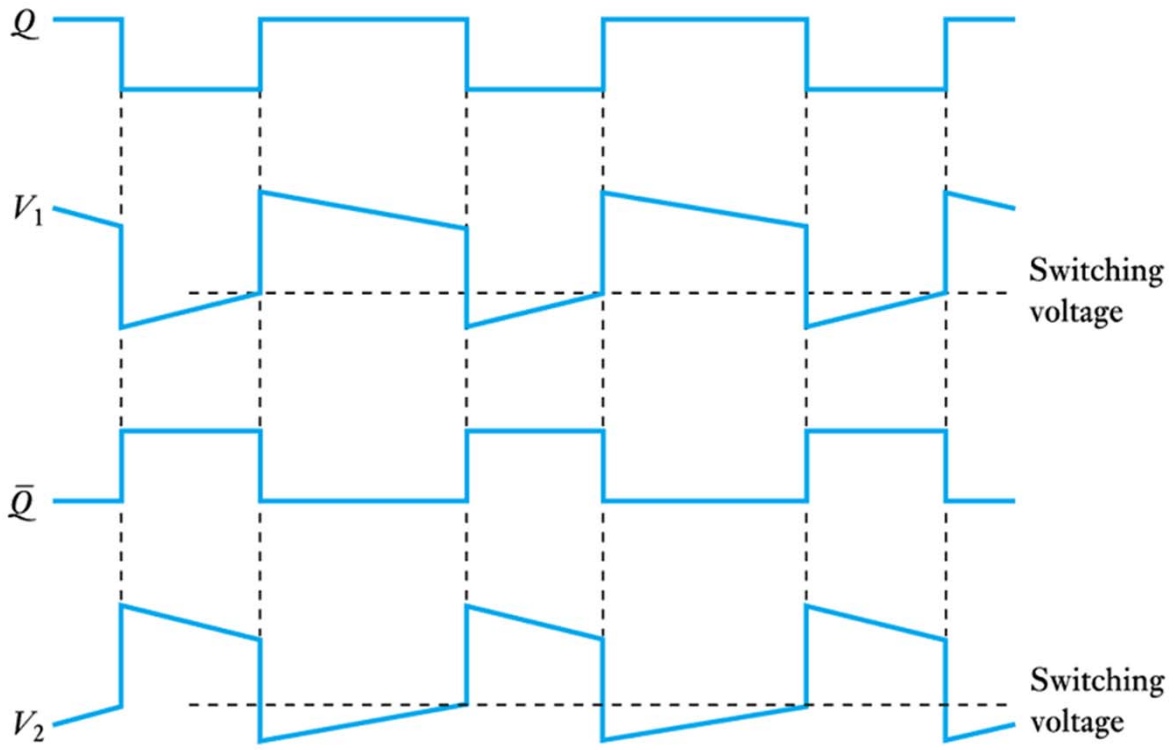
- **Waveforms of the simple astable circuit**



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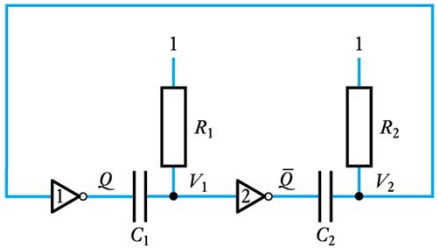
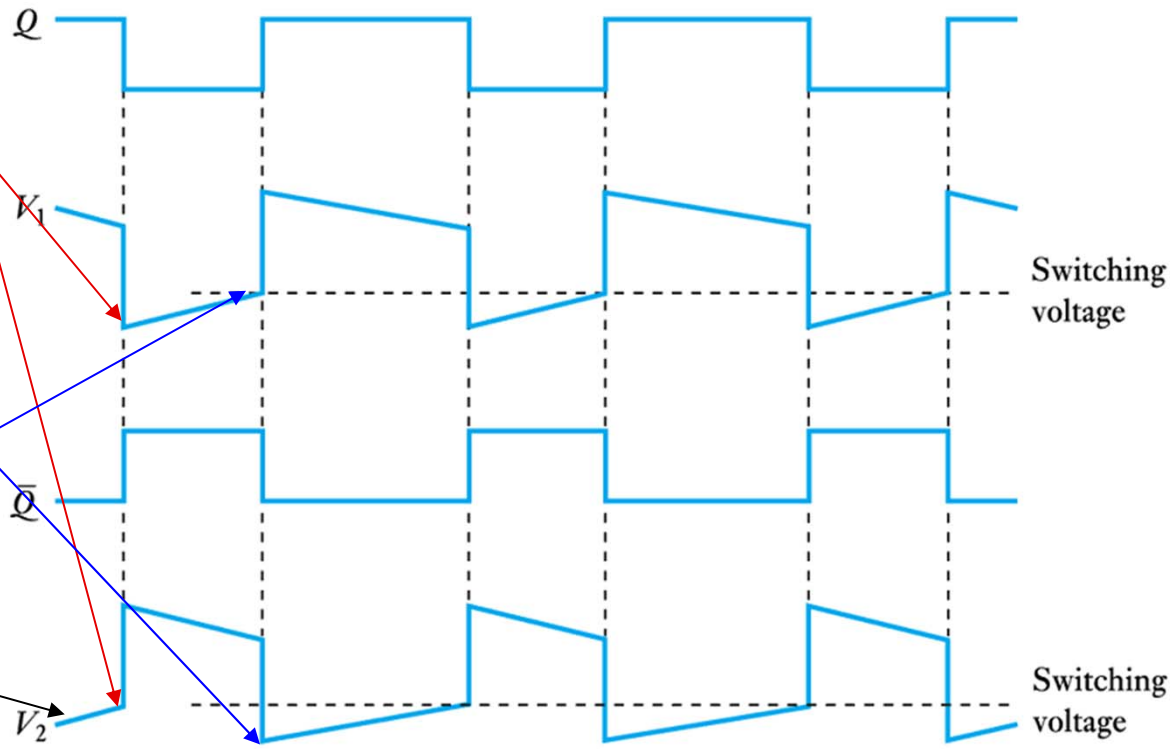


- **Waveforms of the simple astable circuit.**

(2) V_2 hits trigger point, switches Q low → V_1 Low but charging sets !Q high

(3) V_1 hits trigger point switches !Q low → V_2 Low but charging sets Q high

(1) !Q low→V_2 Low but charging keeps Q high



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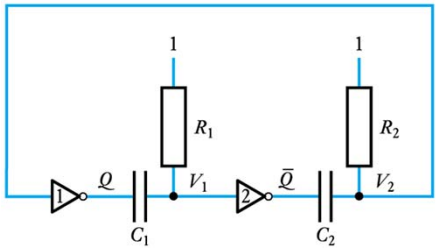
How do I get the signal out to the world?



- **Waveforms of the simple astable circuit.**

(2) V_2 hits trigger point, switches Q low → V_1 Low but charging sets !Q high

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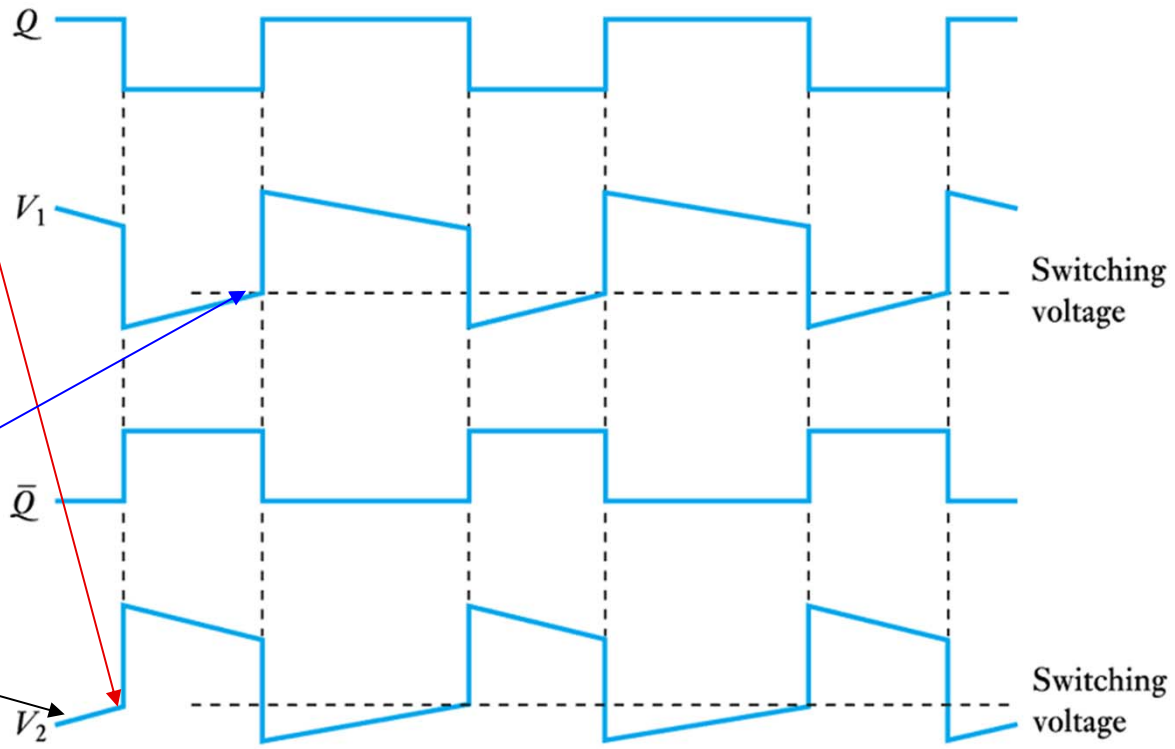

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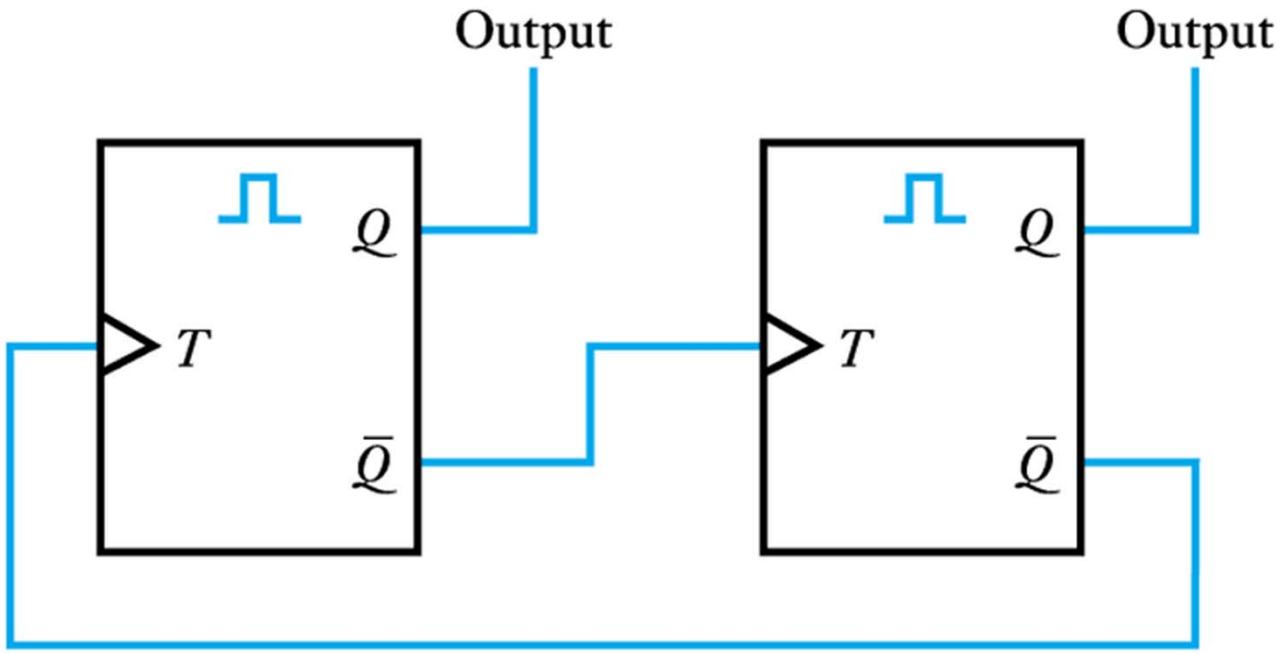
- **An astable formed by two monostables**



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Timers

- The **integrated circuit timer** can produce a range of functions
  - including those of a monostable or astable
  - various devices
  - one of the most popular is the **555 timer**
  - can be configured using just a couple of external passive components
  - internal construction largely unimportant – all required information on using the device is in its data sheet

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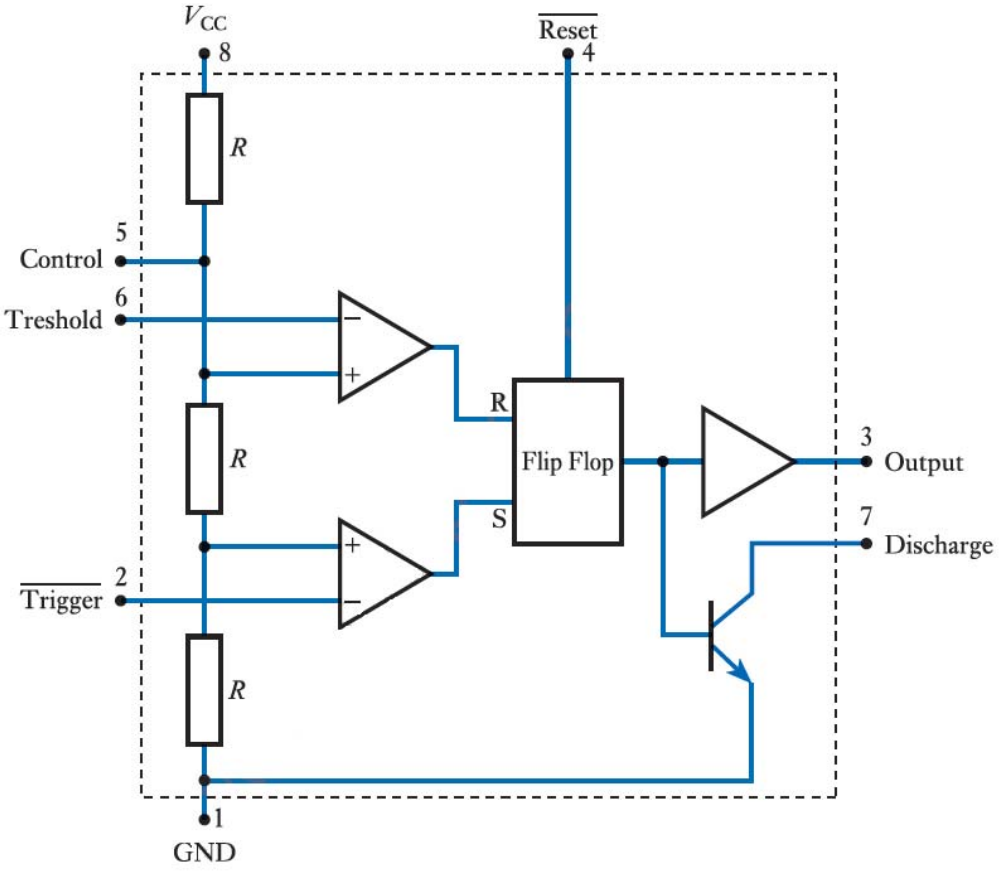
- A simplified circuit diagram of the **555 timer** is shown here
  - It consists basically of a flip-flop, two comparators, a switching transistor and a resistive network.



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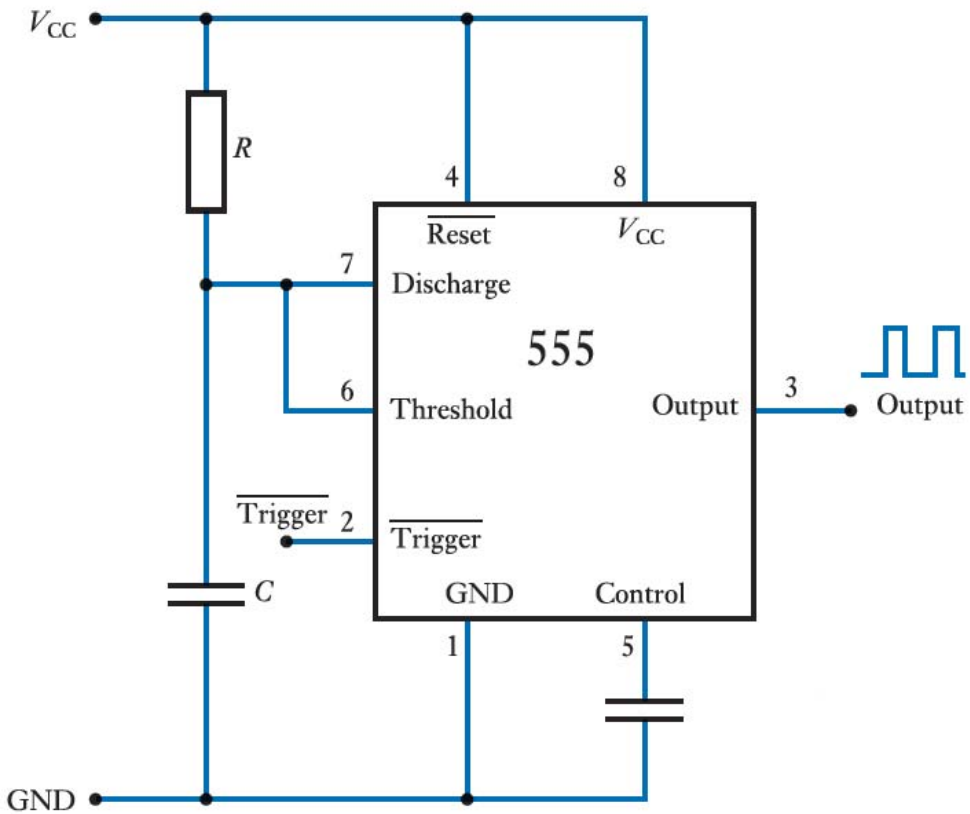
- The diagram here shows the 555 configured as a monostable.
  - It can be seen that only a couple of external components are needed.



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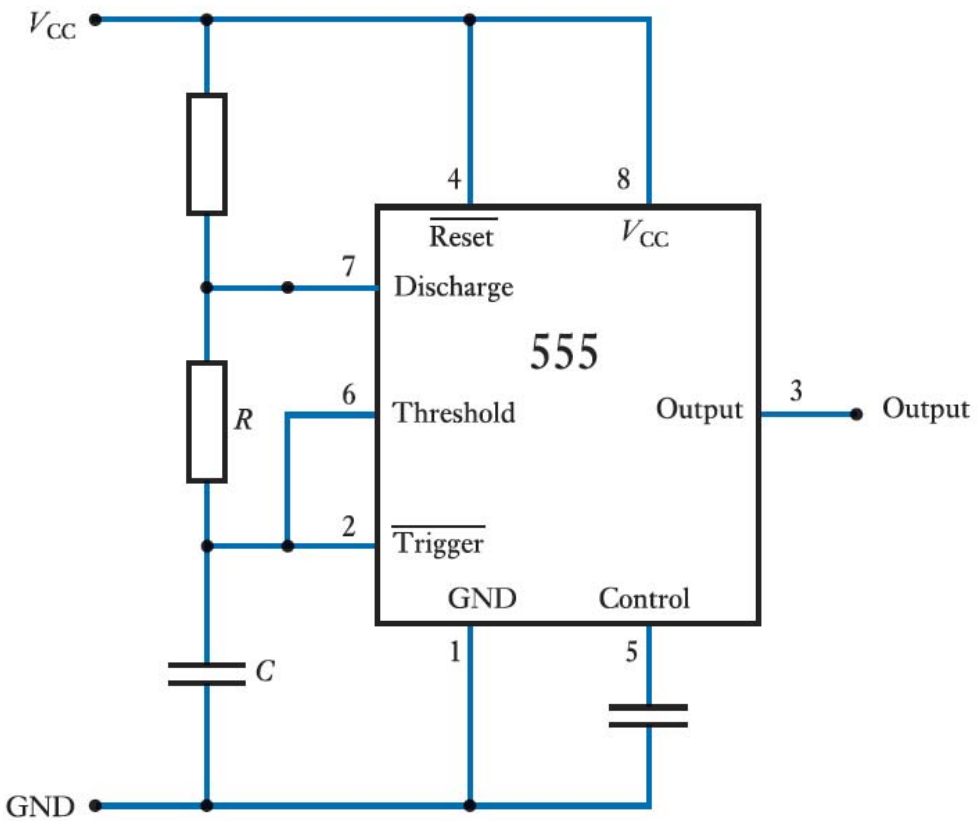
- Here the 555 is shown configured as an astable
  - Again very few additional components are required.



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Sequential Logic or Multivibrators
Logic with memory!

- **Bistables** ⇒two stable output states
  - Q=1 ($\bar{Q}$=0) and Q=0 ($\bar{Q}$=1)
  - Switch between the two with external signals
- **Monostables** ⇒one stable & one metastable states
  - External trigger switches from stable to metastable state
  - After a time (determined by circuit) return to stable state
- **Astable** ⇒this has two metastable states
  - Self switches between the two states with time constant determined by circuit components
  - digital oscillator or timer circuit

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- Questions?

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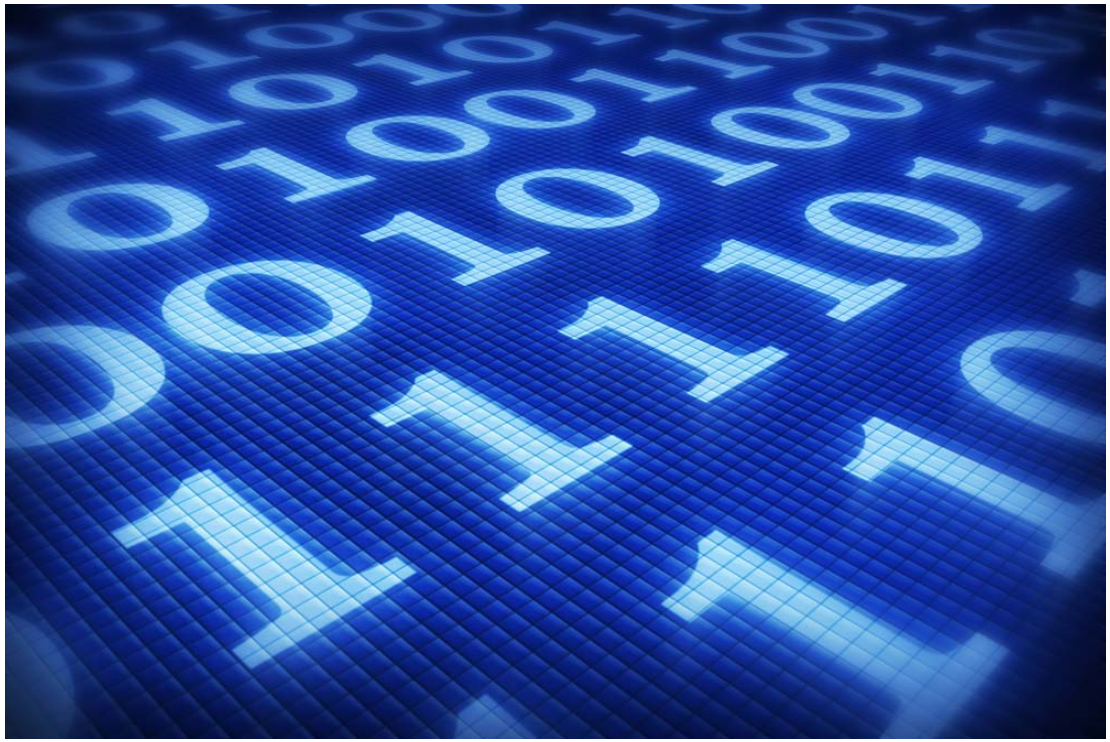
Chapter 25

Today: Sequential logic uses

- Introduction
- Bistables
- Monostables or one-shots
- Astables
- Timers
- Memory registers
- Shift registers
- Counters



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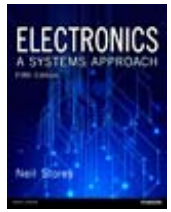
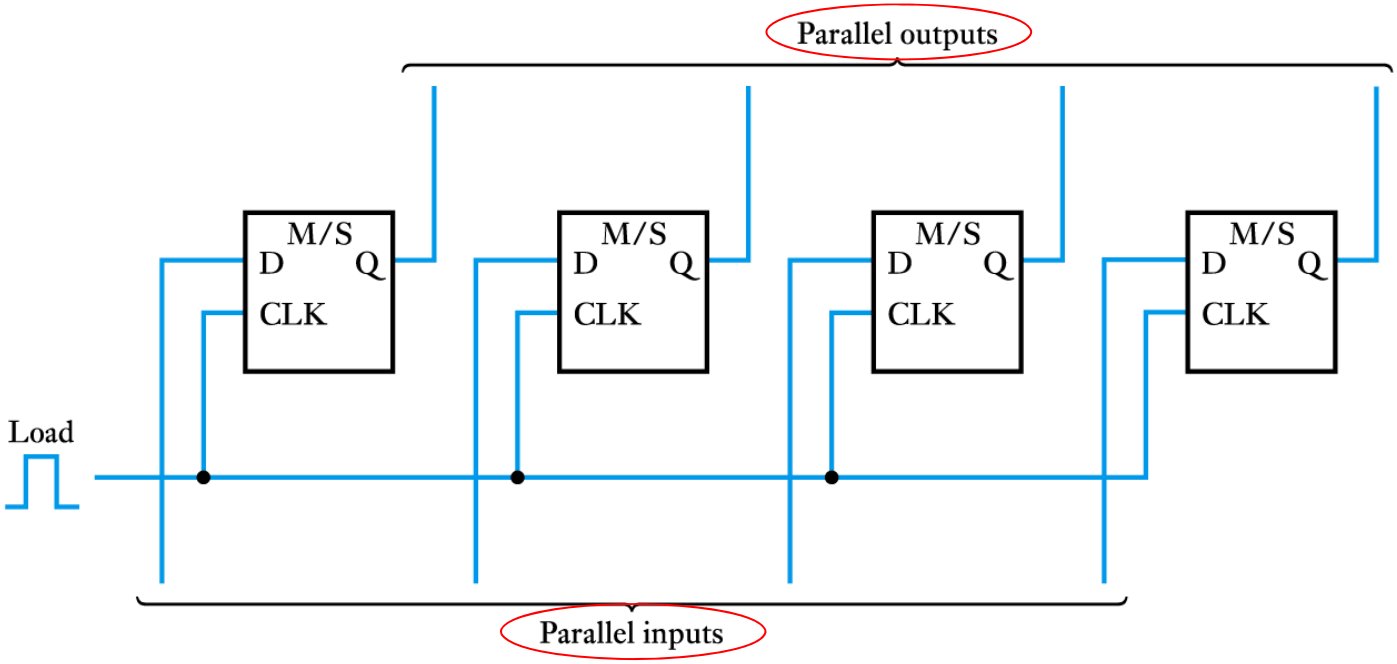


Memory Registers

- Combining a number of bistables we can construct a **memory register**
  - several forms of bistable can be used, for example:



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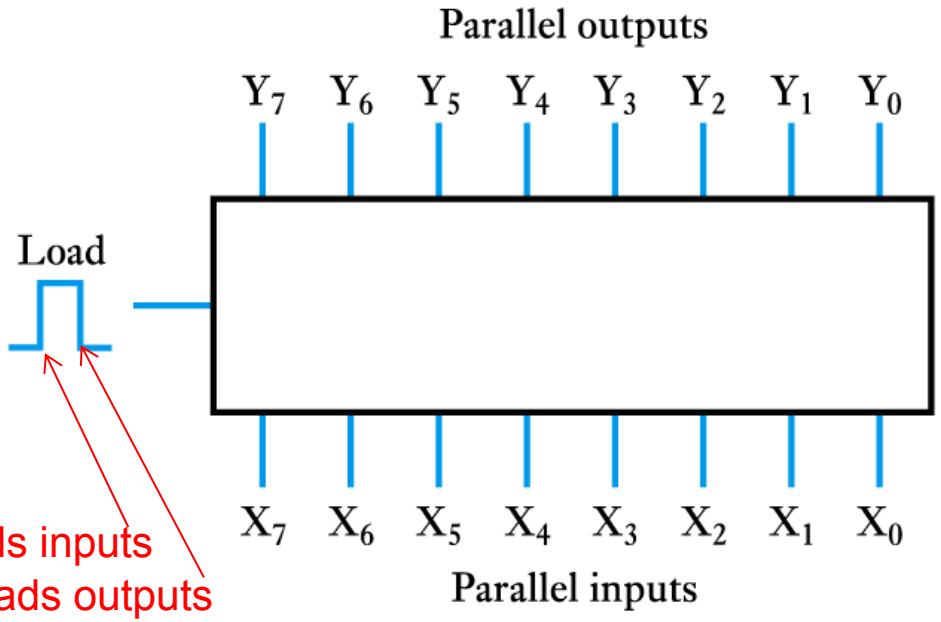
- Often we are not concerned with the internal construction of the register
  - they are a standard integrated component



M/S

Leading edge holds inputs

Falling edge loads outputs

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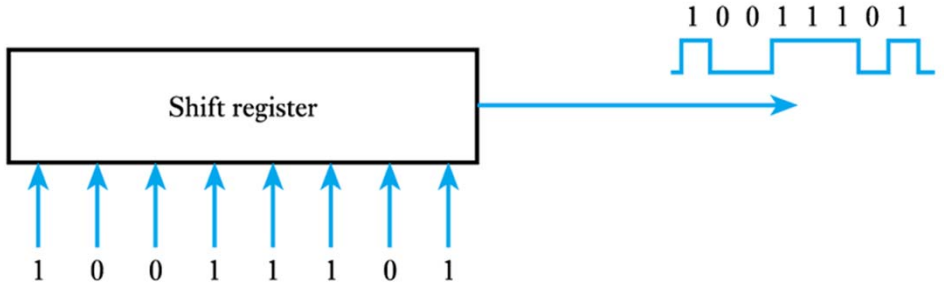
Shift Registers

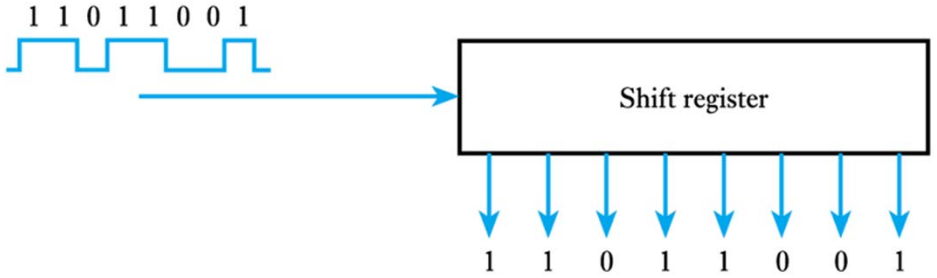
Video 25B

25.7

- **The operation of a shift register**



(a) Parallel to serial conversion



(b) Serial to parallel conversion

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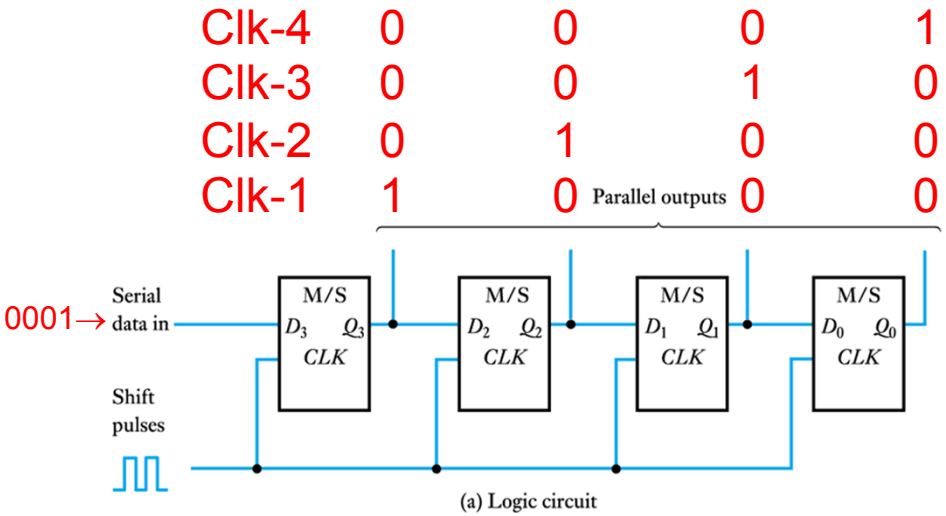
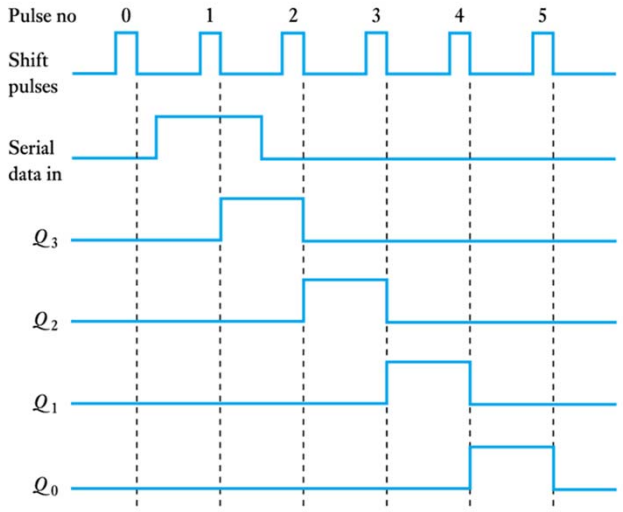
A simple serial to parallel shift register



(a) Logic circuit



(b) Waveform diagram

Every 4 Clk cycles we need to tell the reader to read the word

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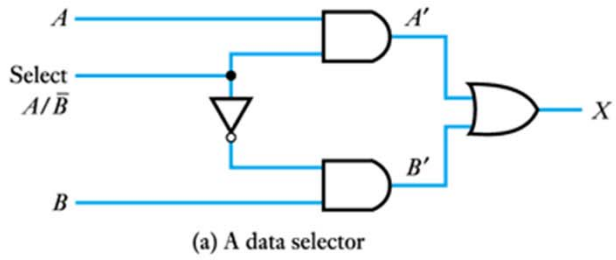
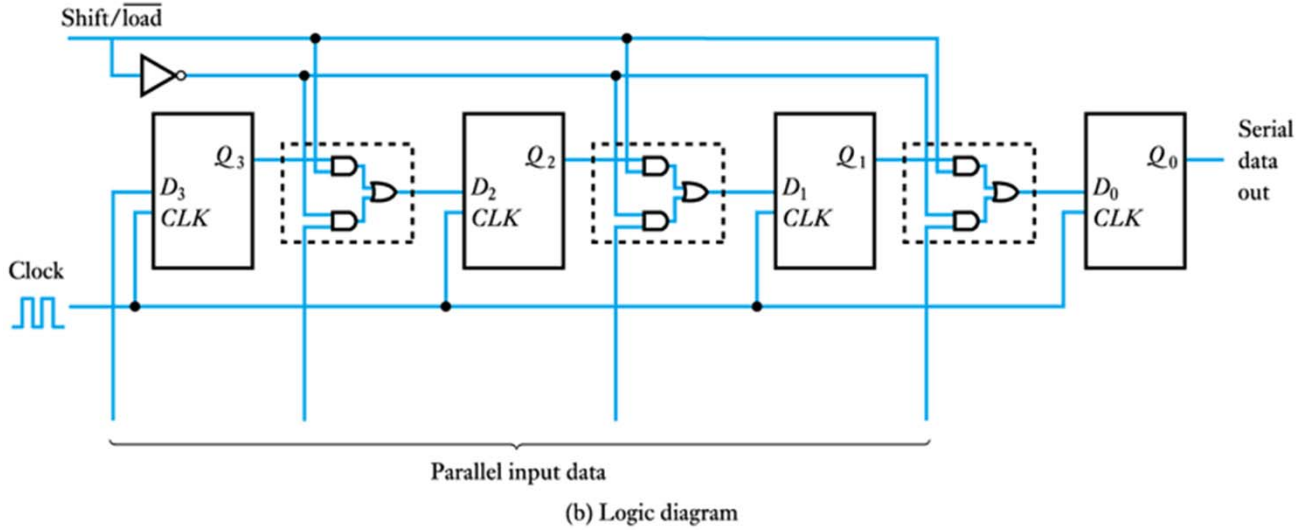
Need to change a memory register (parallel in-parallel out)
where the D's are independent inputs
To a shift register (parallel in-serial out)
where D is from the Q output of previous stage

- **A 4-bit parallel load shift register-**



(a) A data selector

Select=1⇒X = A
Select=0⇒X = B



(b) Logic diagram

Select=0⇒Each D connected to an input line
MEMORY REGISTER

Select=1⇒Each D connected to previous stage's output, Q
SHIFT REGISTER

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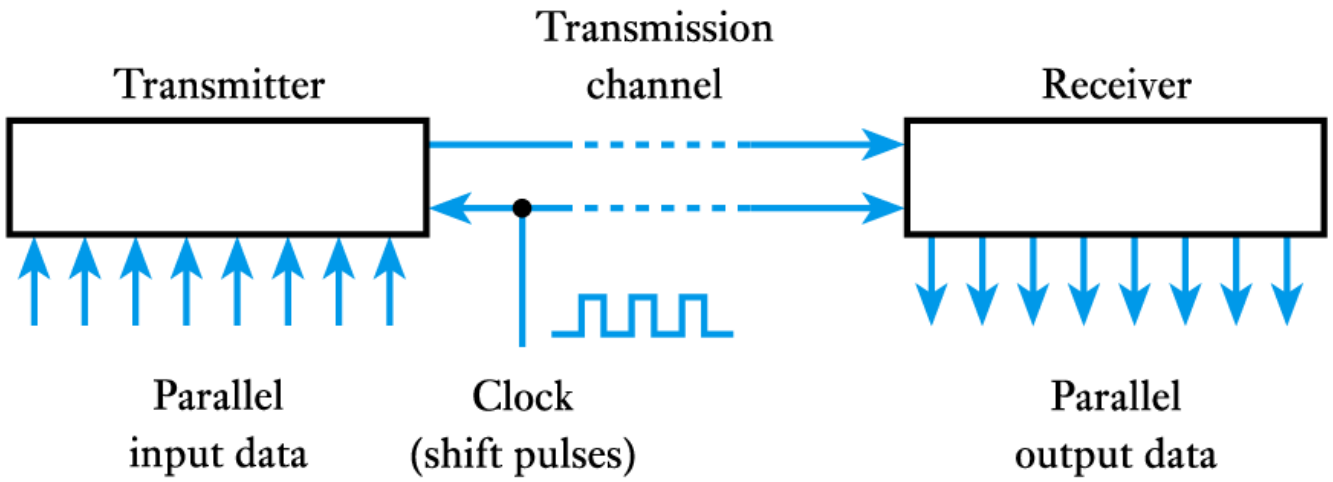
- **A design example** - see **Example 25.3** in course text

Application of a shift register

– shift registers are widely used in communications systems



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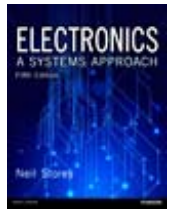
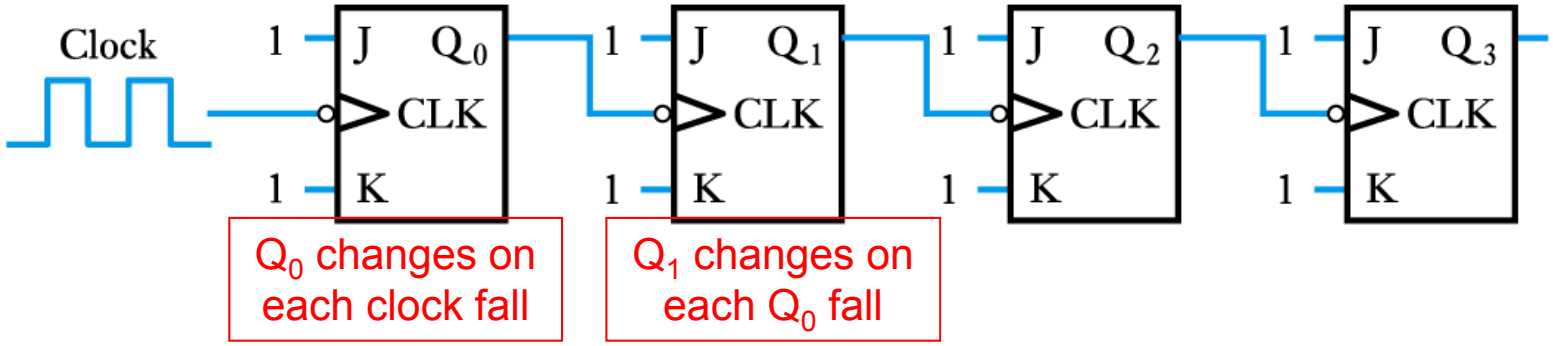
Counters

Video 25C



25.8

- **Ripple counters**
  - can be constructed using several forms of bistable
  - consider the following arrangement
  - with $J = K = 1$ each bistable toggles on the falling edge of its clock input



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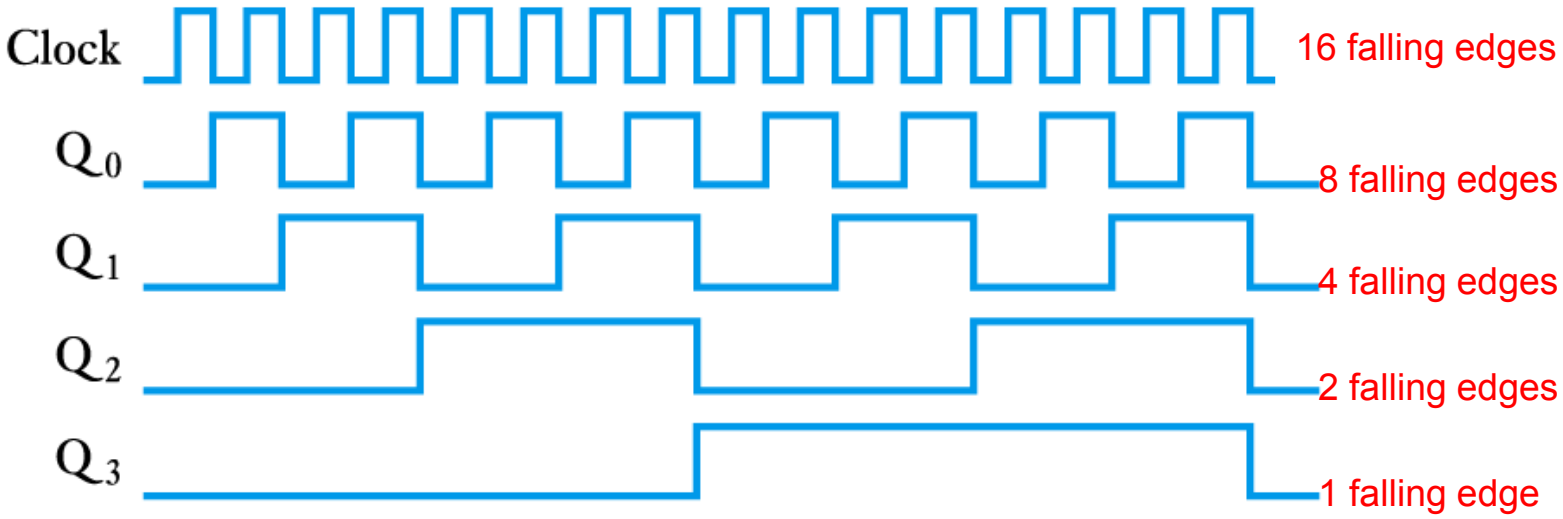
Remember our 4-bit serial to parallel converter
Wanted to tell reader to read on every 4th clock fall⇒Q_1



- Each stage toggles at half the frequency of the previous one
  - acts as a frequency divider
  - divides frequency by 2^n (where *n* is the number of stages)

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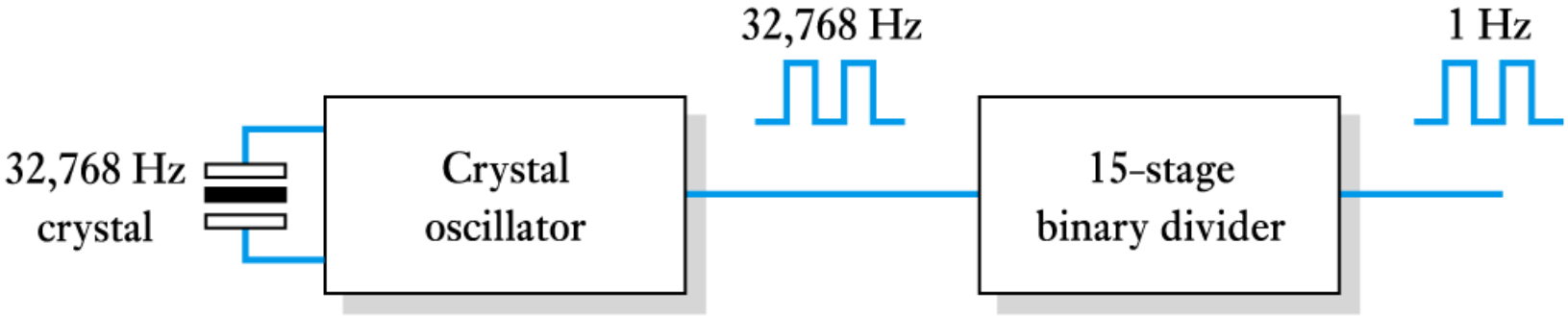
- **A design example -** see **Example 25.4** in course text

Clock generator for a digital watch

– 15-stage counter divides signal from a crystal oscillator by 32,768 to produce a 1 Hz signal to drive stepper motor or digital display



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- Consider the pattern on the outputs of the counter shown earlier – displayed on the right
- the outputs count in binary from 0 to 2^n-1 and then repeat
  - the circuit acts as a **modulo-2^n counter**
  - since the counting process propagates from one bistable to the next this is called a **ripple counter**
  - circuit shown is a **4-bit** or **modulo-16** (or **mod-16**) ripple counter

Number of clock pulses	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16	0	0	0	0
17	0	0	0	1
18	0	0	1	0
19	0	0	1	1
20	0	1	0	0

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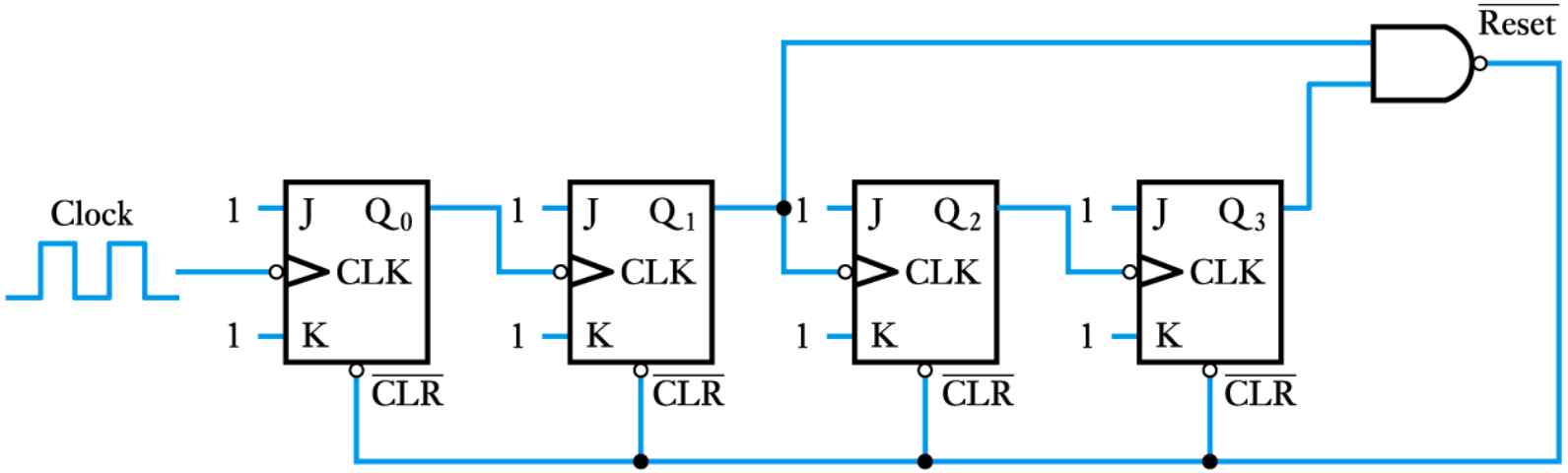
Reset when you detect the counter has reached a binary value.
Mod10$\Rightarrow 10_{10}$=1010, so first occasion one see bit 1 and 3 go high, reset

- **Modulo-*N* counters**
  - by using an appropriate number of stages the earlier counter can count modulo any power of 2
  - to count to any other base we add reset circuitry
  - e.g. the modulo-10 or decade counter shown here



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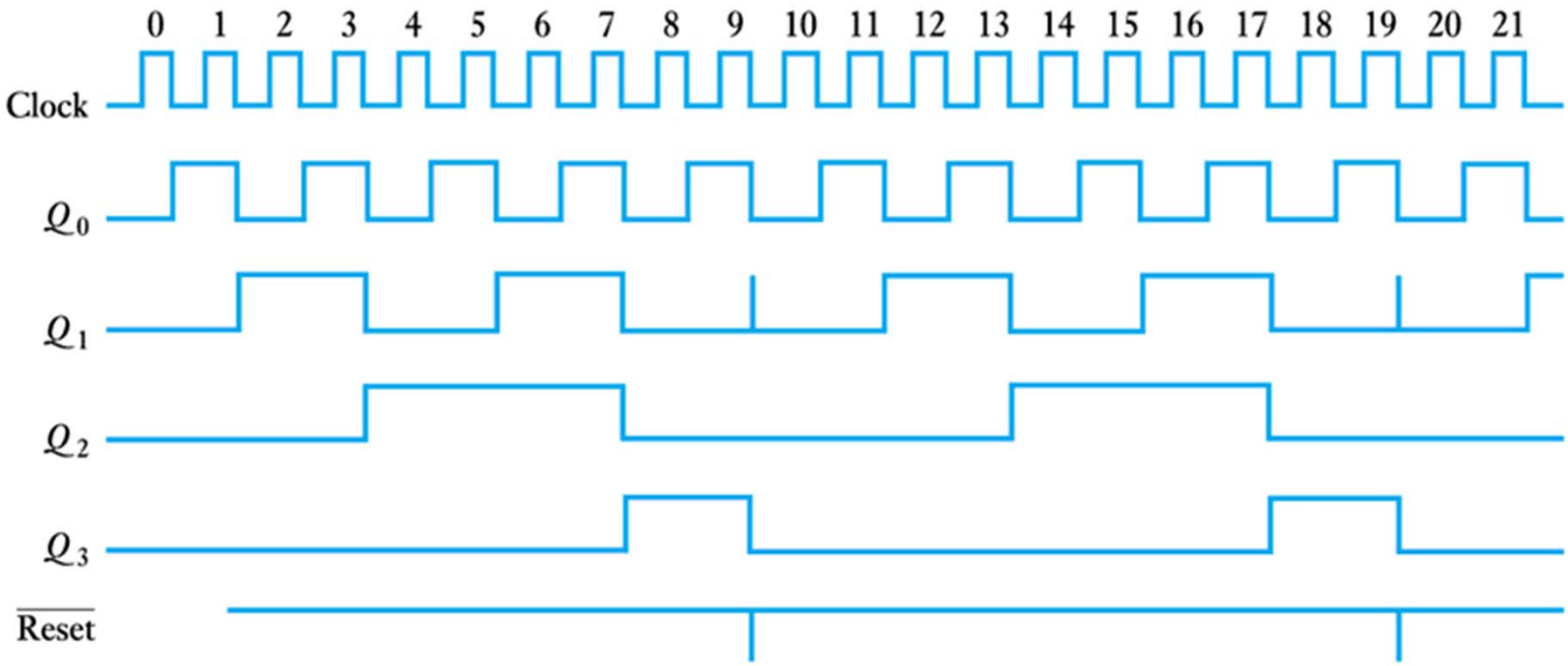
- **Waveform diagram for the decade counter**



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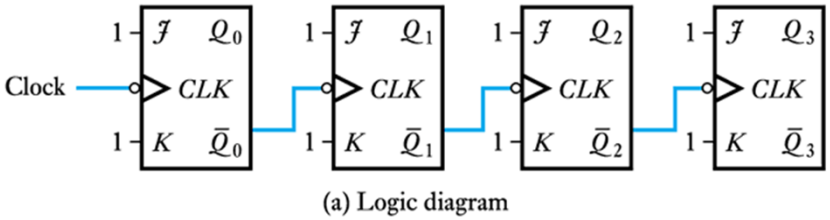
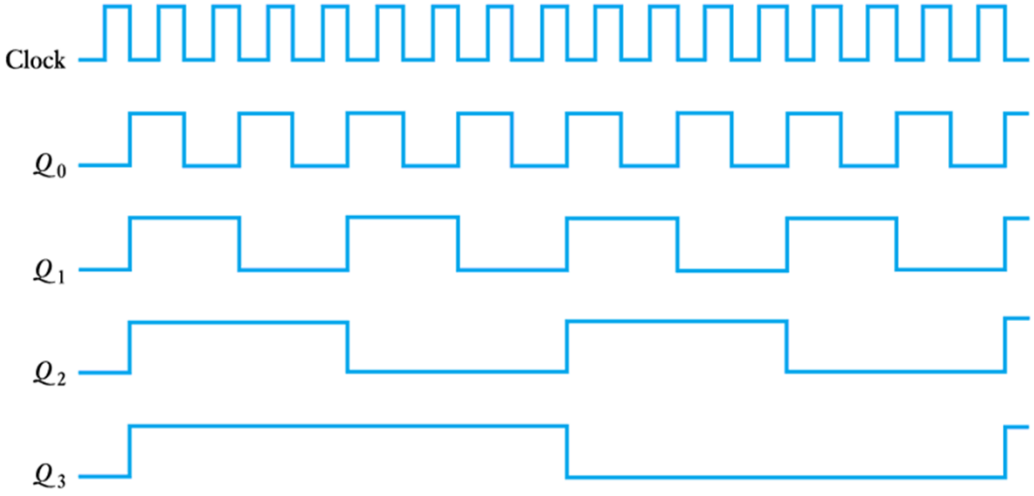
A ripple down counters



(a) Logic diagram



(b) Waveform diagram

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- **The output sequence of the ripple-down counter**

Number of clock pulses	Q_3	Q_2	Q_1	Q_0	Count
0	0	0	0	0	0
1	1	1	1	1	15
2	1	1	1	0	14
3	1	1	0	1	13
4	1	1	0	0	12
5	1	0	1	1	11
6	1	0	1	0	10
7	1	0	0	1	9
8	1	0	0	0	8
9	0	1	1	1	7
10	0	1	1	0	6
11	0	1	0	1	5
12	0	1	0	0	4
13	0	0	1	1	3
14	0	0	1	0	2
15	0	0	0	1	1
16	0	0	0	0	0
17	1	1	1	1	15
18	1	1	1	0	14
19	1	1	0	1	13
20	1	1	0	0	12

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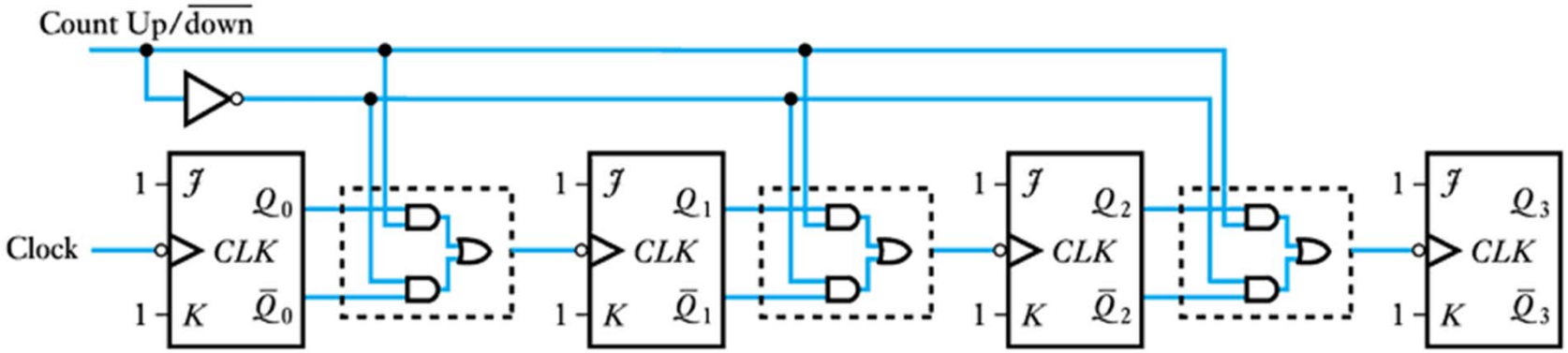
An up/down counter



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- **Propagation delay in ripple counters**
  - while ripple counters are very simple they suffer from problems at high speed
  - since the output of one flip-flop is triggered by the change of the previous device, delays produced by each flip-flop are summed along the chain
  - the time for a single device to respond is termed its **propagation delay time** t_{PD}
  - an n-bit counter will take $n \times t_{PD}$ to respond
  - if read before this time the result will be garbled

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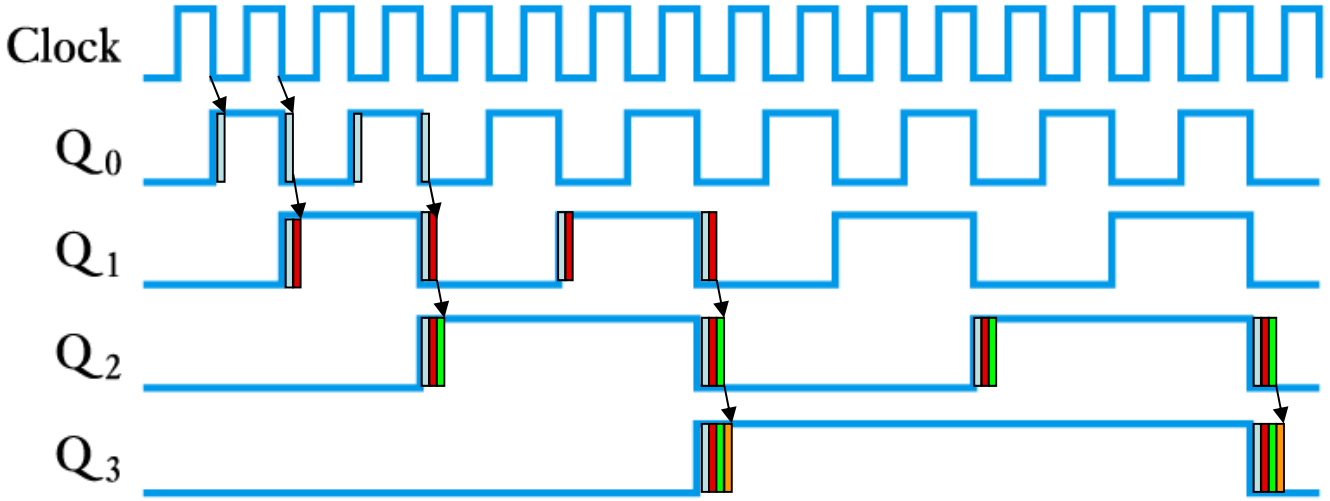
Counters (contd.)

- With a ripple counter, what we really have at each transition is a slight delay from clock fall to output Q_n change:
- But each output Q_n change is the clock to the next stage, which adds its own delay from this clock fall to its output Q_{n+1}!



So since each output feeds that delay into next clock:
Final bit has the delay of $gate_0$, $gate_1$, $gate_2$ and $gate_3$

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- **Synchronous counters**
  - these overcome the propagation delay in ripple counters by connecting all the flip-flops to the same clock signal
  - thus each stage changes state at the same time
  - additional circuitry is used to determine which stages change state on each clock pulse
  - faster than ripple counters but more complex
  - available in many forms including up, down, up/down and modulo-*N* counters

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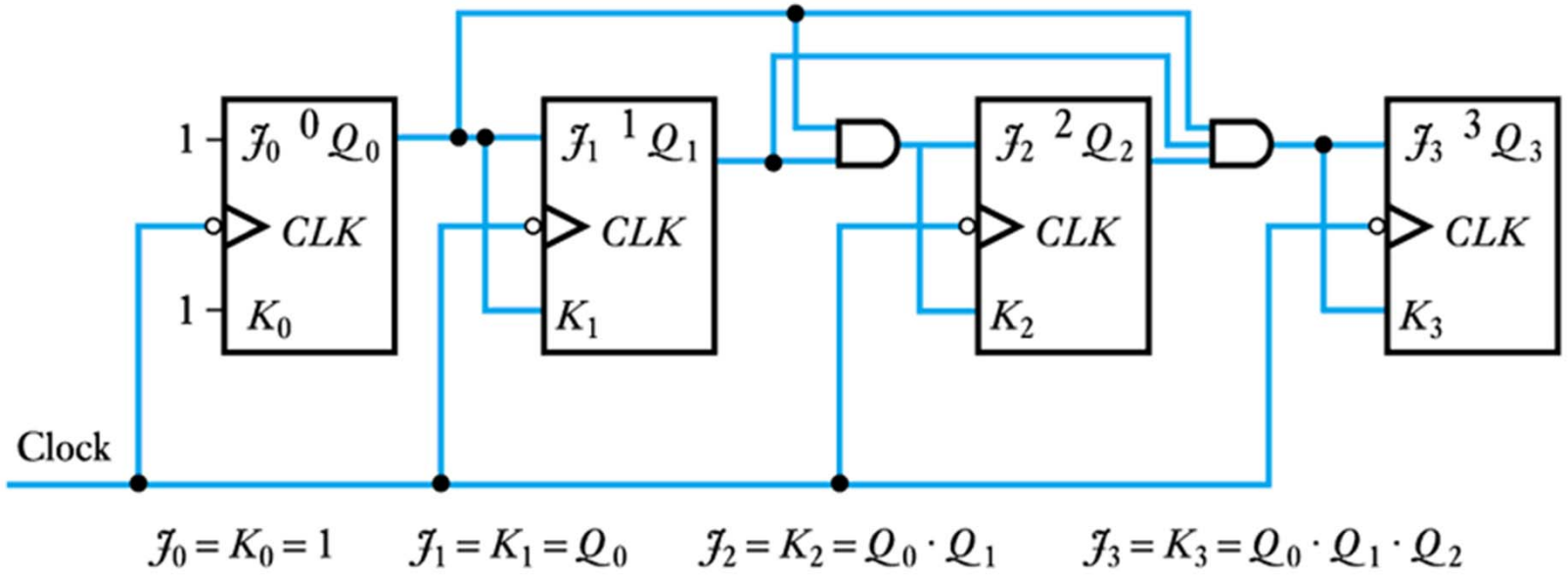
A synchronous four-stage counter



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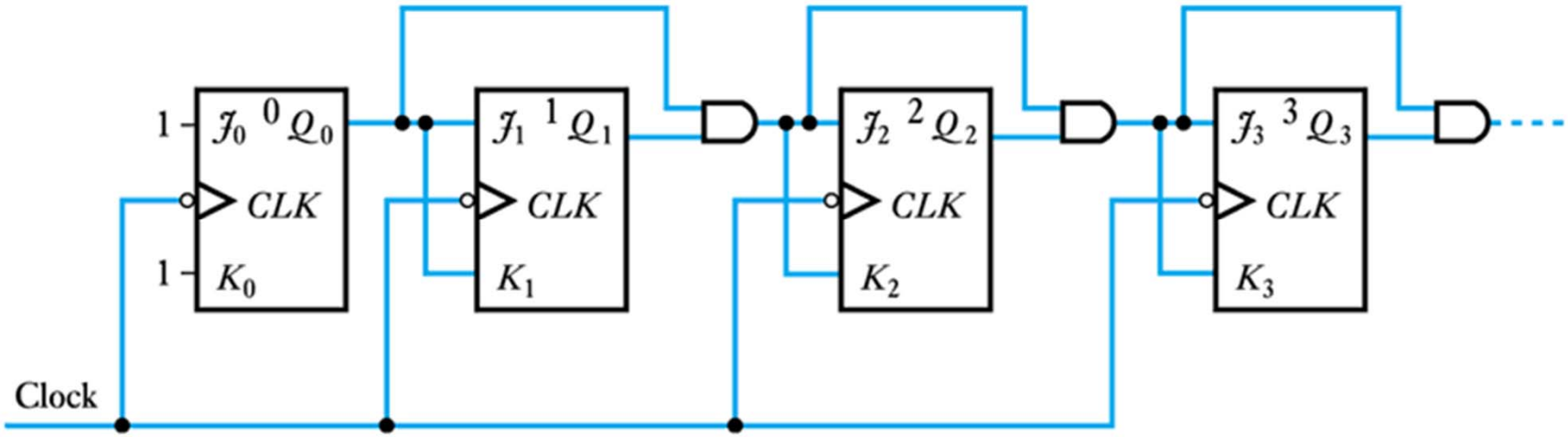
- **A cascadable 4-bit synchronous counter**



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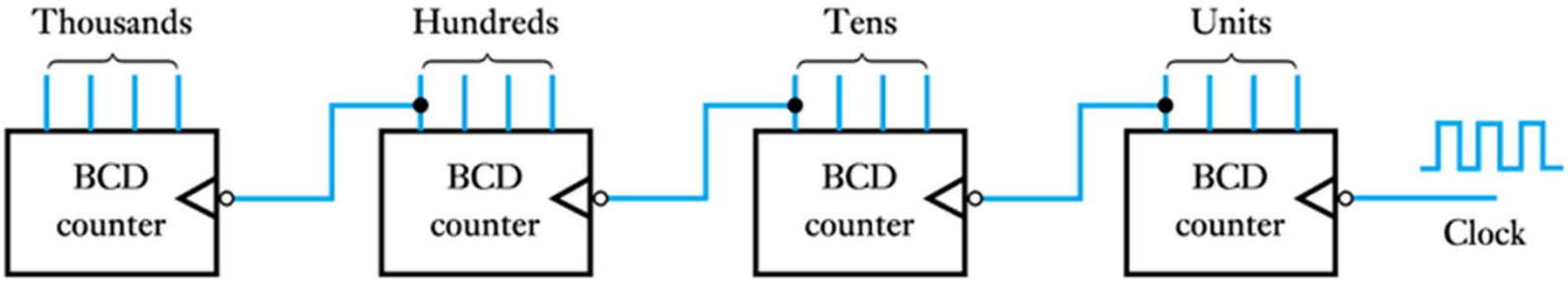
- **Integrated circuit counters**
  - while we can build counters from flip-flops, we more often use dedicated ICs
  - these are available in numerous forms, such as binary, decade, BCD, up, down and up/down
  - they are normally designed to simplify cascading



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Design of Sequential Logic Circuits

- Sequential systems may be **synchronous** or **asynchronous**
  - the design stages involved are similar, although synchronous design is slightly easier
  - the major elements of synchronous design are
    - identification of the system states
    - a state transition diagram
    - a state transition table
    - state reduction
    - state assignment
    - generation of an excitation table
    - circuit design
    - investigation of unused states

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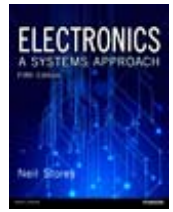
Further Study

Video 25D Further Study



- The Further Study section at the end of Chapter 25 looks at the design of a digital stopwatch.
- The watch has a display showing seconds and minutes, and three pushbuttons.
- Apply the techniques described in this lecture to design such a watch, then compare your design with that given in the video.

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Key points

- Sequential logic circuits have the characteristic of memory
- Among the most important groups of sequential components are the various forms of multivibrator
  - bistables
  - monostables
  - astables
- The most widely used form is the bistable which includes
  - latches, edge-triggered flip-flops and master/slave devices
- Registers form the basis of various memories
- Counters are widely used in a range of applications
- Monostables and astables perform a range of functions

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