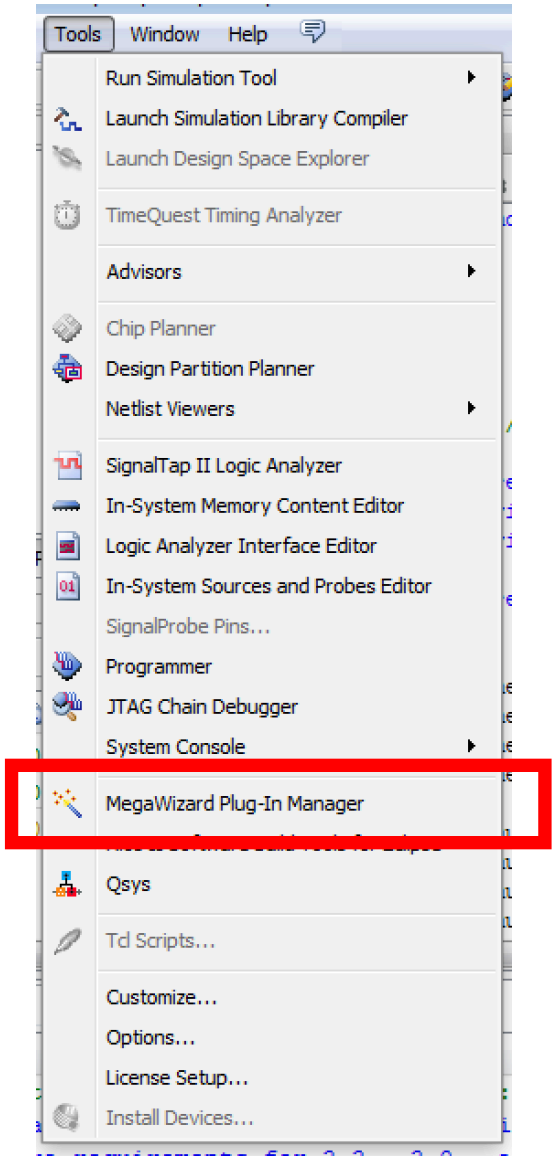
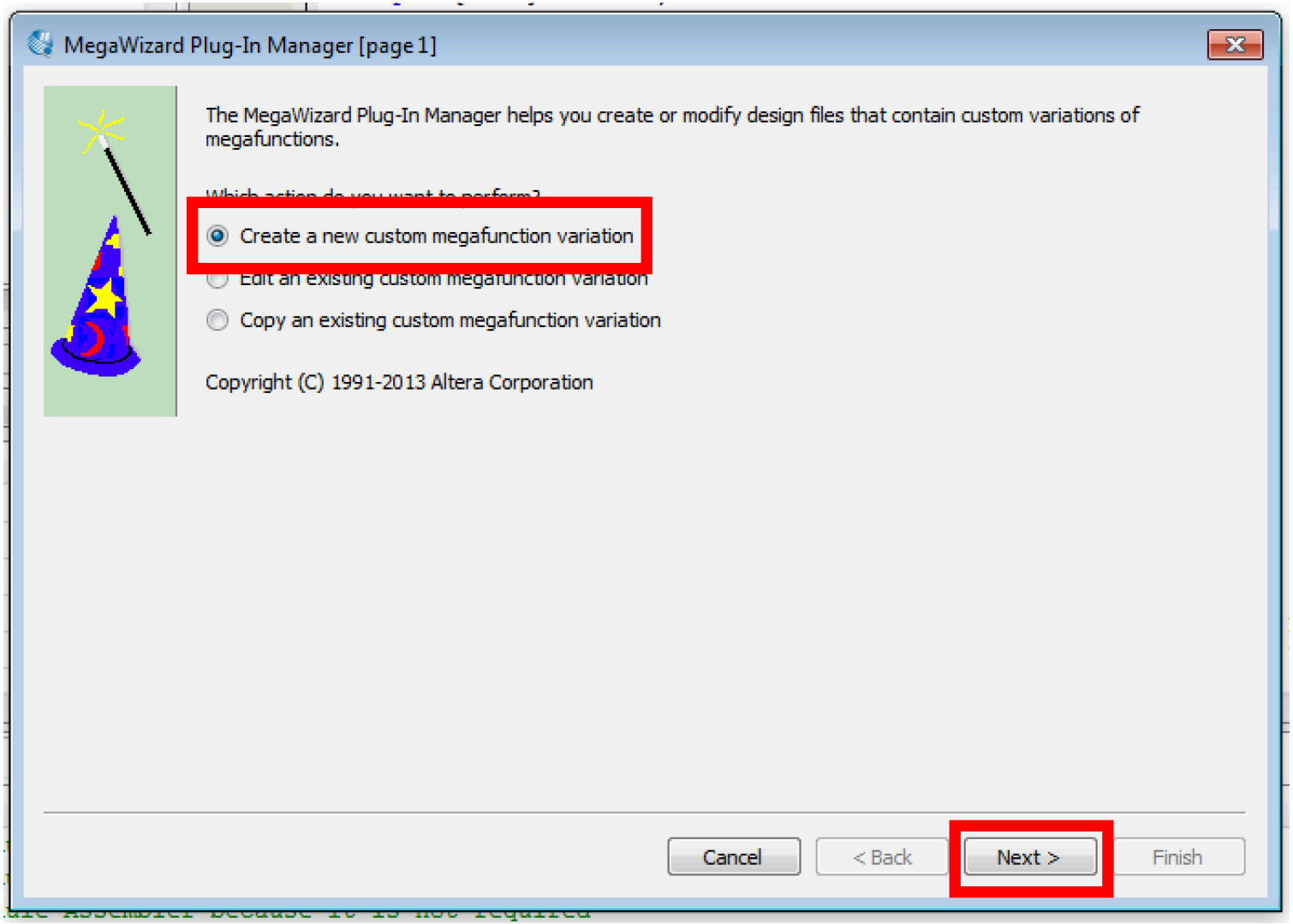
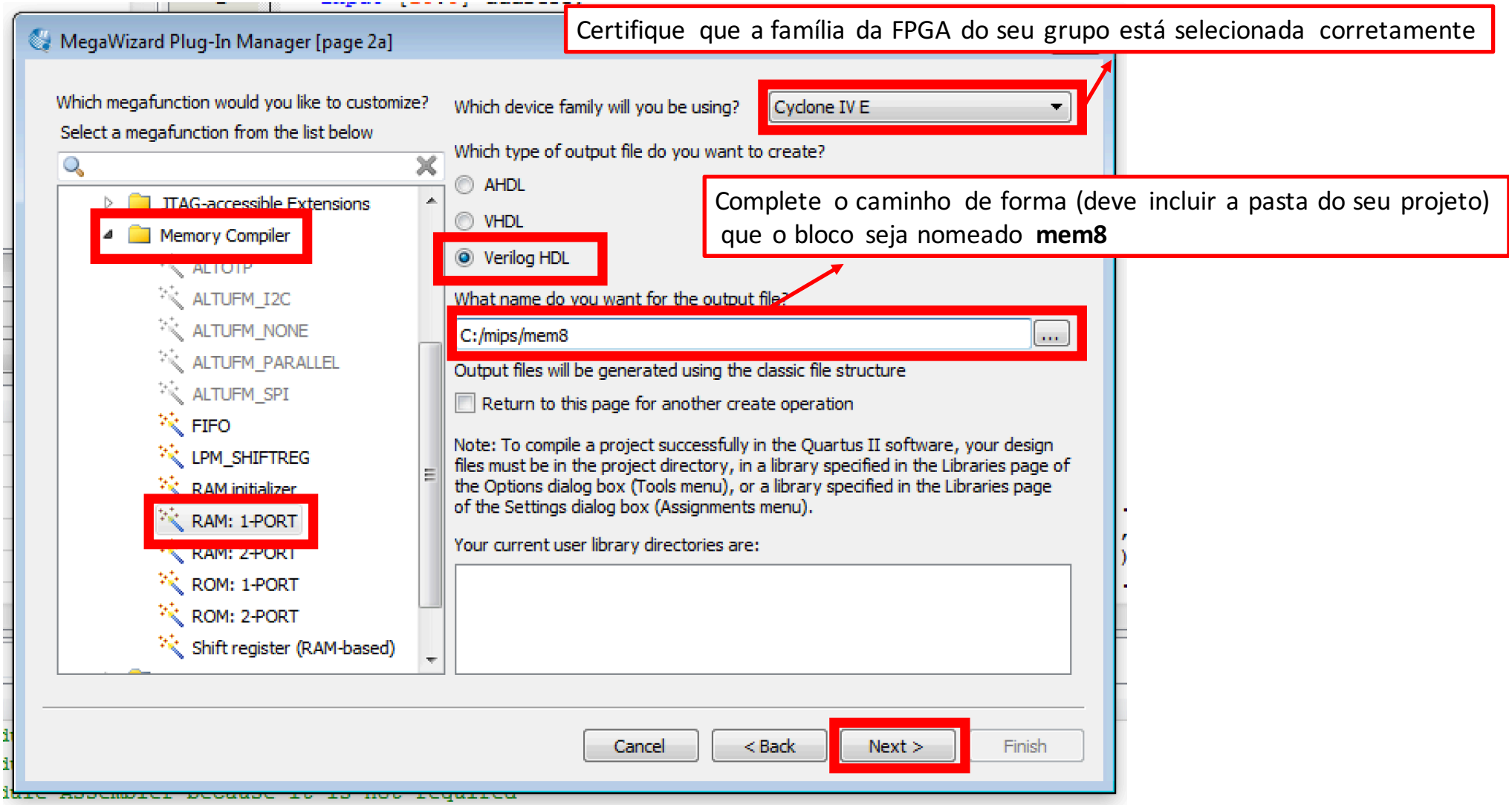
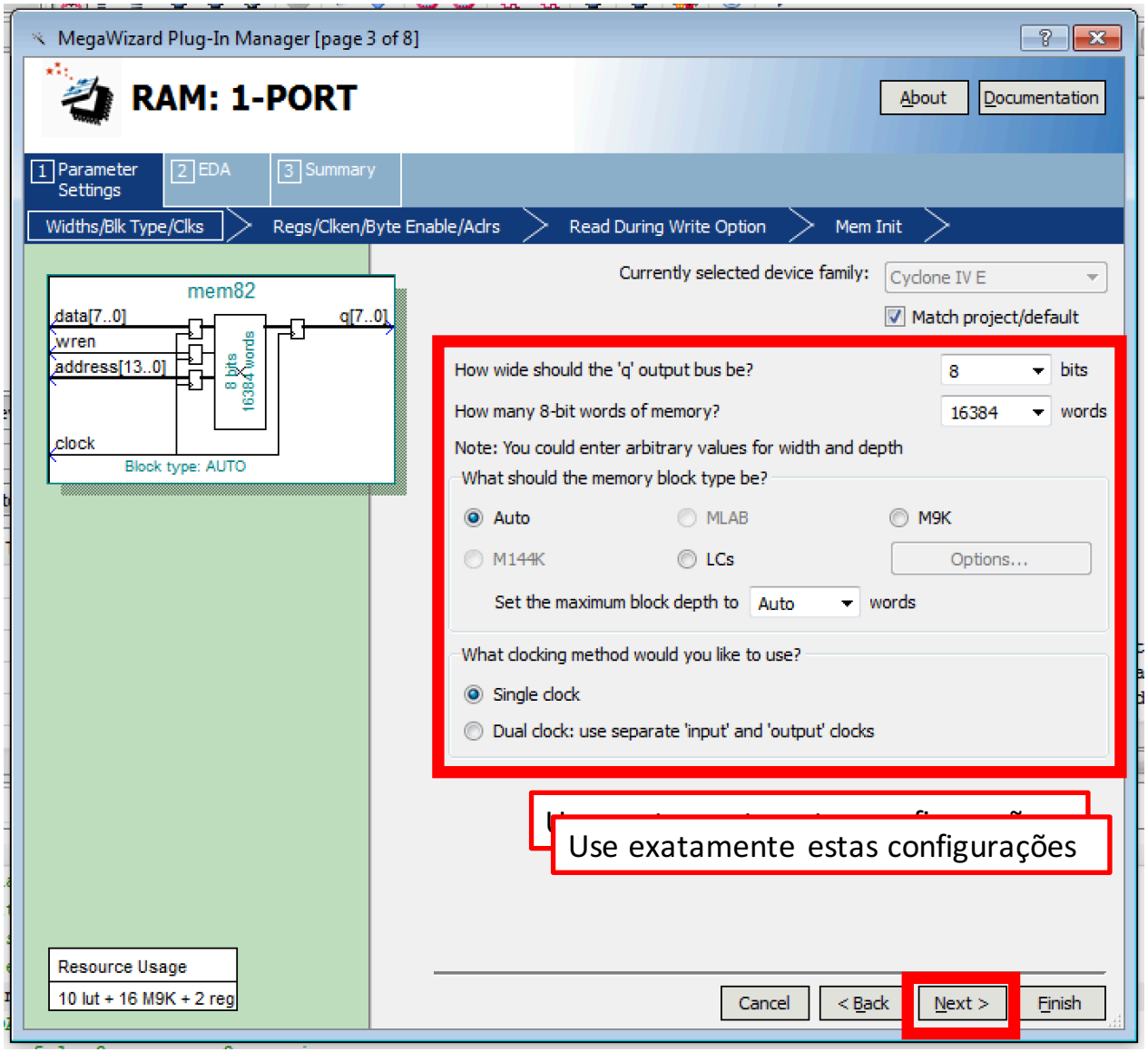
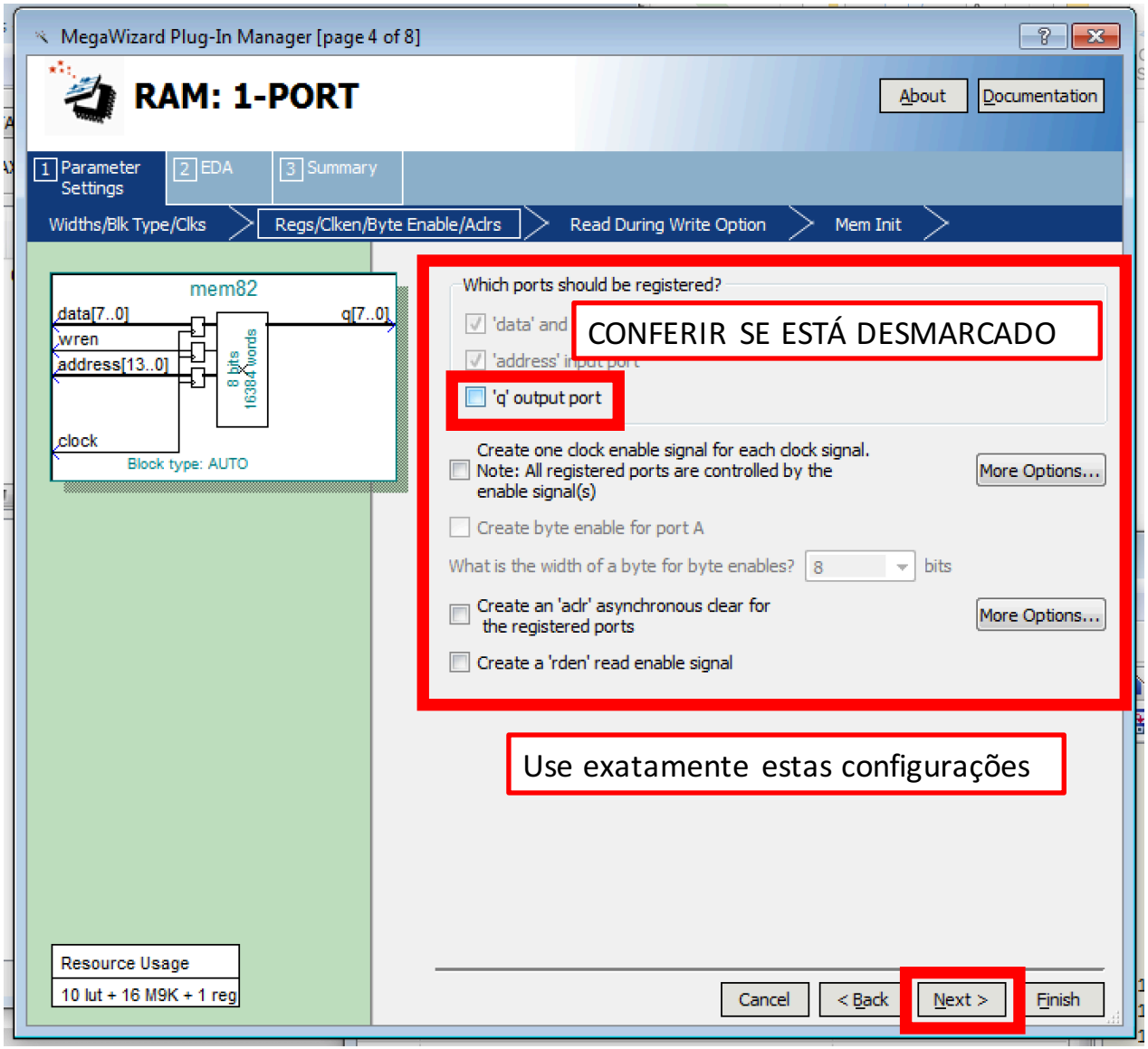


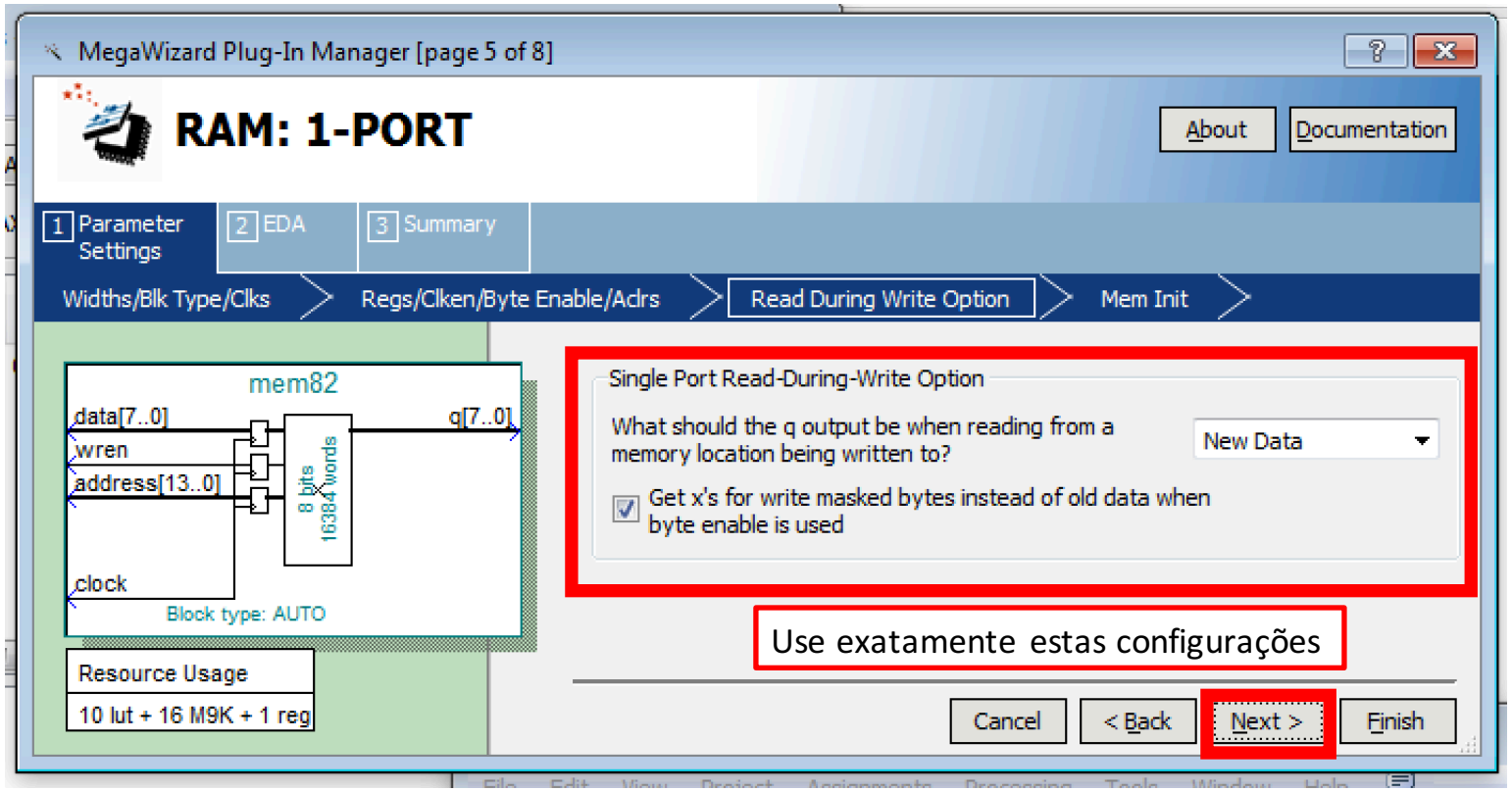
Após criar o projeto, **selecionando o modelo correto da FPGA do seu grupo**, utilize o menu "Tools" e inicie o MegaWizard

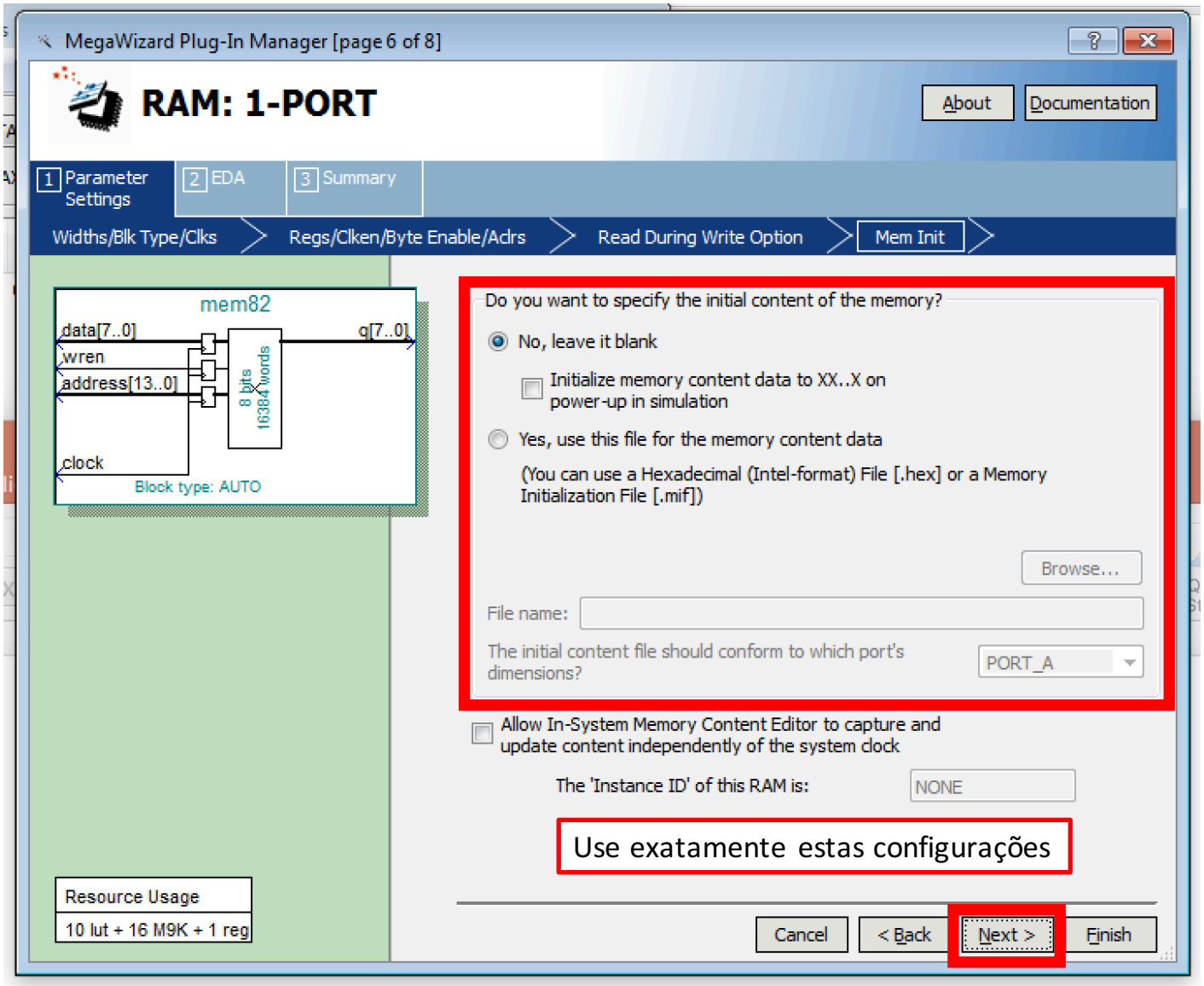

MegaWizard Plug-In Manager [page 1]
The MegaWizard Plug-In Manager helps you create or modify design files that contain custom variations of megafunctions.
Create a new custom megafunction variation
Edit an existing custom megafunction variation
Copy an existing custom megafunction variation
Copyright (C) 1991-2013 Altera Corporation
Cancel
< Back
Next >
Finish

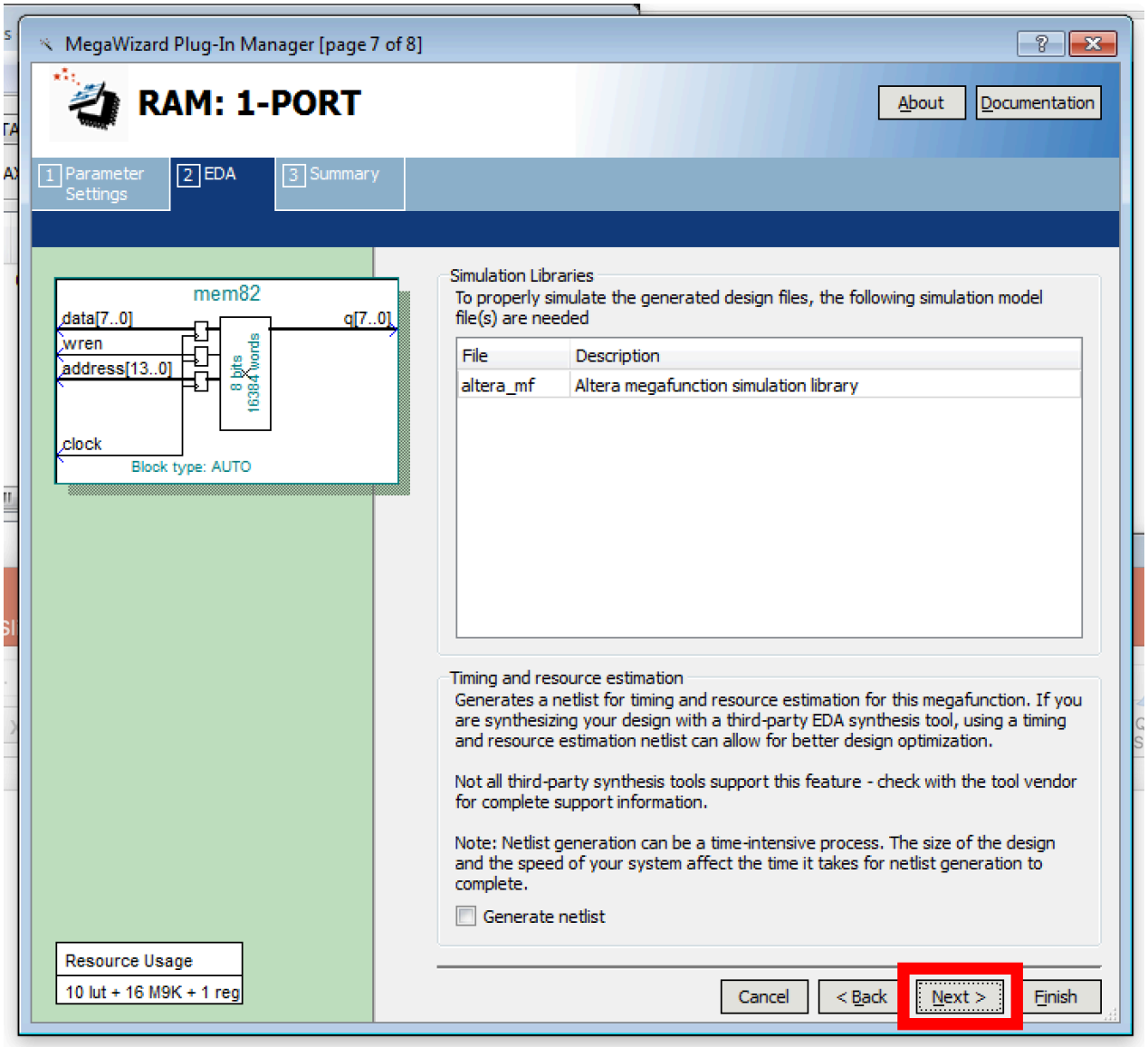

MegaWizard Plug-In Manager [page 2a]
Certifique que a família da FPGA do seu grupo está selecionada corretamente
Which megafunction would you like to customize?
Select a megafunction from the list below
Which device family will you be using?
Cyclone IV E
Which type of output file do you want to create?
AHDL
VHDL
Verilog HDL
Complete o caminho de forma (deve incluir a pasta do seu projeto) que o bloco seja nomeado mem8
What name do you want for the output file?
C:/mips/mem8
...
Output files will be generated using the classic file structure
Return to this page for another create operation
Note: To compile a project successfully in the Quartus II software, your design files must be in the project directory, in a library specified in the Libraries page of the Options dialog box (Tools menu), or a library specified in the Libraries page of the Settings dialog box (Assignments menu).
Your current user library directories are:
JTAG-accessible Extensions
Memory Compiler
ALTUFM_I2C
ALTUFM_NONE
ALTUFM_PARALLEL
ALTUFM_SPI
FIFO
LPM_SHIFTREG
RAM initializer
RAM: 1-PORT
RAM: 2-PORT
ROM: 1-PORT
ROM: 2-PORT
Shift register (RAM-based)
Cancel
< Back
Next >
Finish

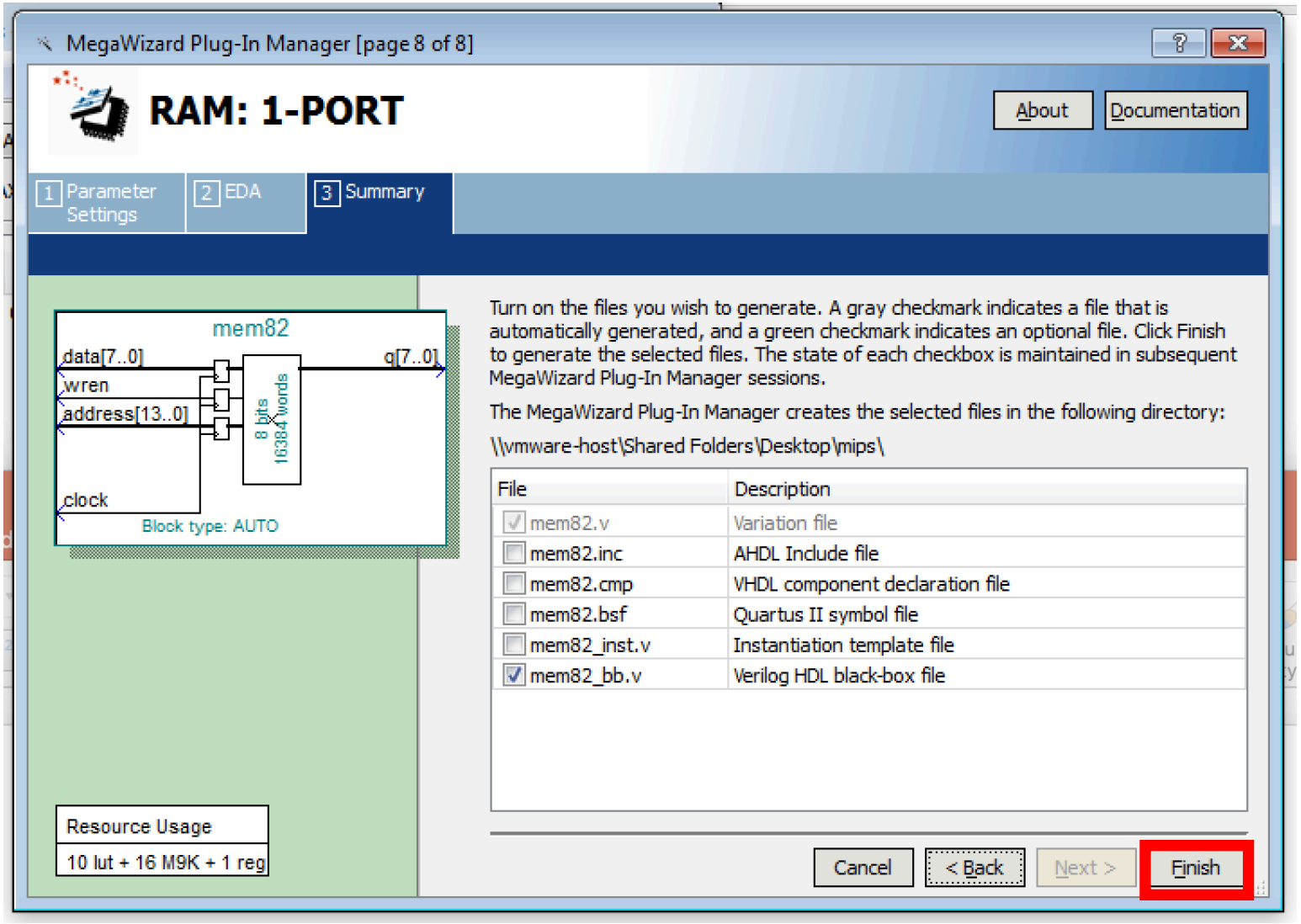

MegaWizard Plug-In Manager [page 3 of 8]
RAM: 1-PORT
About
Documentation
1 Parameter Settings
2 EDA
3 Summary
Widths/Blk Type/Clks
Regs/Clken/Byte Enable/Adrs
Read During Write Option
Mem Init
mem82
data[7..0]
wren
address[13..0]
clock
q[7..0]
8 bits
16384 words
Block type: AUTO
Currently selected device family:
Cyclone IV E
Match project/default
How wide should the 'q' output bus be?
8
bits
How many 8-bit words of memory?
16384
words
Note: You could enter arbitrary values for width and depth
What should the memory block type be?
Auto
MLAB
M9K
M144K
LCs
Options...
Set the maximum block depth to
Auto
words
What clocking method would you like to use?
Single clock
Dual clock: use separate 'input' and 'output' clocks
Use exatamente estas configurações
Resource Usage
10 lut + 16 M9K + 2 reg
Cancel
< Back
Next >
Finish

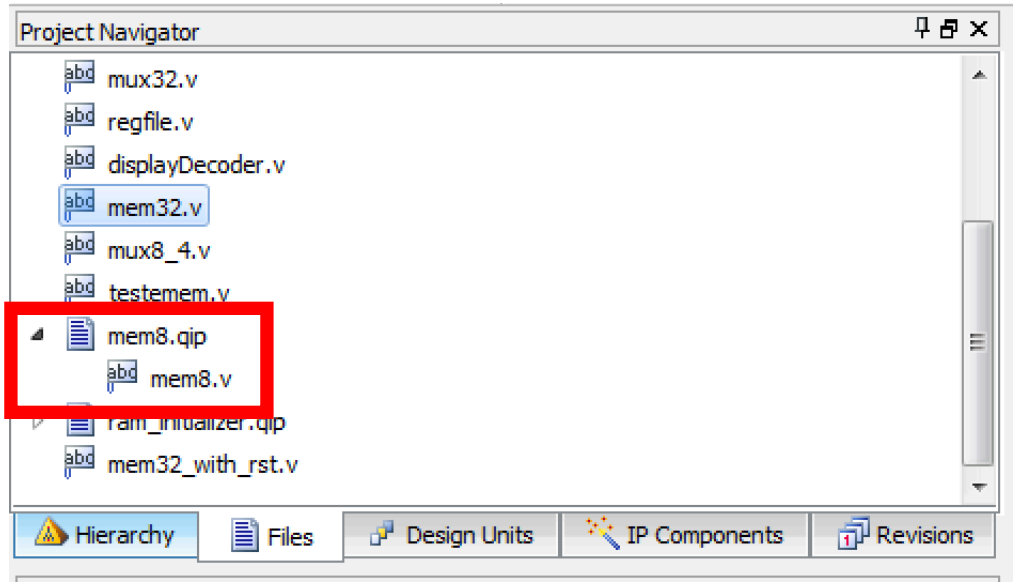

MegaWizard Plug-In Manager [page 4 of 8]
RAM: 1-PORT
About
Documentation
1 Parameter Settings
2 EDA
3 Summary
Widths/Blk Type/Clks
Regs/Clken/Byte Enable/Aclrs
Read During Write Option
Mem Init
mem82
data[7..0]
wren
address[13..0]
clock
q[7..0]
8 bits
16384 words
Block type: AUTO
Which ports should be registered?
'data' and
CONFERIR SE ESTÁ DESMARCADO
'address' input port
'q' output port
Create one clock enable signal for each clock signal.
Note: All registered ports are controlled by the enable signal(s)
More Options...
Create byte enable for port A
What is the width of a byte for byte enables?
8
bits
Create an 'aclr' asynchronous clear for the registered ports
More Options...
Create a 'rden' read enable signal
Use exatamente estas configurações
Resource Usage
10 lut + 16 M9K + 1 reg
Cancel
< Back
Next >
Finish


MegaWizard Plug-In Manager [page 5 of 8]
RAM: 1-PORT
About
Documentation
1 Parameter Settings
2 EDA
3 Summary
Widths/Blk Type/Clks
Regs/Clken/Byte Enable/Adrs
Read During Write Option
Mem Init
mem82
data[7..0]
wren
address[13..0]
clock
q[7..0]
8 bits
16384 words
Block type: AUTO
Resource Usage
10 lut + 16 M9K + 1 reg
Single Port Read-During-Write Option
What should the q output be when reading from a memory location being written to?
New Data
Get x's for write masked bytes instead of old data when byte enable is used
Use exatamente estas configurações
Cancel
< Back
Next >
Finish


MegaWizard Plug-In Manager [page 6 of 8]
RAM: 1-PORT
About
Documentation
1 Parameter Settings
2 EDA
3 Summary
Widths/Blk Type/Clks
Regs/Clken/Byte Enable/Aclrs
Read During Write Option
Mem Init
mem82
data[7..0]
wren
address[13..0]
clock
q[7..0]
8 bits
16384 words
Block type: AUTO
Do you want to specify the initial content of the memory?
No, leave it blank
Initialize memory content data to XX..X on power-up in simulation
Yes, use this file for the memory content data
(You can use a Hexadecimal (Intel-format) File [.hex] or a Memory Initialization File [.mif])
Browse...
File name:
The initial content file should conform to which port's dimensions?
PORT_A
Allow In-System Memory Content Editor to capture and update content independently of the system clock
The 'Instance ID' of this RAM is:
NONE
Use exatamente estas configurações
Resource Usage
10 lut + 16 M9K + 1 reg
Cancel
< Back
Next >
Finish


MegaWizard Plug-In Manager [page 7 of 8]
RAM: 1-PORT
About
Documentation
1 Parameter Settings
2 EDA
3 Summary
mem82
data[7..0]
wren
address[13..0]
clock
q[7..0]
8 bits
16384 words
Block type: AUTO
Simulation Libraries
To properly simulate the generated design files, the following simulation model file(s) are needed
File
Description
altera_mf
Altera megafunction simulation library
Timing and resource estimation
Generates a netlist for timing and resource estimation for this megafunction. If you are synthesizing your design with a third-party EDA synthesis tool, using a timing and resource estimation netlist can allow for better design optimization.
Not all third-party synthesis tools support this feature - check with the tool vendor for complete support information.
Note: Netlist generation can be a time-intensive process. The size of the design and the speed of your system affect the time it takes for netlist generation to complete.
Generate netlist
Resource Usage
10 lut + 16 M9K + 1 reg
Cancel
< Back
Next >
Finish


MegaWizard Plug-In Manager [page 8 of 8]
RAM: 1-PORT
About
Documentation
1 Parameter Settings
2 EDA
3 Summary
mem82
data[7..0]
wren
address[13..0]
clock
q[7..0]
8 bits
16384 words
Block type: AUTO
Turn on the files you wish to generate. A gray checkmark indicates a file that is automatically generated, and a green checkmark indicates an optional file. Click Finish to generate the selected files. The state of each checkbox is maintained in subsequent MegaWizard Plug-In Manager sessions.
The MegaWizard Plug-In Manager creates the selected files in the following directory:
\\vmware-host\Shared Folders\Desktop\mips\
File
Description
mem82.v
Variation file
mem82.inc
AHDL Include file
mem82.cmp
VHDL component declaration file
mem82.bsf
Quartus II symbol file
mem82_inst.v
Instantiation template file
mem82_bb.v
Verilog HDL black-box file
Resource Usage
10 lut + 16 M9K + 1 reg
Cancel
< Back
Next >
Finish



Após a finalização, verifique se o bloco mem8 foi criado corretamente no seu projeto. Caso necessite, verifique a especificação de uso no arquivo mem8.v.