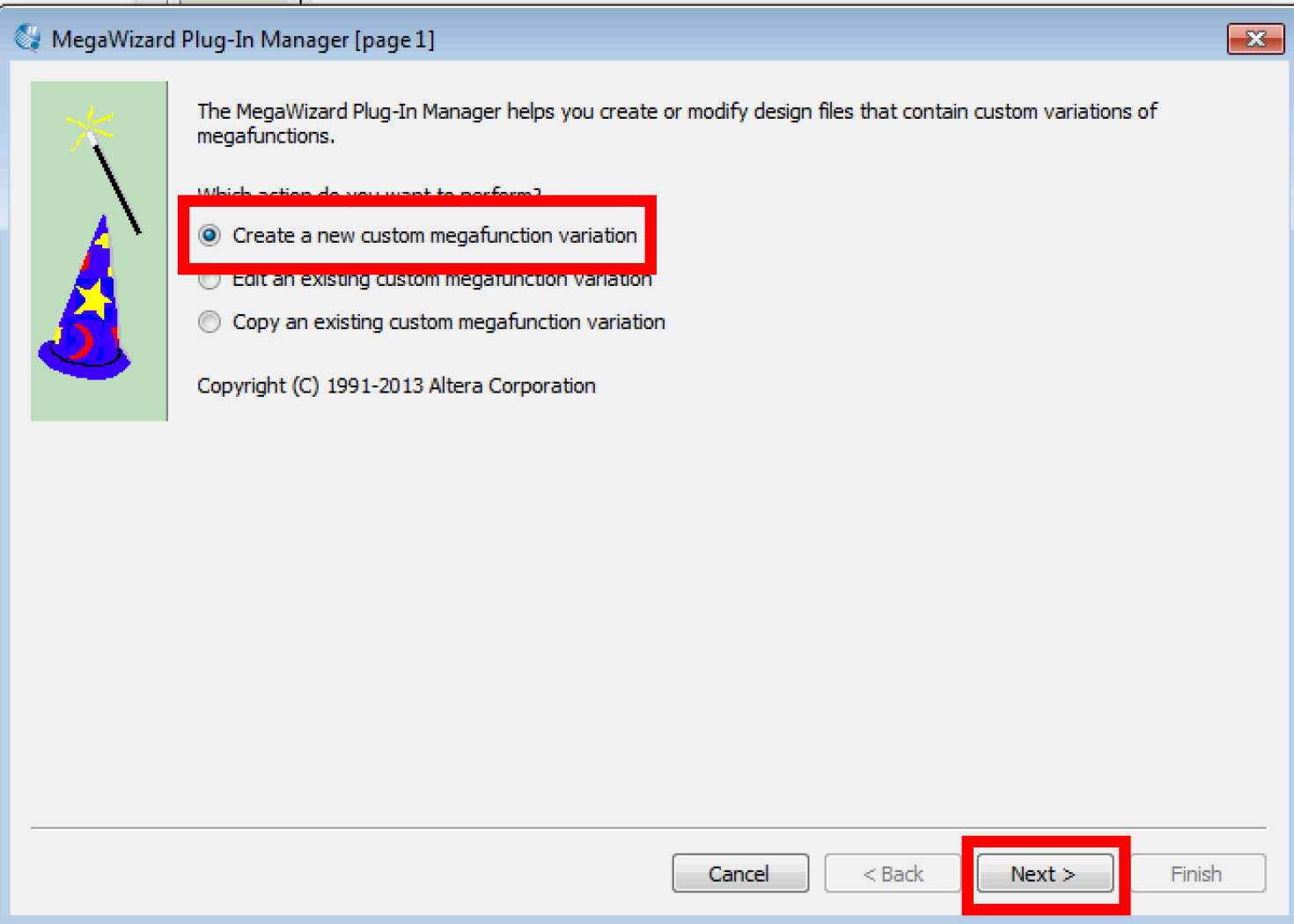
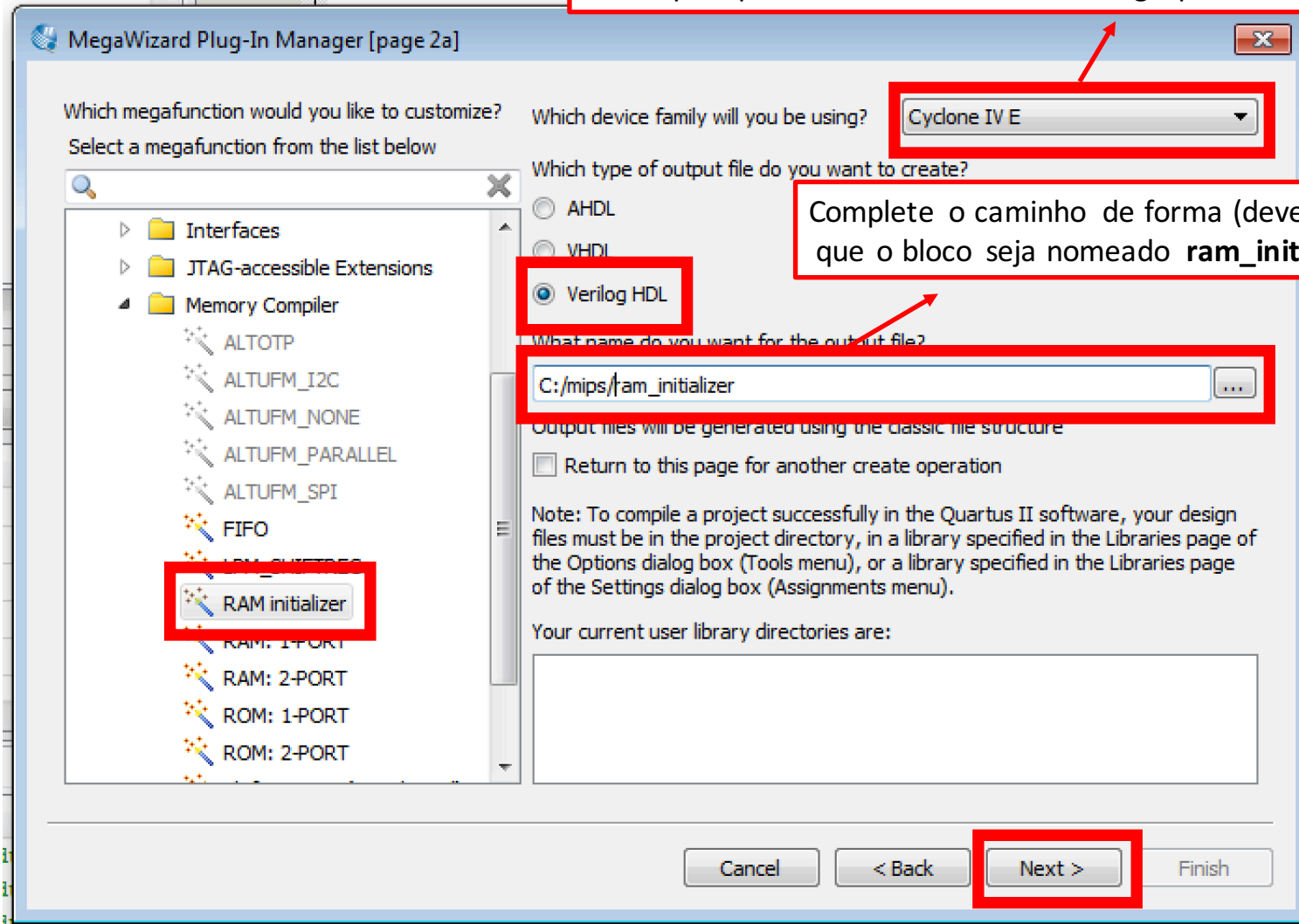


Após criar o projeto, **selecionando o modelo correto da FPGA do seu grupo**, utilize o menu “Tools” e inicie o MegaWizard




Certifique que a família da FPGA do seu grupo está selecionada corretamente



Complete o caminho de forma (deve incluir a pasta do seu projeto) que o bloco seja nomeado **ram_initializer**

MegaWizard Plug-In Manager



RAM initializer

AboutDocumentation

1Parameter Settings2Simulation Model3Summary

asas

init

clock

dataout[0]

ram_address[13..0]

ram_wren

init_busy

Initialization mode: Init data file
Init data file: inst.mif
Number of words: 16384

Resource Usage

41 lut
2 M9K
34 reg

Currently selected device family: Cyclone IV E

☒ Match project/default

RAM Initialization Mode

Which RAM initialization mode should be used?

☐ To zero

☒ From init data file

☐ From external ROM

What is the init data file?

inst.mif

☐ Use ROM data ready port

☐ Use rom_fden port

(ROM can be on/off chip)

What is the read latency?

1

ROM/RAM Information

What is the number of words?

16384

What is the data width?

32

Optional Port

☐ Create a clken port

Cancel

< Back

Next >

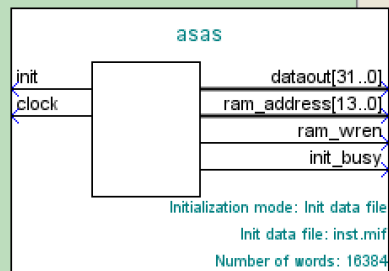
Finish



RAM initializer

[About](#)[Documentation](#)1 Parameter
Settings2 Simulation
Model

3 Summary



Simulation Libraries

To properly simulate the generated design files, the following simulation model file(s) are needed.

File	Description
altera_mf	Altera megafunction simulation library
lpm	LPM megafunction simulation library

Timing and Resource Estimation

Generates a netlist for timing and resource estimation for this megafunction. If you are synthesizing your design with a third-party synthesis tool, using a timing and resource estimation netlist can allow for better design optimization.

Not all third-party synthesis tools support this feature - check with the tool vendor for complete support information.

Note: Netlist generation can be a time-intensive process. The size of the design and the speed of your system affect the time it takes for netlist generation to complete.

☐ Generate netlist

Resource Usage

72 lut
64 M9K
34 reg

Cancel

< Back

Next >

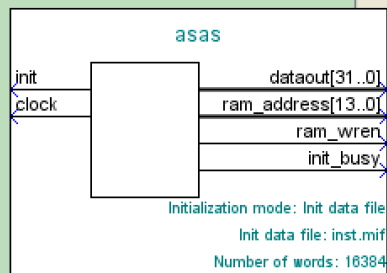
Finish



RAM initializer

[About](#) [Documentation](#)

1 Parameter Settings 2 Simulation Model 3 Summary



Turn on the files you wish to generate. A gray checkmark indicates a file that is automatically generated, and a green checkmark indicates an optional file. Click Finish to generate the selected files. The state of each checkbox is maintained in subsequent MegaWizard Plug-In Manager sessions.

The MegaWizard Plug-In Manager creates the selected files in the following directory:

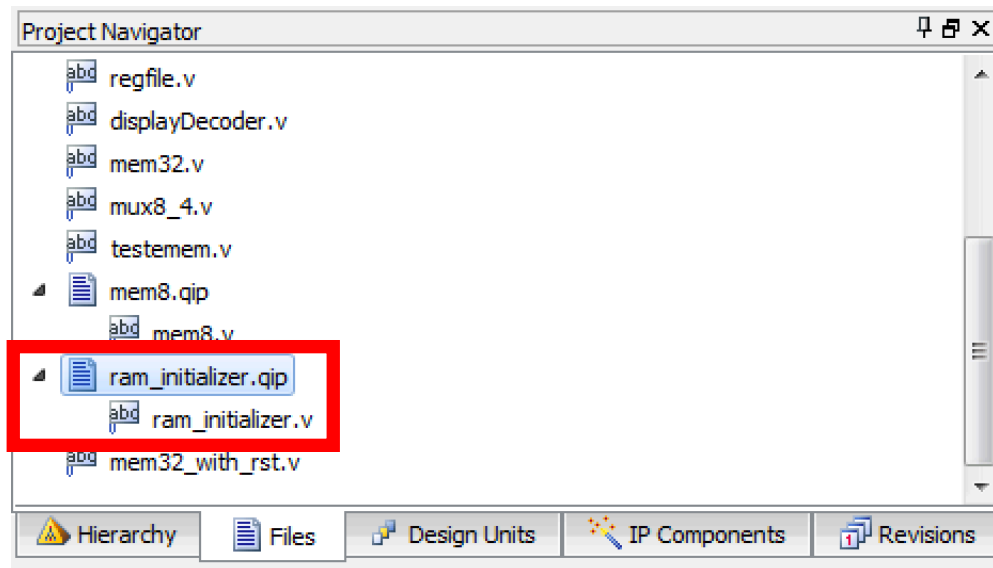
\\vmware-host\Shared Folders\Desktop\mips

File	Description
<input checked="" type="checkbox"/> asas.v	Variation file
<input checked="" type="checkbox"/> asas.qip	Quartus II IP file
<input checked="" type="checkbox"/> asas.bsf	Quartus II symbol file
<input checked="" type="checkbox"/> asas_inst.v	Instantiation template file
<input checked="" type="checkbox"/> asas_bb.v	Verilog HDL black-box file
<input checked="" type="checkbox"/> asas.inc	AHDL Include file
<input checked="" type="checkbox"/> asas.cmp	VHDL component declaration file

Resource Usage

72 lut
64 M9K
34 reg

Cancel < Back Next **Finish**



Após a finalização, verifique se o bloco `ram_initializer` foi criado corretamente no seu projeto. Caso necessite, verifique a especificação de uso no arquivo `ram_initializer.v`.

Caso deseje carregar a memória de dados com conteúdo diferente, talvez seja necessário criar outro inicializador com outro nome.