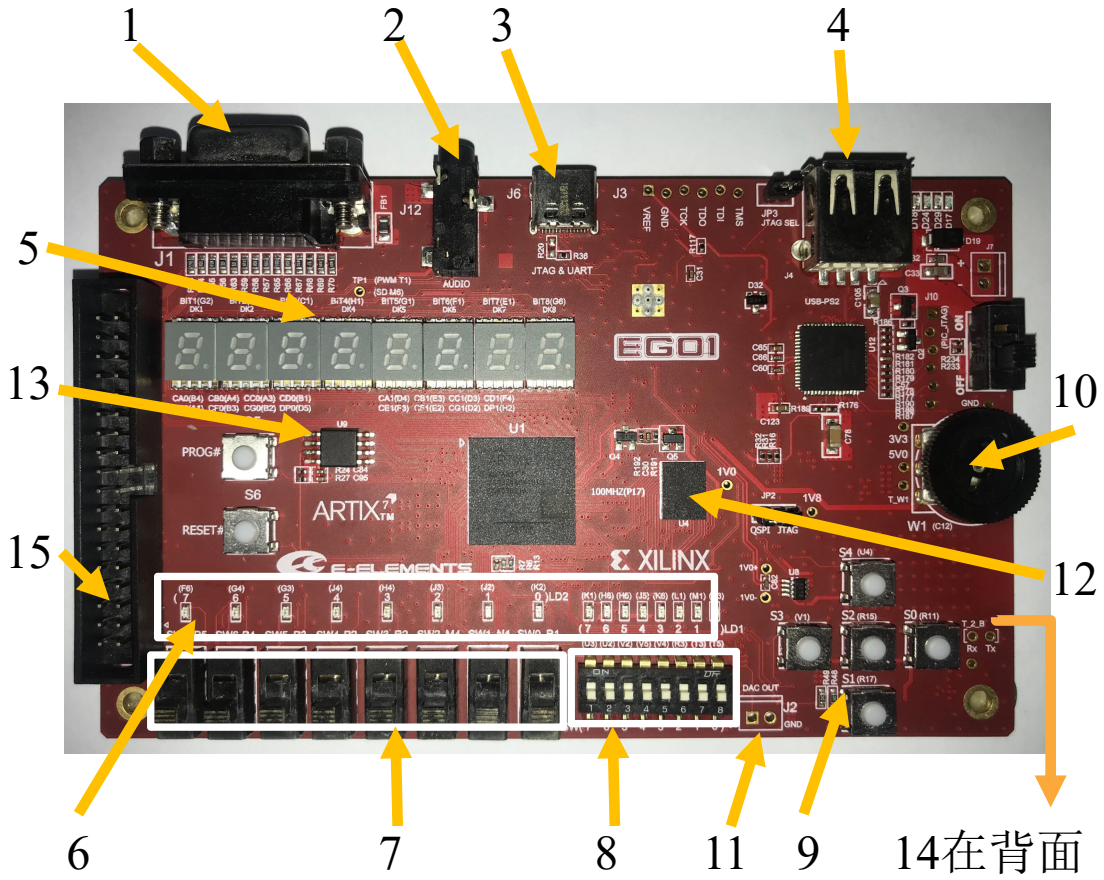
DIGITAL DESIGN

LAB SUPPLEMENTARY INTRODUCTION TO VGA DISPLAY

2022 SUMMER TERM

VGA DISPLAY



编号	描述	编号	描述
1	VGA接口	9	5个按键
2	音频接口	10	1个模拟电压输入
3	USB转Type-C接口	11	1个DAC输出接口
4	USB接口	12	SRAM存储器
5	2个4位数码管	13	SPI FLASH存储器
6	16个LED灯	14	蓝牙模块
7	8个拔码开关	15	通用扩展接口
8	1个8位DIP开关		

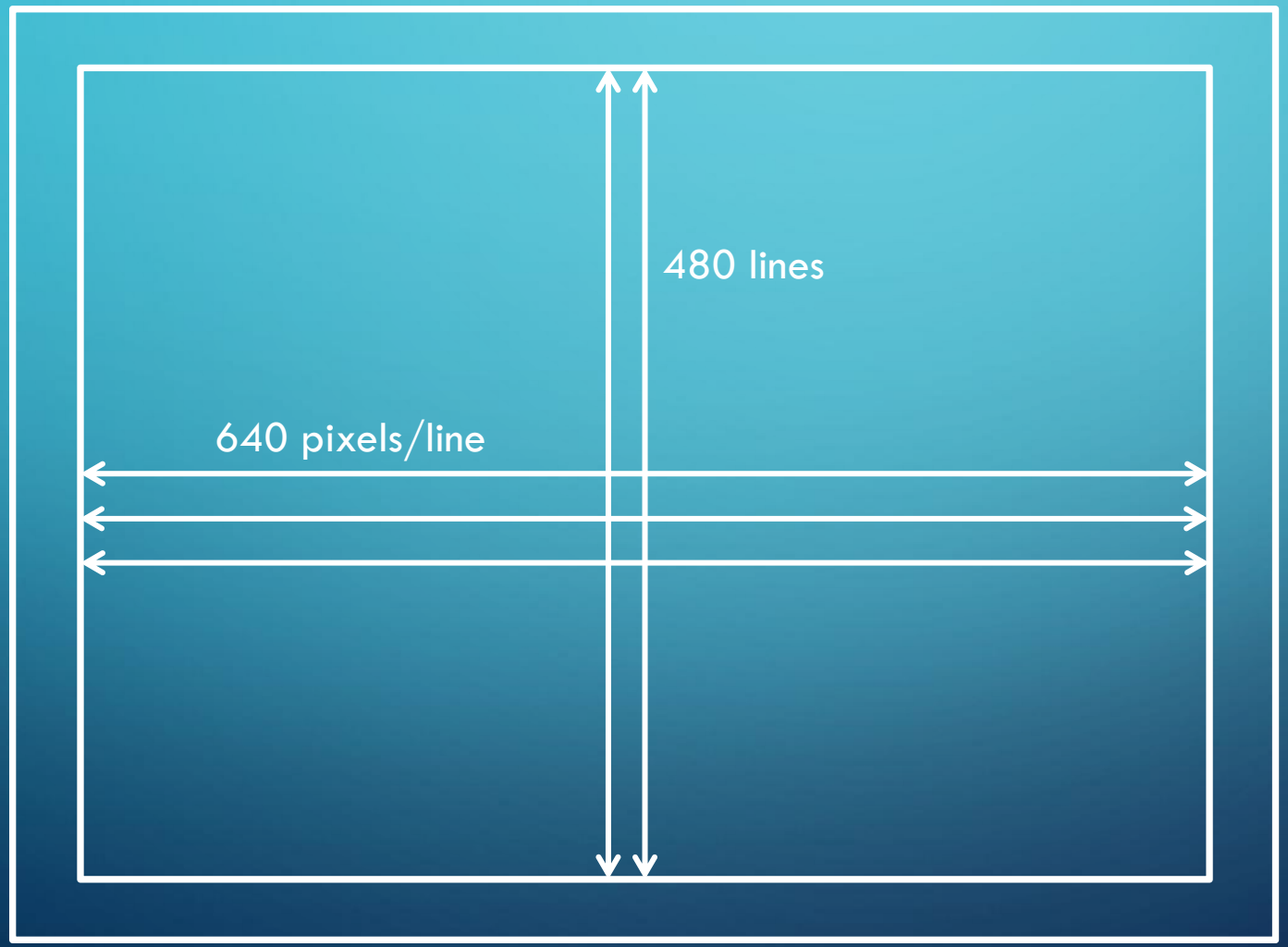
VGA DISPLAY

- Video Graphics Array
- 5 Signals
  - HSYNC, VSYNC
  - Red, Green, Blue
- 640x480@60Hz

RGB444

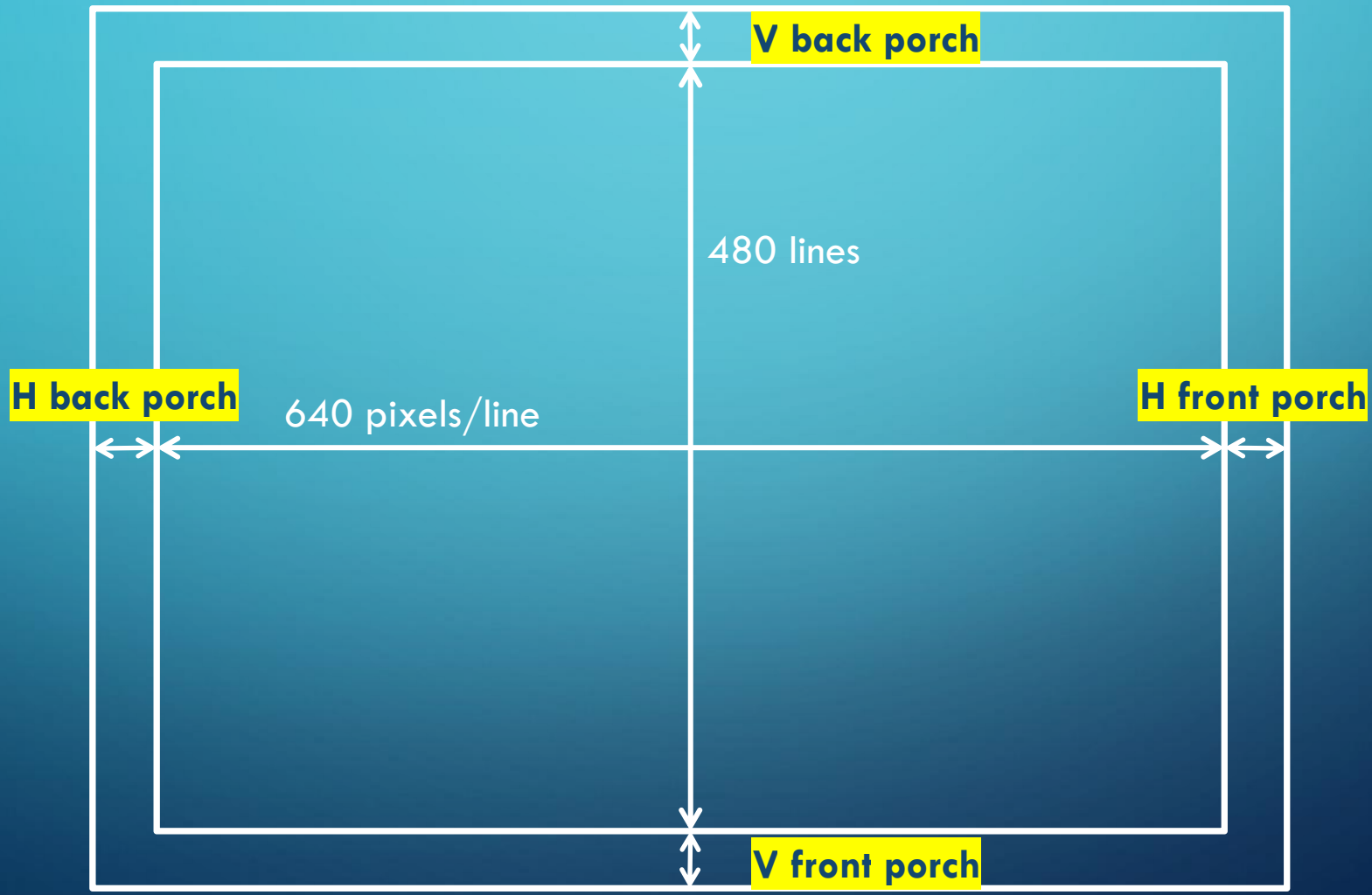
- EGO1 supports RGB444
- White: (0, 0, 0) Black: (15, 15, 15)
- Represents color in a pixel

640X480@60HZ

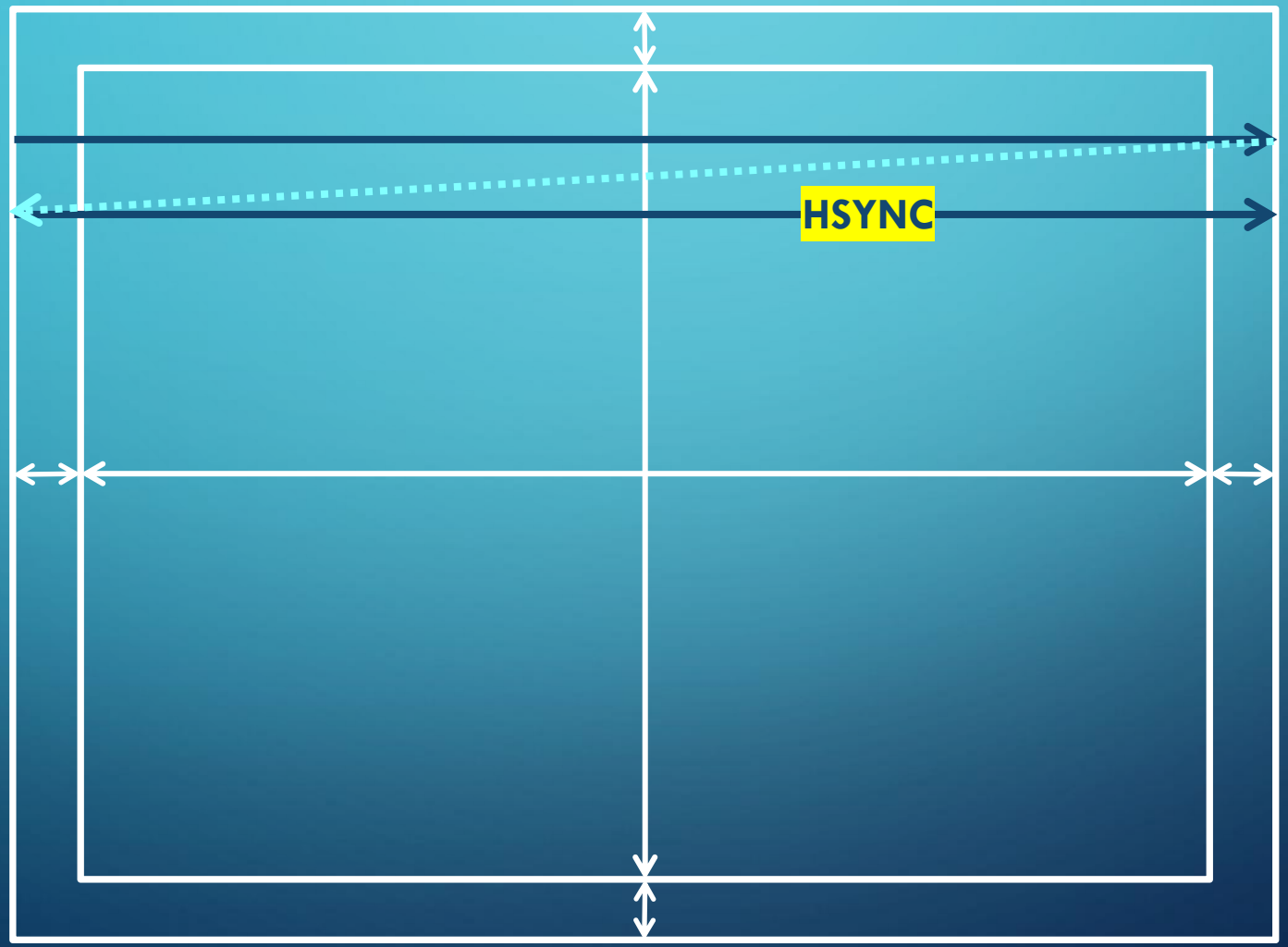


- 640: Number of rows
- 480: Number of columns
- 60HZ: The entire screen is refreshed 60 times per second

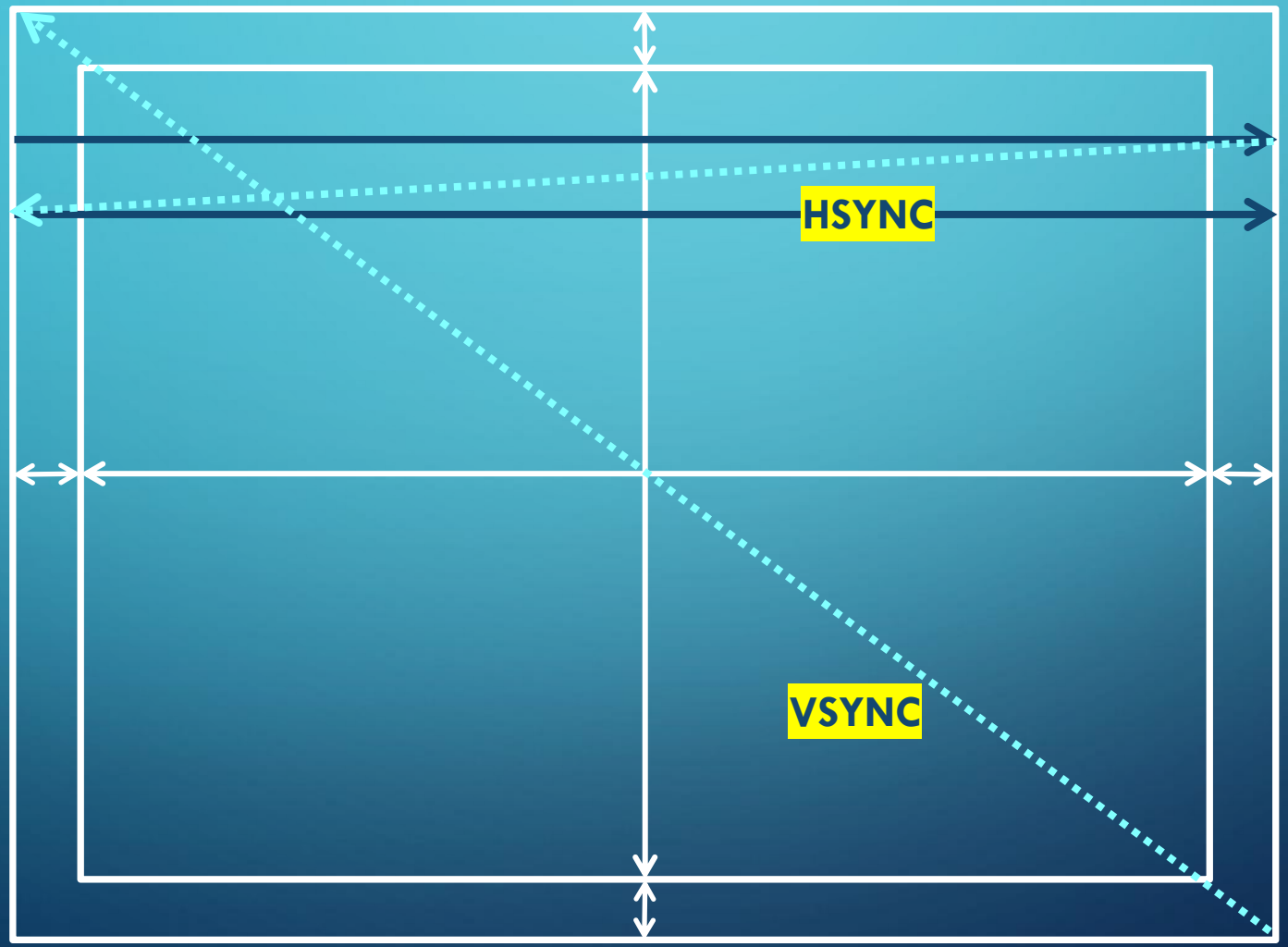
640X480@60HZ



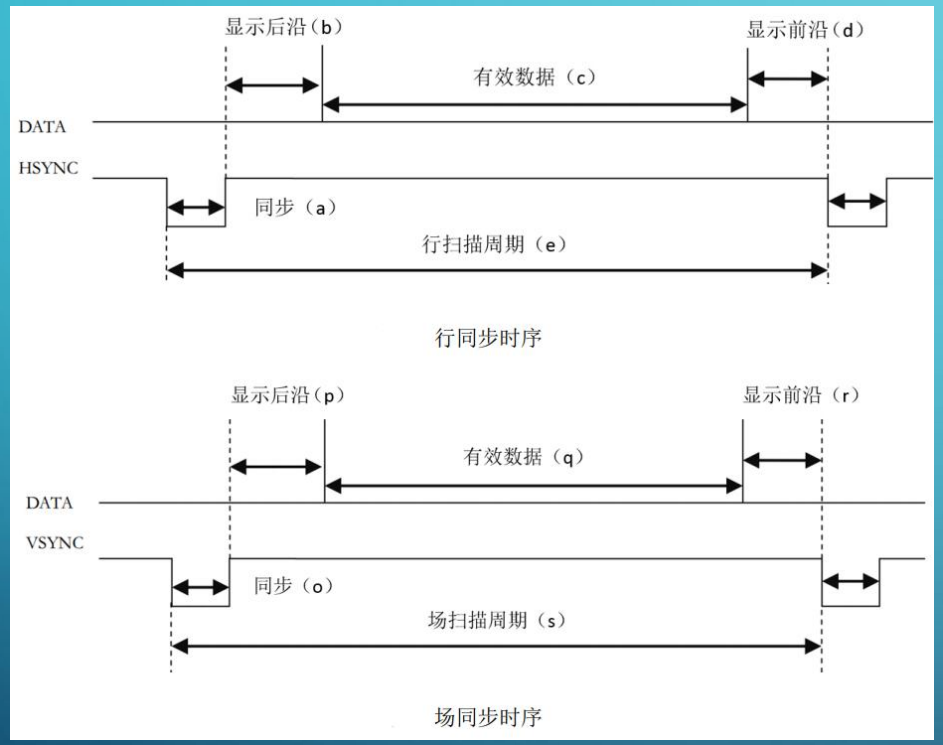
640X480@60HZ



640X480@60HZ



640X480@60HZ



1 H cycle
= HSYNC + H back porch + Data + H front porch
= 48 + 640 + 16 + 96
= 800 clock cycles

1 V cycle
= VSYNC + V back porch + Data + V front porch
= 2 + 33 + 480 + 10
= 525 H cycles

Clock frequency
= Refresh Rate * 1 V cycle
= 60 * 525 * 800
= 25.175MHz

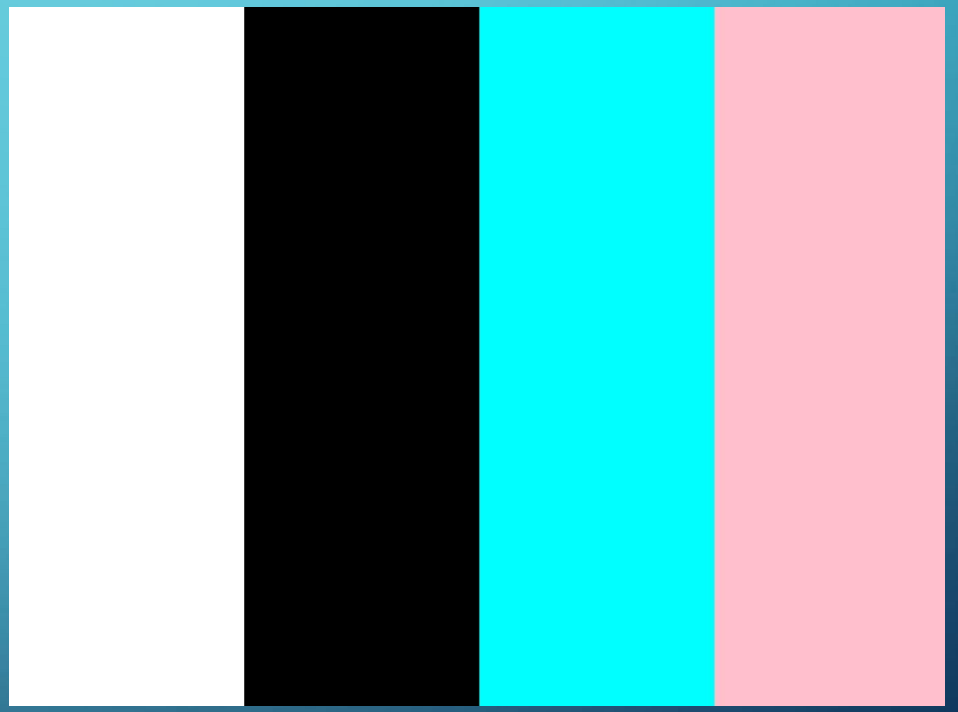
OTHER RESOLUTIONS

VGA 常用分辨率时序参数

显示模式	时钟 /MHz	行时序参数(单位：像素)					列时序参数(单位：行)				
		a	b	c	d	e	f	g	h	i	k
640x480@60Hz	25.175	96	48	640	16	800	2	33	480	10	525
800x600@60Hz	40	128	88	800	40	1056	4	23	600	1	623
1024x768@60Hz	65	136	160	1024	24	1344	6	29	768	3	806
1280x720@60Hz	74.25	40	220	1280	110	1650	5	20	720	5	750
1280x1024@60Hz	108	112	248	1280	48	1688	3	38	1024	1	1066
1920x1080@60Hz	148.5	44	148	1920	88	2200	5	36	1080	4	1125

MODULES (1)

```
module vga(
    input clk,
    input rst_n,
    output reg [3:0] red,
    output reg [3:0] green,
    output reg [3:0] blue,
    output hsync,
    output vsync
);
```



MODULES (2)

```
wire vga_clk; // 25MHz
clk_wiz_0 clk_inst(
    .clk_in1(clk),
    .clk_out1(vga_clk)
);
```

```
parameter   C_H_SYNC_PULSE      =   10'd96  ,
            C_H_BACK_PORCH      =   10'd48  ,
            C_H_ACTIVE_TIME     =   10'd640 ,
            C_H_FRONT_PORCH     =   10'd16  ,
            C_H_LINE_PERIOD     =   10'd800 ;

parameter   C_V_SYNC_PULSE      =   10'd2   ,
            C_V_BACK_PORCH      =   10'd33  ,
            C_V_ACTIVE_TIME     =   10'd480 ,
            C_V_FRONT_PORCH     =   10'd10  ,
            C_V_FRAME_PERIOD    =   10'd525 ;
```

```
assign hsync = (hc < C_H_SYNC_PULSE) ? 0 : 1;
assign vsync = (vc < C_V_SYNC_PULSE) ? 0 : 1;
```

hsync and vsync are low active

```
// horizontal counter
reg [9:0] hc;
always @(posedge clk) begin
    if(~rst_n)
        hc <= 0;
    else if(hc == C_H_LINE_PERIOD - 1)
        hc <= 0;
    else
        hc <= hc + 1;
end
```

```
// vertical counter
reg [9:0] vc;
always @(posedge clk) begin
    if(~rst_n)
        vc <= 0;
    else if (vc == C_V_FRAME_PERIOD - 1)
        vc <= 0;
    else if (hc == C_H_LINE_PERIOD - 1)
        vc <= vc + 1;
    else
        vc <= vc;
end
```

MODULES (3)

```
// 1 indicates inside active pixel range
wire active = (hc >= (C_H_SYNC_PULSE + C_H_BACK_PORCH)) &&
              (hc < (C_H_SYNC_PULSE + C_H_BACK_PORCH + C_H_ACTIVE_TIME)) &&
              (vc >= (C_V_SYNC_PULSE + C_V_BACK_PORCH)) &&
              (vc < (C_V_SYNC_PULSE + C_V_BACK_PORCH + C_V_ACTIVE_TIME)) ? 1 : 0;
```

```
always @(*) begin
    if(!rst_n) begin
        red <= 0;
        green <= 0;
        blue <= 0;
    end
    else if(active) begin
        // White
        if (hc < 160)                    {red, green, blue} = 12'hfff;
        // Black
        else if (hc >= 160 && hc < 320) {red, green, blue} = 12'h000;
        // Cyan
        else if (hc >= 320 && hc < 480) {red, green, blue} = 12'h0ff;
        // Pink
        else                             {red, green, blue} = 12'hfcc;
    end
end
```

CONSTRAINTS

名称	原理图标号	FPGA IO PIN
RED	VGA_R0	F5
	VGA_R1	C6
	VGA_R2	C5
	VGA_R3	B7
GREEN	VGA_G0	B6
	VGA_G1	A6
	VGA_G2	A5
	VGA_G3	D8
BLUE	VGA_B0	C7
	VGA_B1	E6
	VGA_B2	E5
	VGA_B3	E7
H-SYNC	VGA_HSYNC	D7
V-SYNC	VGA_VSYNC	C4