# The 'fishbone' cell library

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## 1 About this document

This document describes the images and libraries supplied with the OCEAN system. The 'image' is the basic pattern on a semi-custom chip. We distribute three types of images:

*fishbone* A gate-isolation image in a 1.6$\mu$ process with two layers of metal.

*octagon* A remarkable octagonal image in an imaginary 0.8$\mu$ process with three layers of metal interconnect.

*gatearray* An old fashioned gate-array in a single metal layer process.

At Delft university we can only process the fishbone image. Therefore most of this document and the other manuals deal with this image. The other images are supplied mainly to demonstrate the features of the placer and the router in the OCEAN system. Therefore they have a small cell library and the SPICE and SLS simulations will not give realistic results.

In any case. the librar The library is quite small, since it doesn't contain the intricate combinatorial logic cells. This was done deliberately to keep it simple for the users. Moreover, on our sea-of-gates style complex combinatorial cells can be constructed quite efficiently, so there is not really a need for such cells in the library.

of the libary This document describes the 'fishbone' Sea-of-Gates library which is used at Delft university of technology, in the release of january 1993. The cells are in the library called 'oplib1_93'. The library contains 12 digital cells and

5 analog cells. The library is quite small, since it doesn't contain the intricate combinatorial logic cells. This was done deliberately to keep it simple for the users. Moreover, on our sea-of-gates style complex combinatorial cells can be constructed quite efficiently, so there is not really a need for such cells in the library.

## 2 Additional information and related documents

This is a library description. To get information about the design tools which use these library cells, we refer to the following documents:

- *The Seafood Menu for Layout: Seadali, Trout, Madonna and more*
  This is the reference manual of the OCEAN layout tools for Sea-of-Gates. It is available in the ocean distribution or from the authors.
- *A tutorial introduction to the* OCEAN *tools*
  Contains a short guided tour along the tools of the design system. We think that this is the best way to get started with the system. Available in the ocean distribution or from the authors.
- *The NELSIS IC design system manuals*
  Especially interesting are the manuals on *simeye*, *sls* and *space*. Available via the authors.
- On-line documentation: icdman
  Just type 'icdman simeye' to get the tool description of *simeye*. This works similarly for any other nelsis tool. To get on-line help on the ocean tools, type 'trout -h' (or 'madonna -h' to get brief information.
- *Studentenhandleiding Ontwerppracticum*
  This is the elaborate student's manual (250 pages) for the second year chip design course at Delft universty of technology. Unifortunately its in Dutch. It contains all information the students need. Available from the Diktatenverkoop electrical engineering, or via the authors.

Finally a special word to you nasty American lawyers which might read this (healthy people: skip this paragraph): We, some humble employees of Delft University of Technology, and Delft University of Technology do not give warranties of any kind, either express or implied, as to any matter whatsoever, including but not limited to implied warranties of merchantability or fitness for any particular purpose or that the use of this library will not infringe any patent or copyright.

# 3 Information of each library cell

The names of the digital cells were chosen using the convention which was used by Philips for its gate-array packages. The first three characters describe the function of the cell. Sometimes the number of inputs is included in the names: 'na210' is a 2-input nand, while 'na310' is a 3-input nand. The last 2 digits describe the fan-out of the output. But sometimes I don't understand this convention myself.

The description of each cell consists of:

- Function
- Terminal connections
- IEC symbol
- Truth table
- Parameters to determine the delay
- Equivalent chip area

The parameters for the circuit delay consist of three parts:

| | |
|---|---|
| $T_{PLH}$ en $T_{PHL}$ | the fixed delay times of the cell. |
| $\Delta T_{PLH}$ en $\Delta T_{PHL}$ | The delay coefficients with a capacitative load. |
| $C_{in}$ | The input capacitance. |

The delay times and delay coefficients are specified for the rising (LH) as well as the falling (HL) edge of the output signal. The total delay can be calculated using the formula:

$$T_{P_{tot}} = T_P + \Delta T_P.C_{load}$$

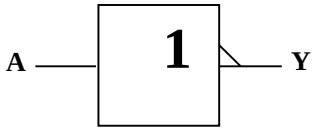
in which $C_{load}$ is the load capacitance. This load capacitance is the sum of the input capacitances of the cells which are driven plus the capacity of the interconnection wires. The unit of chip area is defined as the smallest piece of the fishbone image, which consists of one nmos and one pmos transistor.

# 4 iv110

Function: Inverter

Terminals: (A, Y, vss, vdd)

IEC-symbol:




Function table:

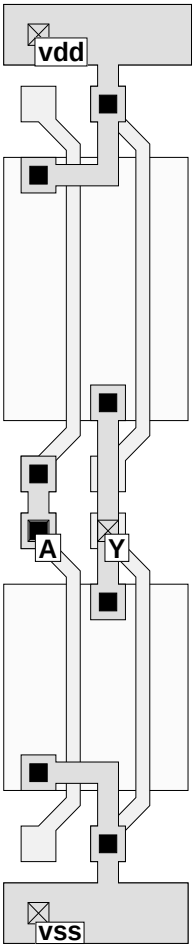
| A | Y |
|---|---|
| L | H |
| H | L |

Propagation and load dependent delays:

| Parameter | From | To | Typ | Unit |
|---|---|---|---|---|
| $T_{PLH}$ | A | Y | 0.4 | ns |
| $T_{PHL}$ | A | Y | 0.3 | ns |
| $\Delta T_{PLH}$ | A | Y | 2.2 | ns/pF |
| $\Delta T_{PHL}$ | A | Y | 2.0 | ns/pF |
| $C_{in}$ | A | vss | 0.12 | pF |

Equivalent chip area: 2

layout:

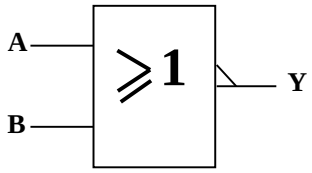


## 5 no210

Function: 2-input nor

Terminals: (A, B, Y, vss, vdd)

IEC-symbol:




Function table:

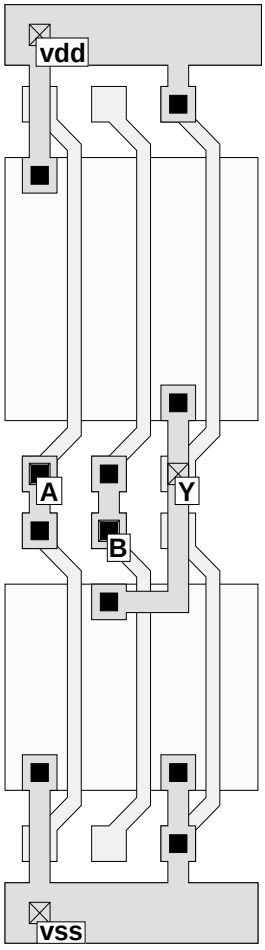
| A | B | Y |
|---|---|---|
| L | L | H |
| - | H | L |
| H | - | L |

Propagation and load dependent delays:

| Parameter | From | To | Typ | Unit |
|---|---|---|---|---|
| $T_{PLH}$ | A | Y | 0.7 | ns |
| $T_{PHL}$ | A | Y | 0.3 | ns |
| $T_{PLH}$ | B | Y | 0.6 | ns |
| $T_{PHL}$ | B | Y | 0.2 | ns |
| $\Delta T_{PLH}$ | any | Y | 7.0 | ns/pF |
| $\Delta T_{PHL}$ | any | Y | 5.0 | ns/pF |
| $C_{in}$ | any | vss | 0.12 | pF |

Equivalent chip area: 3

layout:

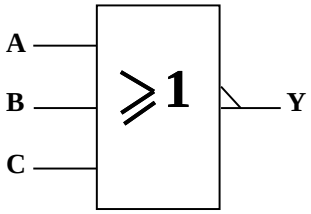


## 6 no310

Function: 3-input nor

Terminals: (A, B, C, Y, vss, vdd)

IEC-symbol:




Function table:

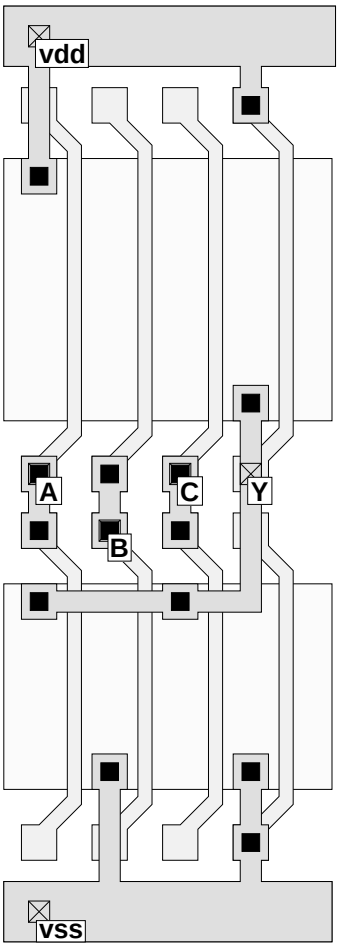
| A | B | C | Y |
|---|---|---|---|
| L | L | L | H |
| - | - | H | L |
| - | H | - | L |
| H | - | - | L |

Propagation and load dependent delays:

| Parameter | From | To | Typ | Unit |
|---|---|---|---|---|
| $T_{PLH}$ | A | Y | 1.4 | ns |
| $T_{PHL}$ | A | Y | 0.5 | ns |
| $T_{PLH}$ | B | Y | 1.3 | ns |
| $T_{PHL}$ | B | Y | 0.4 | ns |
| $T_{PLH}$ | C | Y | 1.1 | ns |
| $T_{PHL}$ | C | Y | 0.3 | ns |
| $\Delta T_{PLH}$ | any | Y | 5.0 | ns/pF |
| $\Delta T_{PHL}$ | any | Y | 10.0 | ns/pF |
| $C_{in}$ | any | vss | 0.12 | pF |

Equivalent chip area: 4

layout:

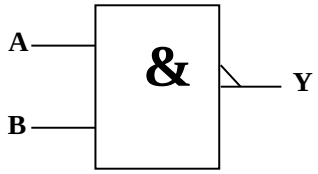


# 7 na210

Function: 2-input nand

Terminals: (A, B, Y, vss, vdd)

IEC-symbol:




Function table:

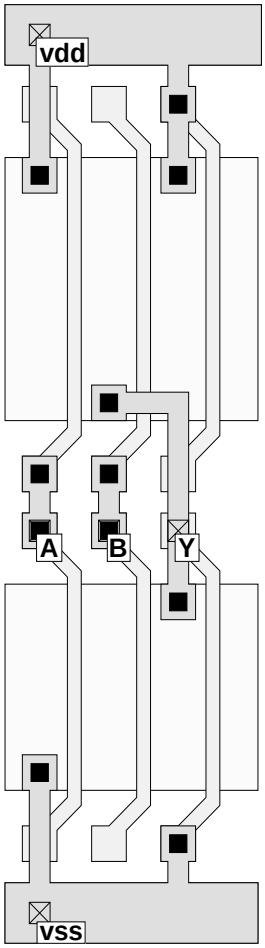
| A | B | Y |
|---|---|---|
| - | L | H |
| L | - | H |
| H | H | L |

Propagation and load dependent delays:

| Parameter | From | To | Typ | Unit |
|---|---|---|---|---|
| $T_{PLH}$ | A | Y | 0.3 | ns |
| $T_{PHL}$ | A | Y | 0.4 | ns |
| $T_{PLH}$ | B | Y | 0.3 | ns |
| $T_{PHL}$ | B | Y | 0.4 | ns |
| $\Delta T_{PLH}$ | any | Y | 4.0 | ns/pF |
| $\Delta T_{PHL}$ | any | Y | 5.0 | ns/pF |
| $C_{in}$ | any | vss | 0.12 | pF |

Equivalent chip area: 3

layout:

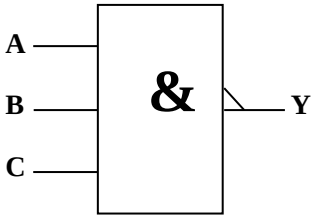


## 8 na310

Function: 3-input nand

Terminals: (A, B, C, Y, vss, vdd)

IEC-symbol:




Function table:

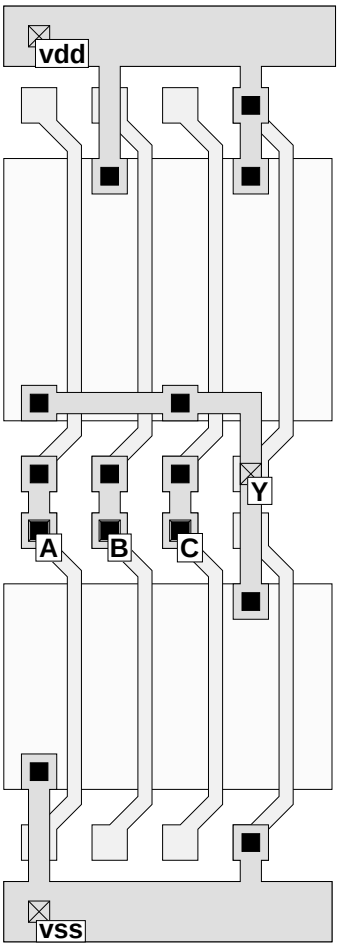
| A | B | C | Y |
|---|---|---|---|
| - | - | L | H |
| - | L | - | H |
| L | - | - | H |
| H | H | H | L |

Propagation and load dependent delays:

| Parameter | From | To | Typ | Unit |
|---|---|---|---|---|
| $T_{PLH}$ | A | Y | 0.6 | ns |
| $T_{PHL}$ | A | Y | 1.2 | ns |
| $T_{PLH}$ | B | Y | 0.5 | ns |
| $T_{PHL}$ | B | Y | 1.1 | ns |
| $T_{PLH}$ | C | Y | 0.4 | ns |
| $T_{PHL}$ | C | Y | 0.9 | ns |
| $\Delta T_{PLH}$ | any | Y | 9.0 | ns/pF |
| $\Delta T_{PHL}$ | any | Y | 3.0 | ns/pF |
| $C_{in}$ | any | vss | 0.12 | pF |

Equivalent chip area: 4

layout:

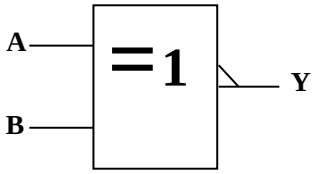


# 9 ex210

Function: Exclusive or

Terminals: (A, B, Y, vss, vdd)

IEC-symbol:




Function table:

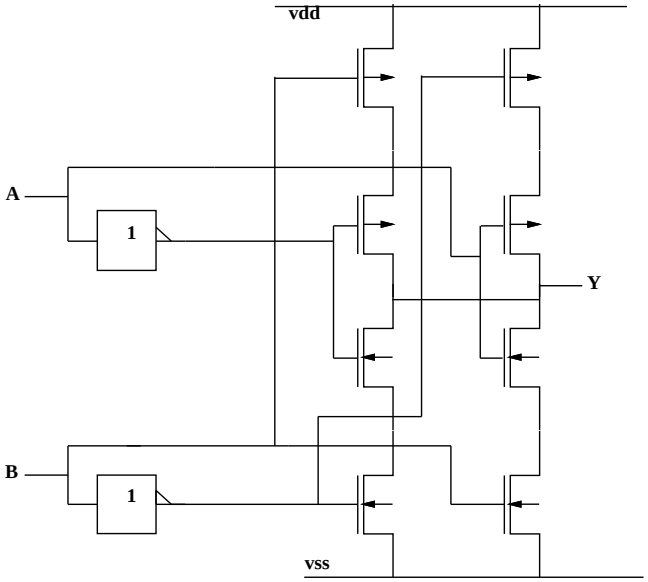
| A | B | Y |
|---|---|---|
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

Propagation and load dependent delays:

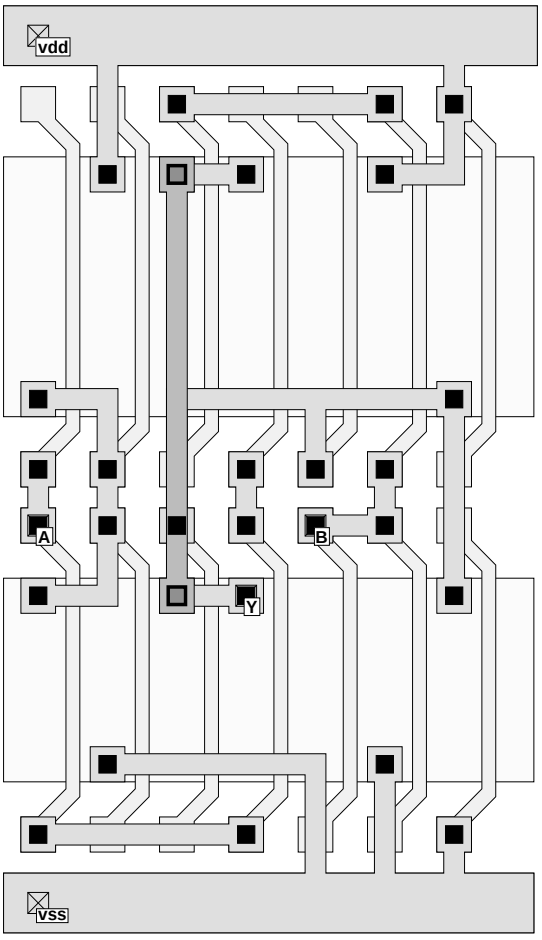
| Parameter | From | To | Typ | Unit |
|---|---|---|---|---|
| $T_{PLH}$ | A | Y | 0.7 | ns |
| $T_{PHL}$ | A | Y | 0.3 | ns |
| $T_{PLH}$ | B | Y | 0.6 | ns |
| $T_{PHL}$ | B | Y | 0.2 | ns |
| $\Delta T_{PLH}$ | any | Y | 7.0 | ns/pF |
| $\Delta T_{PHL}$ | any | Y | 5.0 | ns/pF |
| $C_{in}$ | any | vss | 0.12 | pF |

Equivalent chip area: 7

circuit:




layout:

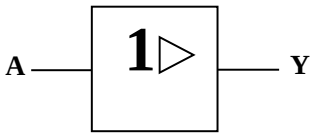


## 10 buf20

Function: Buffer (2x-drive)

Terminals: (A, Y, vss, vdd)

IEC-symbol:




Function table:

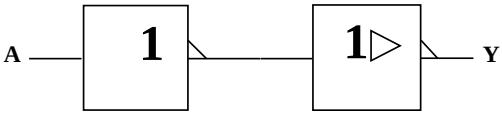
| A | Y |
|---|---|
| L | L |
| H | H |

Propagation and load dependent delays:

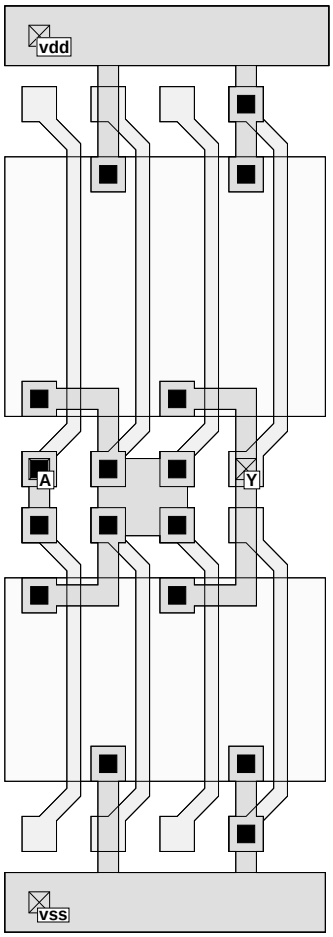
| Parameter | Van | Naar | Typ | Eenheid |
|---|---|---|---|---|
| $T_{PLH}$ | A | Y | 0.6 | ns |
| $T_{PHL}$ | A | Y | 0.7 | ns |
| $\Delta T_{PLH}$ | A | Y | 1.1 | ns/pF |
| $\Delta T_{PHL}$ | A | Y | 1.0 | ns/pF |
| $C_{in}$ | A | vss | 0.12 | pF |

Equivalent chip area: 4

circuit:




layout:

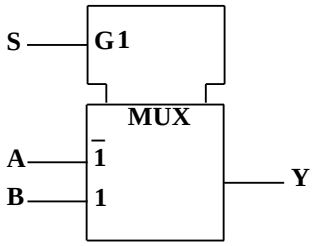


# 11 mu111

Function: 2-line-to-1-line data selector/multiplexer

Terminals: (A, B, S, Y, vss, vdd)

IEC-symbol:




Function table:

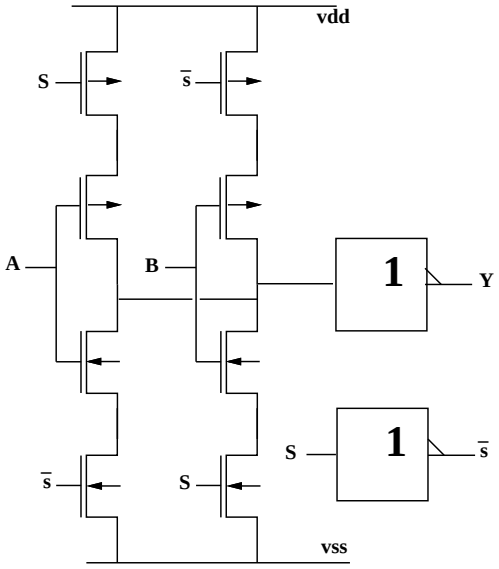
| S | A | B | Y |
|---|---|---|---|
| L | L | - | L |
| L | H | - | H |
| H | - | L | L |
| H | - | H | H |

Propagation and load dependent delays:

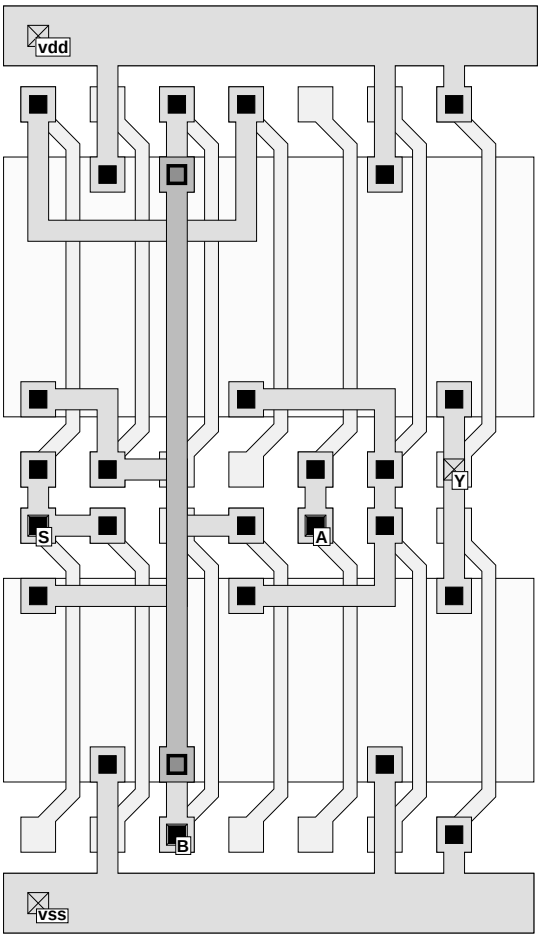
| Parameter | From | To | Typ | Unit |
|---|---|---|---|---|
| $T_{PLH}$ | A, B | Y | 0.7 | ns |
| $T_{PHL}$ | A, B | Y | 0.8 | ns |
| $T_{PLH}$ | S | Y | 1.2 | ns |
| $T_{PHL}$ | S | Y | 1.1 | ns |
| $\Delta T_{PLH}$ | alle | Y | 1.1 | ns/pF |
| $\Delta T_{PHL}$ | alle | Y | 0.9 | ns/pF |
| $C_{in}$ | A, B | vss | 0.12 | pF |
| $C_{in}$ | S | vss | 0.26 | pF |

Equivalent chip area: 7

circuit:




layout:

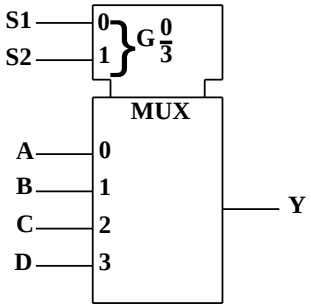


## 12 mu210

Function: 4-line-to-1-line data selector/multiplexer

Terminals: (S1, S2, A, B, C, D, Y, vss,vdd)

IEC-symbol:




Function table:

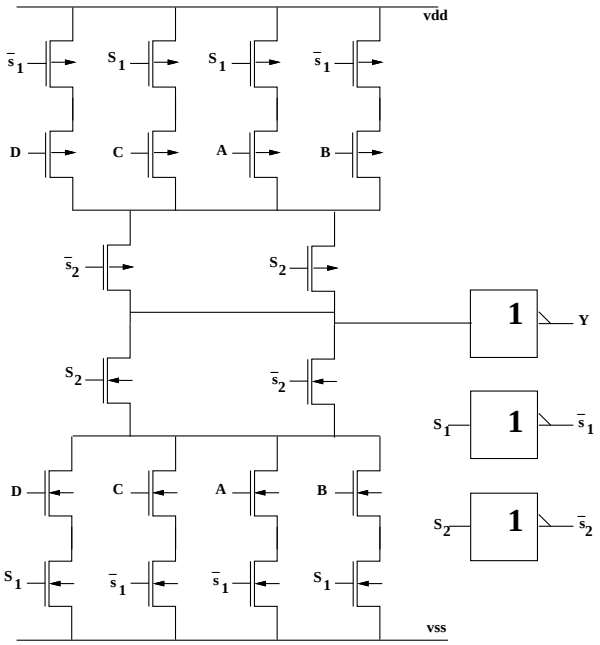
| S2 | S1 | A | B | C | D | Y |
|---|---|---|---|---|---|---|
| L | L | L | - | - | - | L |
| L | L | H | - | - | - | H |
| L | H | - | L | - | - | L |
| L | H | - | H | - | - | H |
| H | L | - | - | L | - | L |
| H | L | - | - | H | - | H |
| H | H | - | - | - | L | L |
| H | H | - | - | - | H | H |

Propagation and load dependent delays:

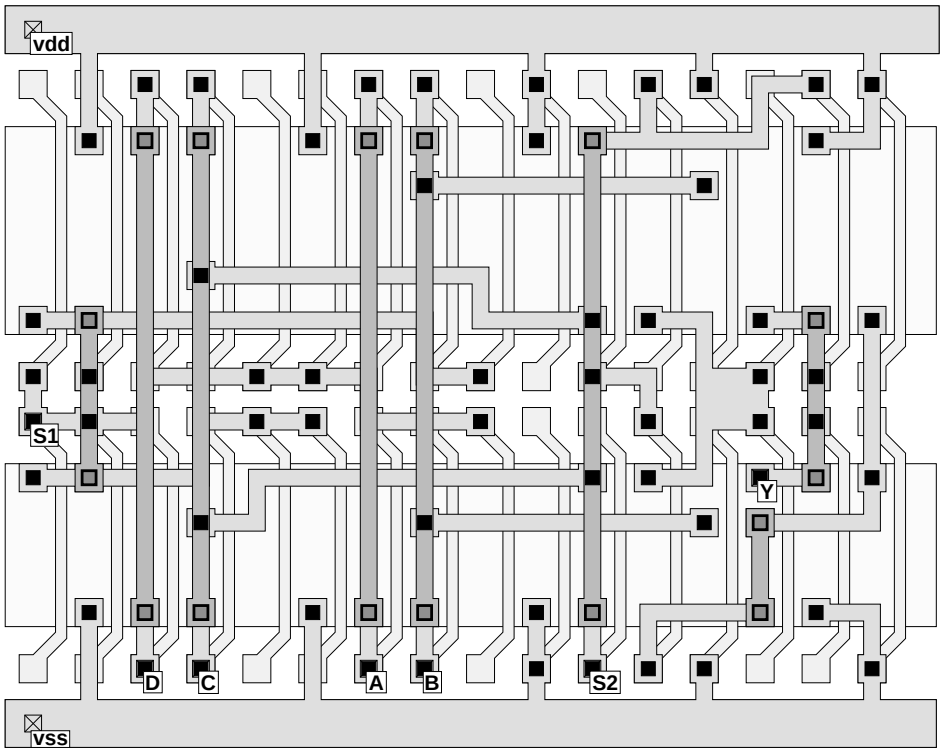
| Parameter | From | To | Typ | Unit |
|---|---|---|---|---|
| $T_{PLH}$ | A, B, C, D | Y | 2.4 | ns |
| $T_{PHL}$ | A, B, C, D | Y | 2.1 | ns |
| $T_{PLH}$ | S1 | Y | 3.0 | ns |
| $T_{PHL}$ | S1 | Y | 2.4 | ns |
| $T_{PLH}$ | S2 | Y | 2.0 | ns |
| $T_{PHL}$ | S2 | Y | 1.1 | ns |
| $\Delta T_{PLH}$ | alle | Y | 3.0 | ns/pF |
| $\Delta T_{PHL}$ | alle | Y | 7.0 | ns/pF |
| $C_{in}$ | A, B, C, D | vss | 0.12 | pF |
| $C_{in}$ | S1 | vss | 0.42 | pF |
| $C_{in}$ | S2 | vss | 0.28 | pF |

Equivalent chip area: 20

circuit:




layout:

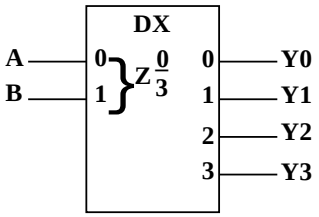


# 13 de211

Function: 2-to-4 decoder/demultiplexer

Terminals: (A, B, Y0, Y1, Y2, Y3, vss, vdd)

IEC-symbol:




Function table:

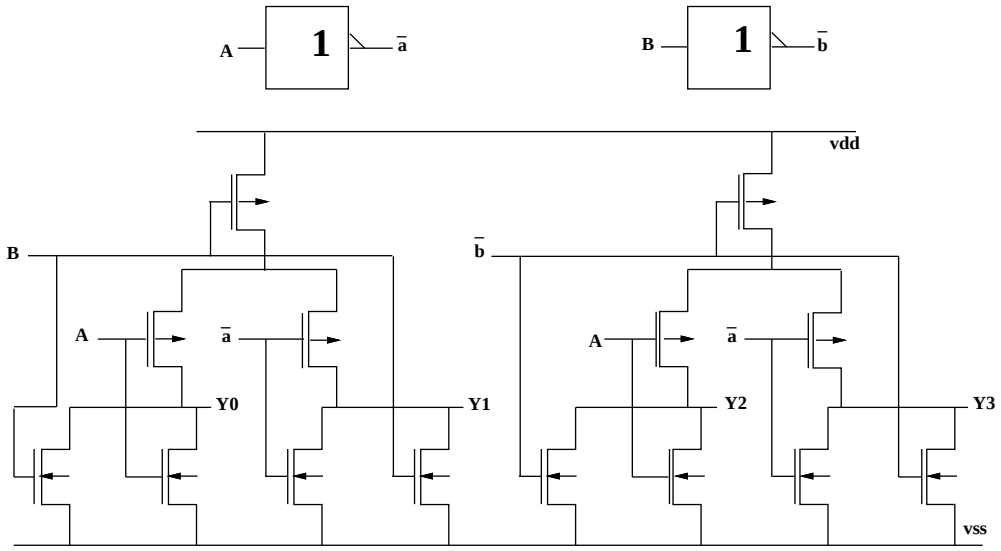
| B | A | Y0 | Y1 | Y2 | Y3 |
|---|---|---|---|---|---|
| L | L | H | L | L | L |
| L | H | L | H | L | L |
| H | L | L | L | H | L |
| H | H | L | L | L | H |

Propagation and load dependent delays:

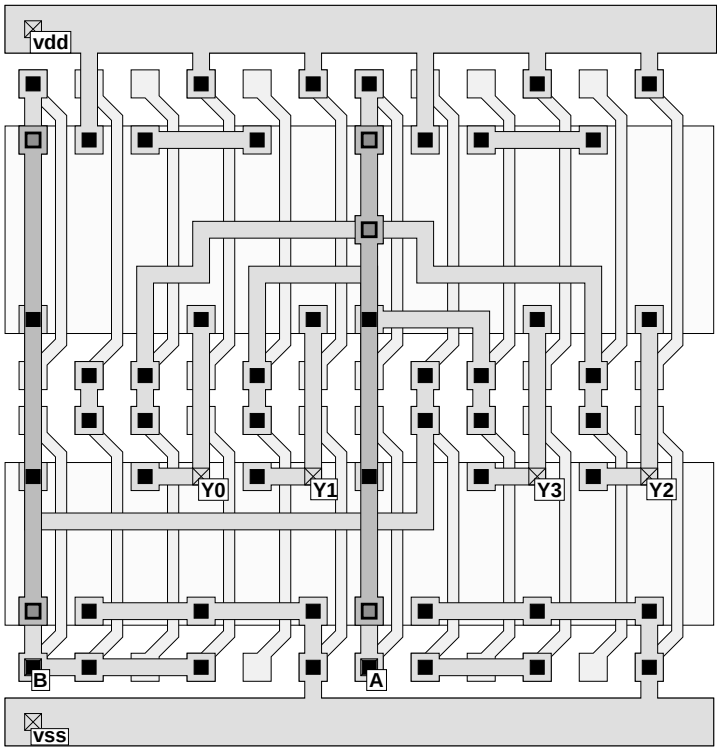
| Parameter | From | To | Typ | Unit |
|---|---|---|---|---|
| $T_{PLH}$ | A | Y0,Y2 | 0.5 | ns |
| $T_{PHL}$ | A | Y0,Y2 | 0.3 | ns |
| $T_{PLH}$ | A | Y1,Y3 | 0.8 | ns |
| $T_{PHL}$ | A | Y1,Y3 | 0.8 | ns |
| $T_{PLH}$ | B | Y0,Y1 | 0.5 | ns |
| $T_{PHL}$ | B | Y0,Y1 | 0.3 | ns |
| $T_{PLH}$ | B | Y2,Y3 | 0.8 | ns |
| $T_{PHL}$ | B | Y2,Y3 | 0.8 | ns |
| $\Delta T_{PLH}$ | any | any | 2.2 | ns/pF |
| $\Delta T_{PHL}$ | any | any | 1.0 | ns/pF |
| $C_{in}$ | A | vss | 0.38 | pF |
| $C_{in}$ | B | vss | 0.37 | pF |

Equivalent chip area: 14

circuit:




layout:

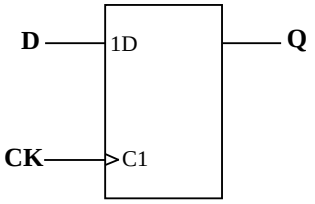


# 14 dfn10

Function: D-type positive edge triggered flipflop

Terminals: (D, CK, Q, QN, vss, vdd)

IEC-symbol:




Function table:

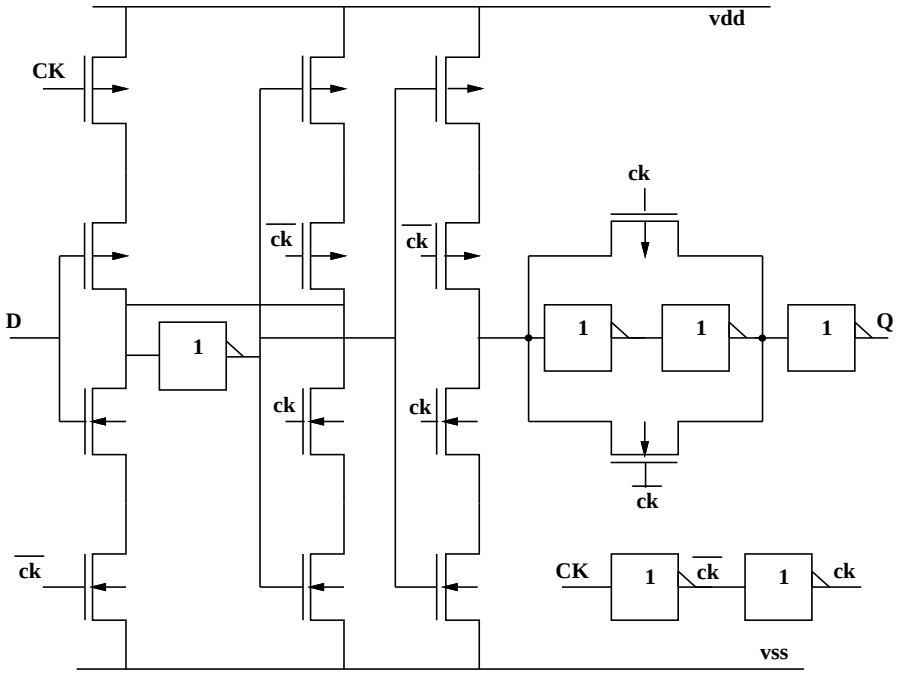
| D | CK | Q | QN |
|---|---|---|---|
| L | ↑ | L | H |
| H | ↑ | H | L |

Propagation and load dependent delays:

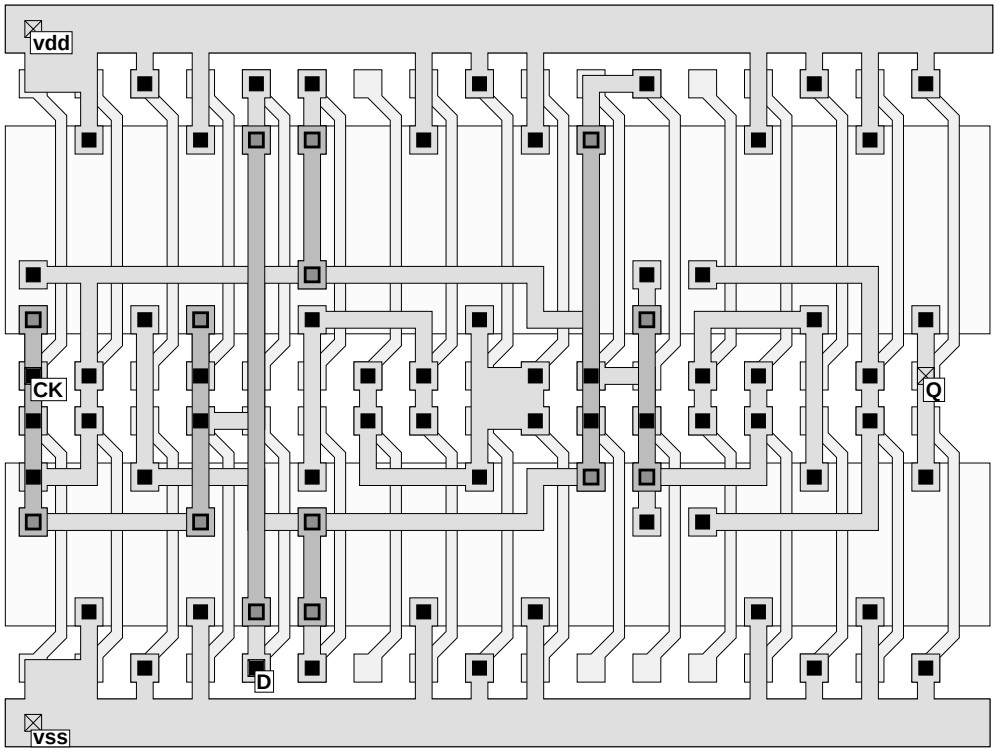
| Parameter | From | To | Typ | Unit |
|---|---|---|---|---|
| $T_{PLH}$ | CK | Q | 1.8 | ns |
| $T_{PHL}$ | CK | Q | 2.3 | ns |
| $T_{PLH}$ | CK | QN | 1.9 | ns |
| $T_{PHL}$ | CK | QN | 2.3 | ns |
| $\Delta T_{PLH}$ | CK | any | 8.0 | ns/pF |
| $\Delta T_{PHL}$ | CK | any | 7.0 | ns/pF |
| $C_{in}$ | D | vss | 0.12 | pF |
| $C_{in}$ | CK | vss | 0.43 | pF |

Equivalent chip area: 12

circuit:




layout:

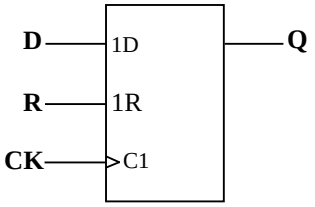


# 15 dfr11

Function: D-type positive edge triggered flipflop with synchronous reset

Terminals: (D, R, CK, Q, QN, vss, vdd)

IEC-symbol:




Function table:

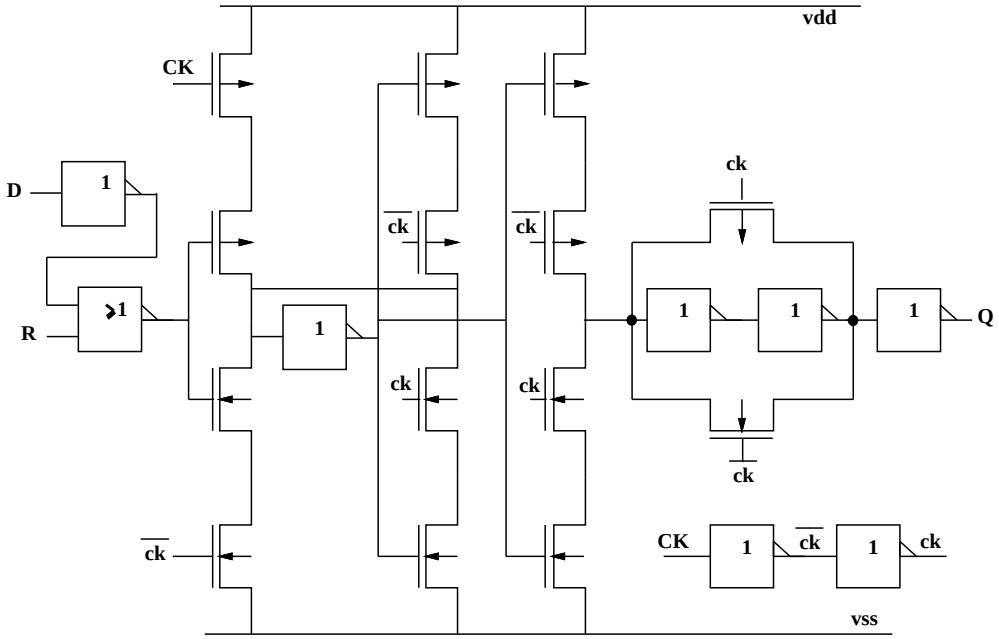
| R | D | CK | Q | QN |
|---|---|---|---|---|
| L | L | ↑ | L | H |
| L | H | ↑ | H | L |
| H | - | ↑ | L | H |

Propagation and load dependent delays:

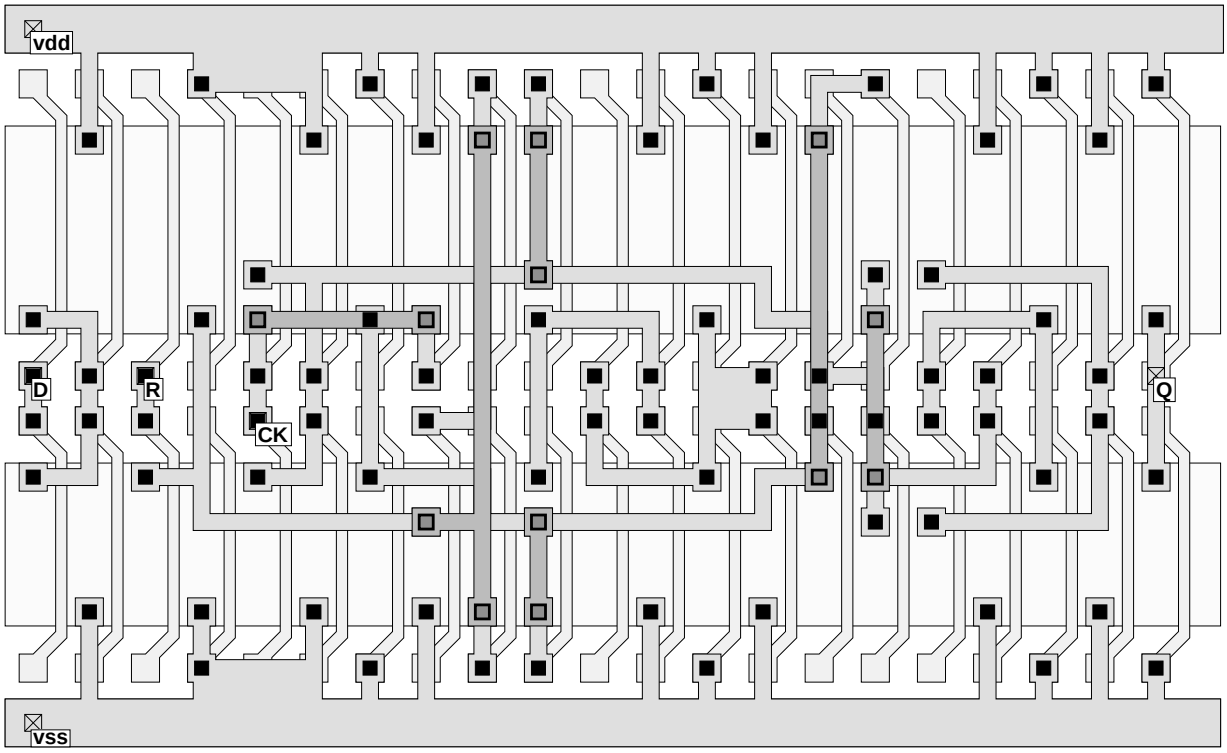
| Parameter | From | To | Typ | Unit |
|---|---|---|---|---|
| $T_{PLH}$ | CK | Q | 1.8 | ns |
| $T_{PHL}$ | CK | Q | 2.3 | ns |
| $T_{PLH}$ | CK | QN | 1.9 | ns |
| $T_{PHL}$ | CK | QN | 2.3 | ns |
| $\Delta T_{PLH}$ | CK | any | 8.0 | ns/pF |
| $\Delta T_{PHL}$ | CK | any | 7.0 | ns/pF |
| $C_{in}$ | D,R | vss | 0.12 | pF |
| $C_{in}$ | CK | vss | 0.43 | pF |

Equivalent chip area: 15

circuit:



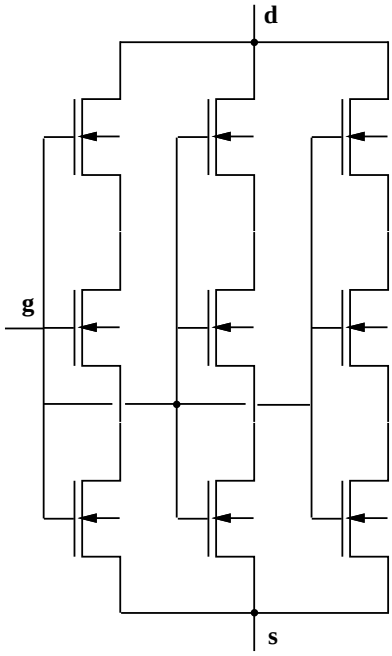

layout:



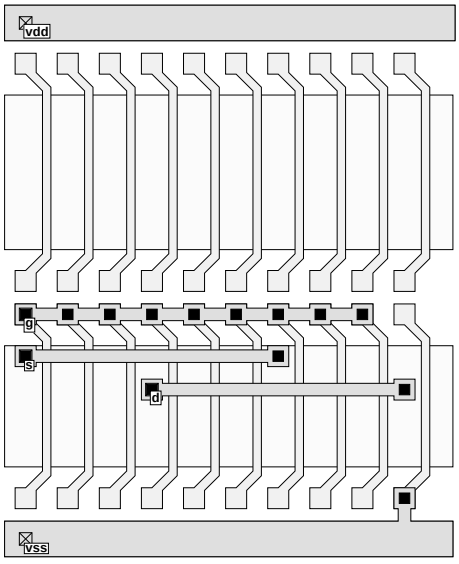
# 16 NMOS Compound transistor ln3x3

The NMOS Compoundtransistor ln3x3 consists of 9 NMOS transistors which are connected in a 3x3 matrix.

Circuit:



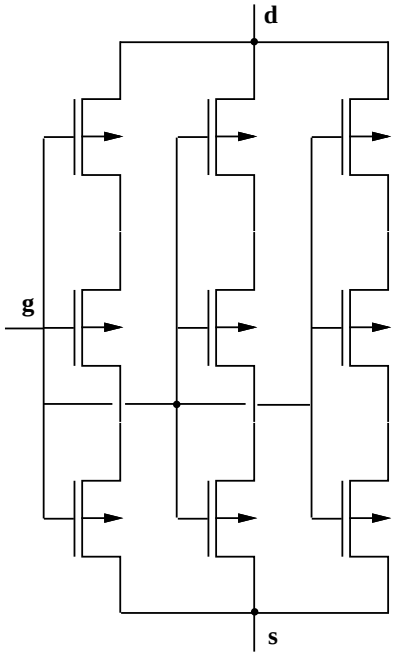

Layout:



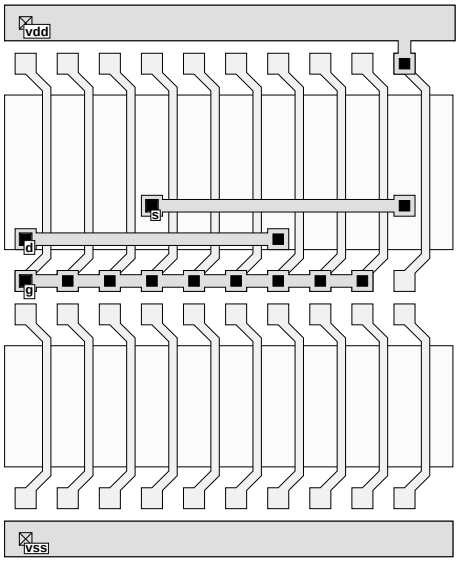
# 17 PMOS Compoundtransistor lp3x3

The PMOS Compoundtransistor lp3x3 consists of 9 PMOS transistors which are connected in a 3x3 matrix.

Circuit:



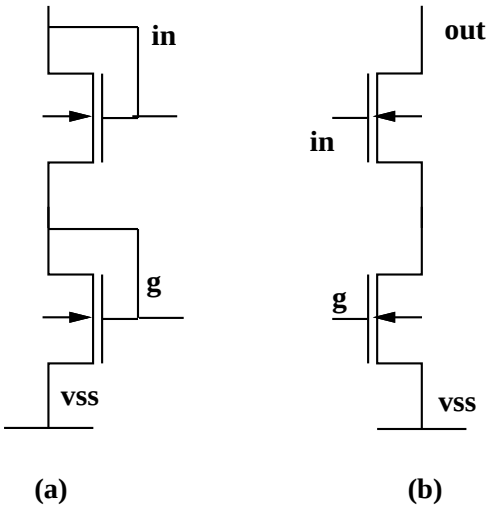

Layout:



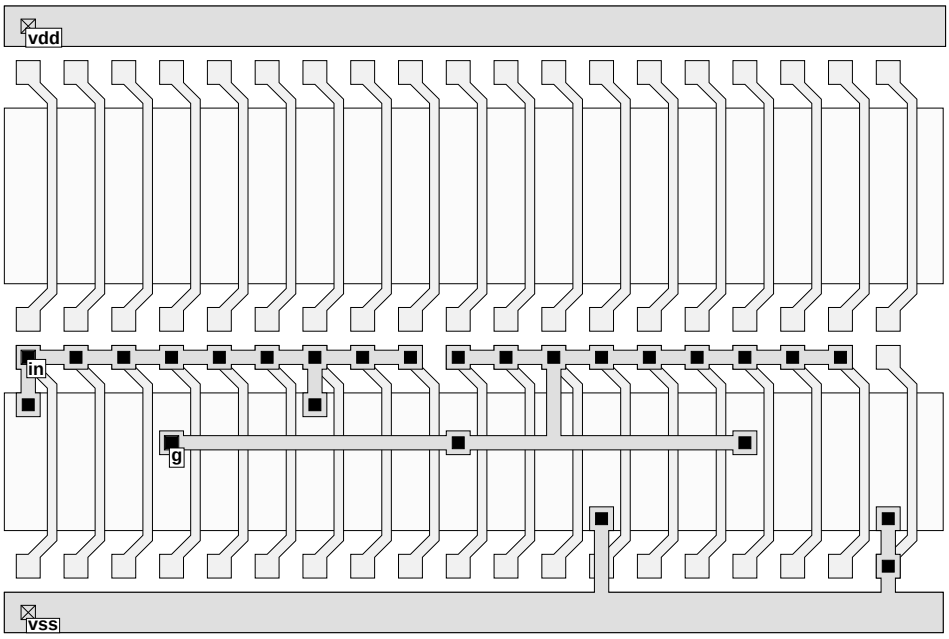
# 18 NMOS mirrors mir_nin en mir_nout

The MNOS mirrors are building blocks for a cascoded current mirror. It consists of the input mir_nin and the output mir_nout. In a mirror, both can be repeated a number of times to achive the entire circuit.

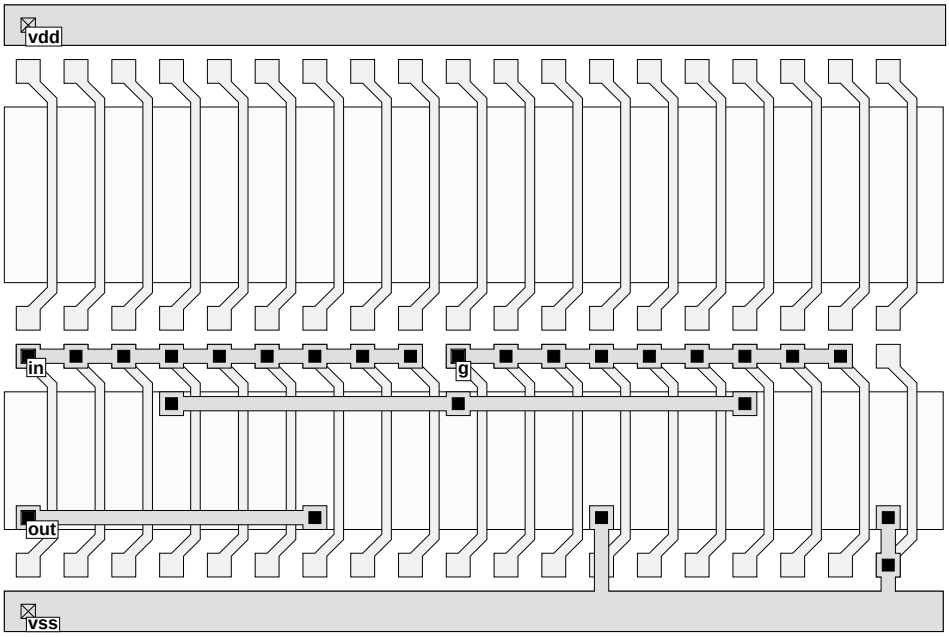
Circuit:
(a) mir_nin (b) mir_nout



Layout mir_nin:



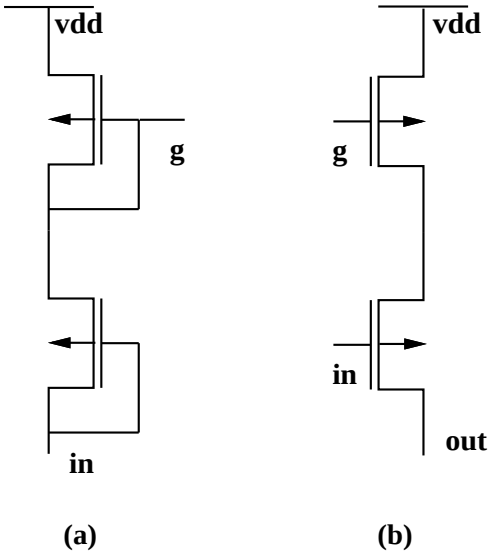

Layout mir_nout:



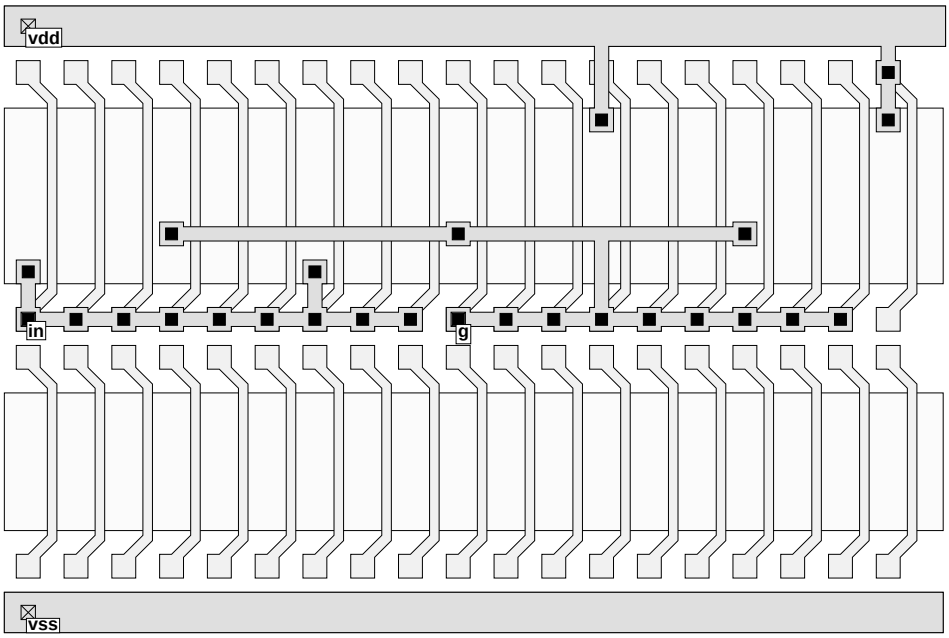
# 19 PMOS mirrors mir_pin and mir_pout

The PNOS mirrors are building blocks for a cascoded current mirror. It consists of the input mir_pin and the output mir_pout. In a mirror, both can be repeated a number of times to achive the entire circuit.

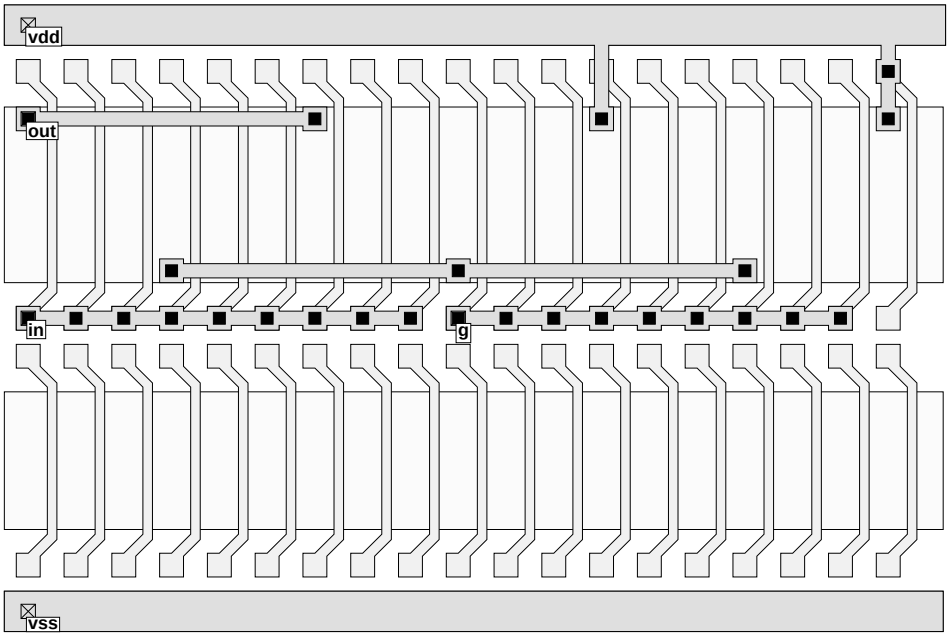
Circuit:
(a) mir_pin (b) mir_pout



Layout mir_pin:




Layout mir_pout:

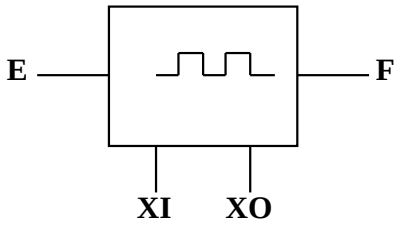


## 20 osc10

Function: Crystal oscillator with enable

Terminals: (E, F, XI, XO, vss, vdd)

Symbol:



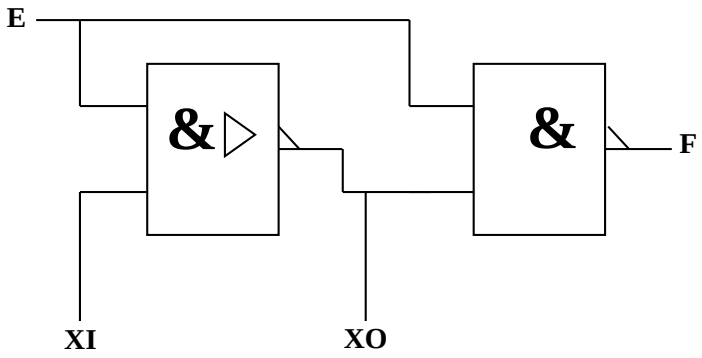

Frequency range: 1MHz to 20MHz

Equivalent chip area: 16

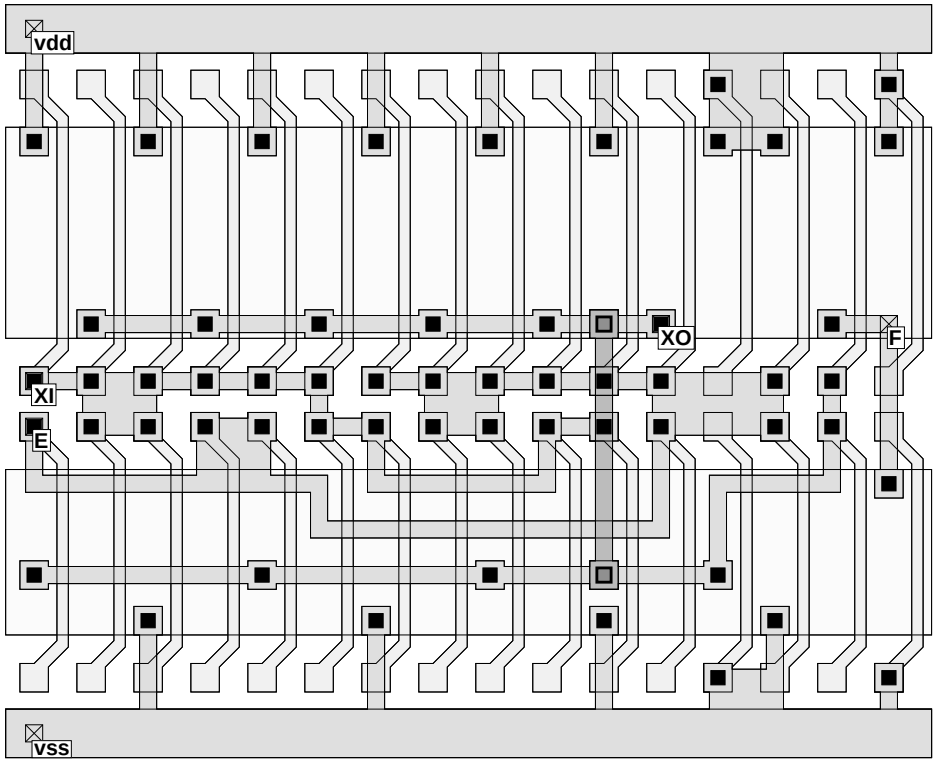
Description:

XI and XO are the connections for the crystal. XI must be buffered using and input buffer, X) should not be buffered. If E (enalble) is high, the oscillator is active, If E is low, the output F is high.

circuit:




layout:



## Contents

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