# SPACE APPLICATION NOTE ABOUT BACK ANNOTATION

*S. de Graaf*

Circuits and Systems Group
Faculty of Electrical Engineering,
Mathematics and Computer Science
Delft University of Technology
The Netherlands

Report EWI-ENS 03-11
December 11, 2003



Last revision: December 12, 2003.

## 1. Introduction

We had this week, Monday 8 December, a meeting about this topic with Nick van der Meijs and Kees-Jan van der Kolk. Some of the SPACE users (mr. Li of Intel) are interested in back annotation of substrate nodes. Thus, i shall try to explain something about the back annotation possibilities of the SPACE system.

Back annotation is used, to find elements from the cell layout back into the extracted circuit of the cell. For example the layout positions of transistor devices and terminal nodes.

For extraction with the SPACE system see the "Space User's Manual" [1] and for substrate extraction see the "Space Substrate Resistance Extraction User's Manual" [2].

See also section "Back Annotation", section 2.10 of [1].

See also the *space* back annotation options **-x** and **-t**, sections 2.10.7 - 2.10.9 of [1].

**2. Back Annotation of Nodes**

For back annotation of nodes, it is important that the nodes are not eliminated from the extracted network (circuit). A node is not eliminated, because of one of the following reasons:

1. The node is a terminal or label.
2. The node is a device pin.
3. The node is a element pin, that must be kept.
4. The node is the last node of a node group.
5. The node is a substrate terminal.

**NOTE:**
Labels are named (node) positions in the layout (see *dali*).

**NOTE:**
Devices (transistor elements) are never eliminated by *space*.

**NOTE:**
Elements can be resistors, capacitors and contacts. Are specified in the element definition (technology) file, but can be eliminated.

**NOTE:**
There are only node groups by resistance extraction. The nodes in the group are connected to each other by resistors. A node group can be eliminated to one node.

Nodes can be kept with the *keep_nodes* parameter, see section 2.8.12 of [1].

**Example:**
keep_nodes lcap_cms ecap_cms_cpg.2

Note that substrate terminals are default not eliminated (except the distributed ones).
But with parameters *elim_sub_term_node* and *elim_sub_node*, this can be changed. See also section 6 of [2].

Note that there is also a special *space* option **-%f** (fine network) to put off all node elimination.

With *space* parameter *node_pos_name*, see section 2.10.4 of [1], you can get special net names with the mask and starting (most left/bottom) net/node position.

### 3. Back Annotation of Substrate Nodes

There are two kinds of substrate nodes:

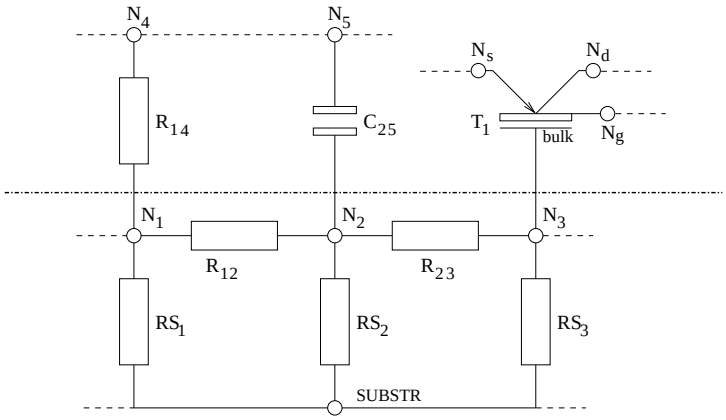
1. The general node of the substrate, named "SUBSTR".
2. The substrate terminal nodes.

   **NOTE:**
   The substrate terminal nodes are connected to "SUBSTR" by a substrate resistor. Substrate terminal nodes exist only, when substrate extraction is done.

There are two kinds of substrate terminals:

1. Substrate terminals of capacitances and transistors. These nodes make no real contact with interconnect nodes.
2. Substrate terminals of contact elements. These nodes are connected (via contact resistors) with interconnect nodes.

See the following figure for an explanation:




Nodes $N_1$, $N_2$ and $N_3$ are substrate terminals. Node $N_1$ of a substrate contact ($R_{14}$ is the contact resistor). Node $N_3$ is also the bulk pin of transistor $T_1$. Nodes $N_4$, $N_5$, $N_s$, $N_d$ and $N_g$ are nodes in the interconnect. Resistors $RS_1$, $RS_2$, $RS_3$, $R_{12}$ and $R_{23}$ are substrate resistors. There is normally also a substrate resistor between nodes $N_1$ and $N_3$.

Note that the above substrate nodes are all in different node groups. However, substrate node $N_1$ is in the same node group as node $N_4$. But this node does not get the conductor number (net attribute "cd") of that node group by output. All substrate terminal nets get "cd=0" by output. This can be used by other tools, like *xspef* and *xspf*.

**4. Examples Listing**

```
% space3d -v -E elem.t -P param.p -B sub3term
% xsls sub3term
/* Generated by: xsls 2.34 27-Sep-2000 */
/* Date: 12-Dec-03 8:28:37 GMT */
/* Path: /u/52/52/work/simon/CACD/demo/demo/sub3term/projectname */

network sub3term (terminal c, b, a)
{
    res 1.275388M (c, a);
    res 680.1685k (c, b);
    res 75.8245k (c, SUBSTR);
    res 680.1685k (a, b);
    res 75.8245k (a, SUBSTR);
    res 49.43491k (b, SUBSTR);
}

% space3d -v -E elem.t -P param.p -B -S node_pos_name sub3term
% xsls sub3term
/* Generated by: xsls 2.34 27-Sep-2000 */
/* Date: 12-Dec-03 8:29:55 GMT */
/* Path: /u/52/52/work/simon/CACD/demo/demo/sub3term/projectname */

network sub3term (terminal c, b, a)
{
    net {cmf_40_0, c};
    net {cmf_0_0, a};
    net {cmf_15_30, b};
    res 1.275388M (cmf_40_0, cmf_0_0);
    res 680.1685k (cmf_40_0, cmf_15_30);
    res 75.8245k (cmf_40_0, SUBSTR);
    res 680.1685k (cmf_0_0, cmf_15_30);
    res 75.8245k (cmf_0_0, SUBSTR);
    res 49.43491k (cmf_15_30, SUBSTR);
}

% dbcat -c sub3term
dbcat: -c: list only circuit data
=> circuit/sub3term/mc
cell:"res" inst:"_R1" attr:"v=1.275388e+06" dim:0
cell:"res" inst:"_R2" attr:"v=6.801685e+05" dim:0
cell:"res" inst:"_RS1" attr:"v=7.582450e+04" dim:0
cell:"res" inst:"_R3" attr:"v=6.801685e+05" dim:0
cell:"res" inst:"_RS2" attr:"v=7.582450e+04" dim:0
cell:"res" inst:"_RS3" attr:"v=4.943491e+04" dim:0
=> circuit/sub3term/term
term:"c" attr:"" dim:0
term:"b" attr:"" dim:0
term:"a" attr:"" dim:0
=> circuit/sub3term/net
net:"cmf_40_0" inst:"" attr:"cd=0" subnets:4
    subnet[0]:"c" inst:"" attr:""
```

```
    subnet[1]:"p" inst:"_R1" attr:""
    subnet[2]:"p" inst:"_R2" attr:""
    subnet[3]:"p" inst:"_RS1" attr:""
net:"cmf_0_0" inst:"" attr:"cd=0" subnets:4
    subnet[0]:"a" inst:"" attr:""
    subnet[1]:"p" inst:"_R3" attr:""
    subnet[2]:"n" inst:"_R1" attr:""
    subnet[3]:"p" inst:"_RS2" attr:""
net:"cmf_15_30" inst:"" attr:"cd=0" subnets:4
    subnet[0]:"b" inst:"" attr:""
    subnet[1]:"n" inst:"_R3" attr:""
    subnet[2]:"n" inst:"_R2" attr:""
    subnet[3]:"p" inst:"_RS3" attr:""
net:"SUBSTR" inst:"" attr:"cd=0" subnets:3
    subnet[0]:"n" inst:"_RS1" attr:""
    subnet[1]:"n" inst:"_RS2" attr:""
    subnet[2]:"n" inst:"_RS3" attr:""

% space3d -v -E elem.t -P param.p -B -x sub3term
% dbcat -c sub3term
=> circuit/sub3term/mc
cell:"res" inst:"_R1" attr:"v=1.275388e+06" dim:0
cell:"res" inst:"_R2" attr:"v=6.801685e+05" dim:0
cell:"res" inst:"_RS1" attr:"v=7.582450e+04" dim:0
cell:"res" inst:"_R3" attr:"v=6.801685e+05" dim:0
cell:"res" inst:"_RS2" attr:"v=7.582450e+04" dim:0
cell:"res" inst:"_RS3" attr:"v=4.943491e+04" dim:0
=> circuit/sub3term/term
term:"c" attr:"" dim:0
term:"b" attr:"" dim:0
term:"a" attr:"" dim:0
=> circuit/sub3term/net
net:"c" inst:"" attr:"cd=0;x=40;y=5" subnets:3
    subnet[0]:"p" inst:"_R1" attr:""
    subnet[1]:"p" inst:"_R2" attr:""
    subnet[2]:"p" inst:"_RS1" attr:""
net:"a" inst:"" attr:"cd=0;x=0;y=5" subnets:3
    subnet[0]:"p" inst:"_R3" attr:""
    subnet[1]:"n" inst:"_R1" attr:""
    subnet[2]:"p" inst:"_RS2" attr:""
net:"b" inst:"" attr:"cd=0;x=15;y=35" subnets:3
    subnet[0]:"n" inst:"_R3" attr:""
    subnet[1]:"n" inst:"_R2" attr:""
    subnet[2]:"p" inst:"_RS3" attr:""
net:"SUBSTR" inst:"" attr:"cd=0;x=0;y=0" subnets:3
    subnet[0]:"n" inst:"_RS1" attr:""
    subnet[1]:"n" inst:"_RS2" attr:""
    subnet[2]:"n" inst:"_RS3" attr:""
```

**NOTE**:

Because the net contains a terminal, the x,y position of the terminal is used. The x value is the lower left position of the terminal and the y value is the center position of the terminal. By resistance extraction, the x value is also the center position.

**References**

1. A.J. van Genderen, N.P. van der Meijs, F. Beeftink, and P.J.H. Elias, ‘‘Space User’s Manual,’’ Report ET-NT 92.21, Delft University of Technology, Network Theory Section, Delft, the Netherlands (June 2001).

2. A.J. van Genderen, N.P. van der Meijs, and T. Smedes, ‘‘Space Substrate Resistance Extraction User’s Manual,’’ Report ET-NT 96.03, Delft University of Technology, Network Theory Section, Delft, the Netherlands (July 2002).

CONTENTS