

# **Path Preserving Resistance Extraction**

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## 1. INTRODUCTION

Path preserving can be enabled when a resistance extraction is done. To preserve corner nodes, set parameter "use\_corner\_nodes" to "on". Thus, around the corners of high resistive conductor paths, the *space* extractor shall retain special line nodes. At this way the topology of paths in the layout can be found back in the resulting extracted resistance network.

For making these special line nodes, special equi\_line rectangles are layed done around the corners in the path. Note that for a horizontal path the equi\_line rectangle has a delta-x of  $\text{use\_corner\_ratio} * \text{delta-y}$  (the thickness of the path). And for a vertical path the equi\_line rectangle has a delta-y of  $\text{use\_corner\_ratio} * \text{delta-x}$ . Where parameter "use\_corner\_ratio" has the value 0.5 as default. This makes it possible that these special line nodes are layed done closely to the corners of the path. You may experiment with this "use\_corner\_ratio" value, to see what happens with the resistivity value of the path.

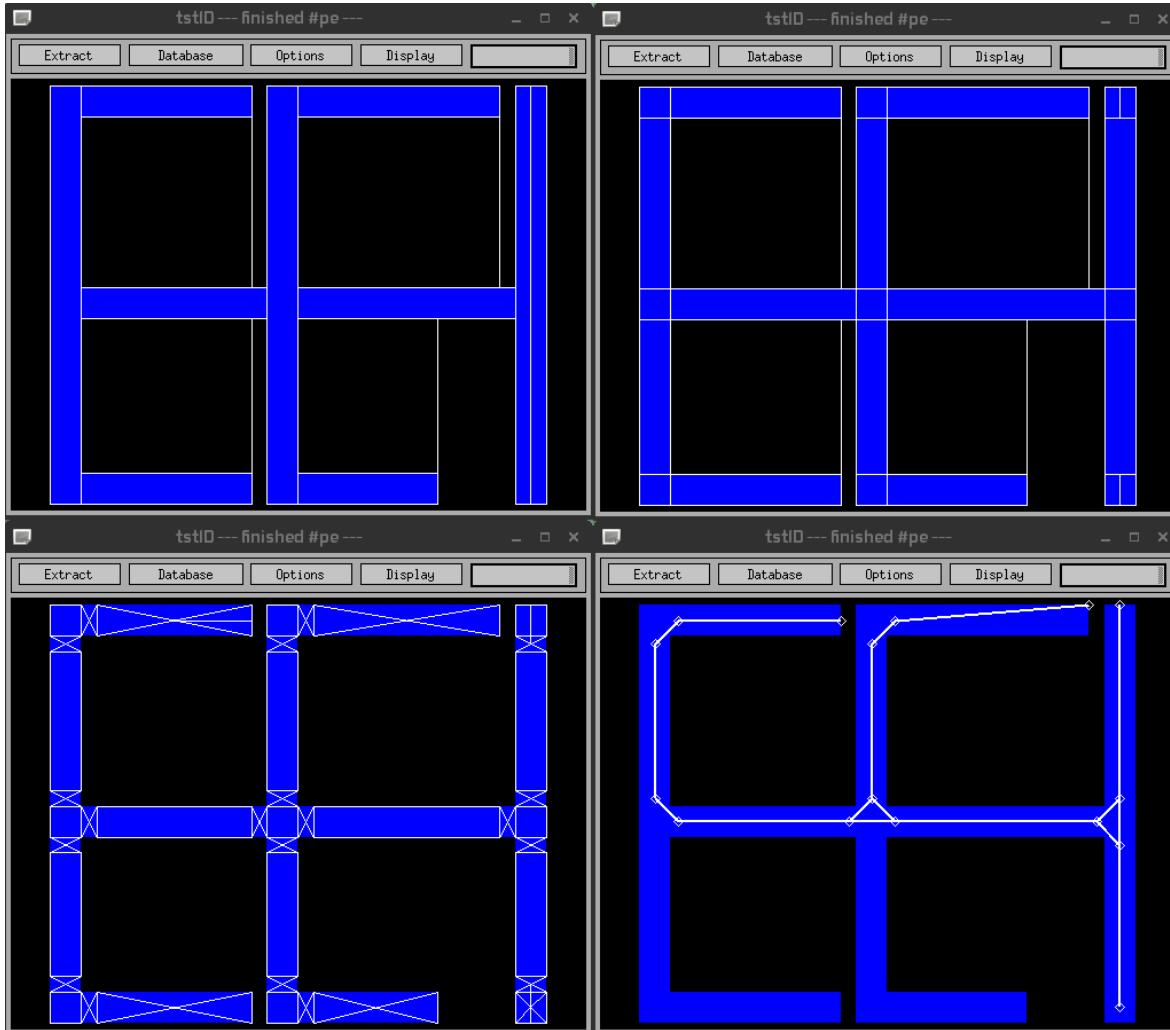
Note that a negative or zero value disables the layment of these special nodes on the path. Thus it is possible to use the special mesh for other resistance extractions.

Note that the resistance mesh corrections has as goal to make maximum use of line nodes. To do this, currently two extra prepass steps are needed. Therefor no other mesh refinement is possible (like option -z). Because the prepass and extract pass must look around to the tiles at the scanline position a new bandwidth is added to the code. By this the enumTile procedure is delayed against the enumPair procedure. Thus, when a tile becomes ready and is done by the enumTile procedure, we can look forward to other tiles with the new introduced bandwidth. And also we can look backward with the same bandwidth, because the tiles are not directly cleared by the clearTile procedure.

Thus, parameter "equi\_line\_width" must be set to a large enough value to work with.

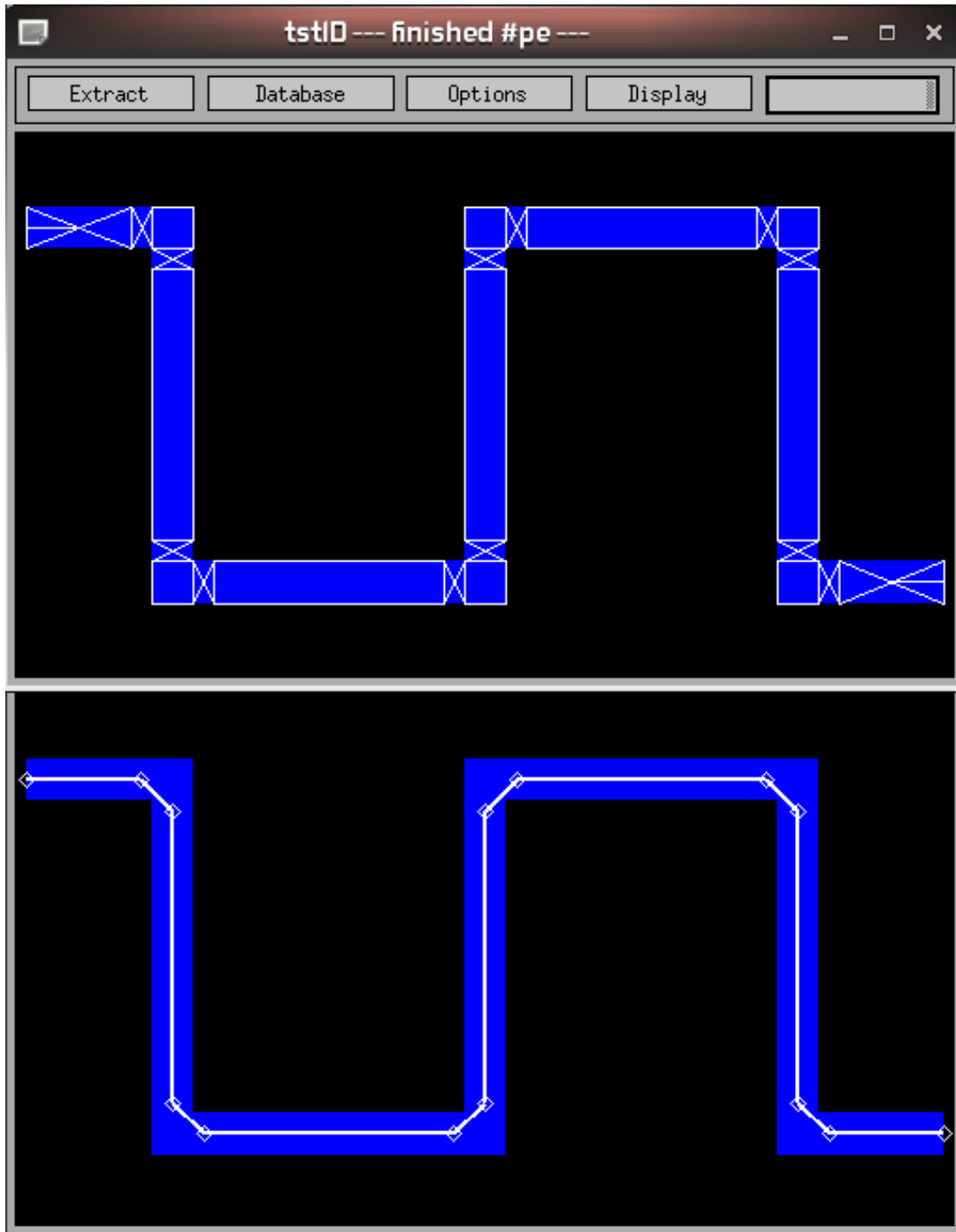
Note that parameter "equi\_line\_area" must not be set to "off" (default "on"). Because in that case the special nodes are not flagged as special area nodes and are not preserved (but eliminated). However you can use it, if you want to know the total resistivity value of the path.

The following pages demonstrate the path preserving technique.

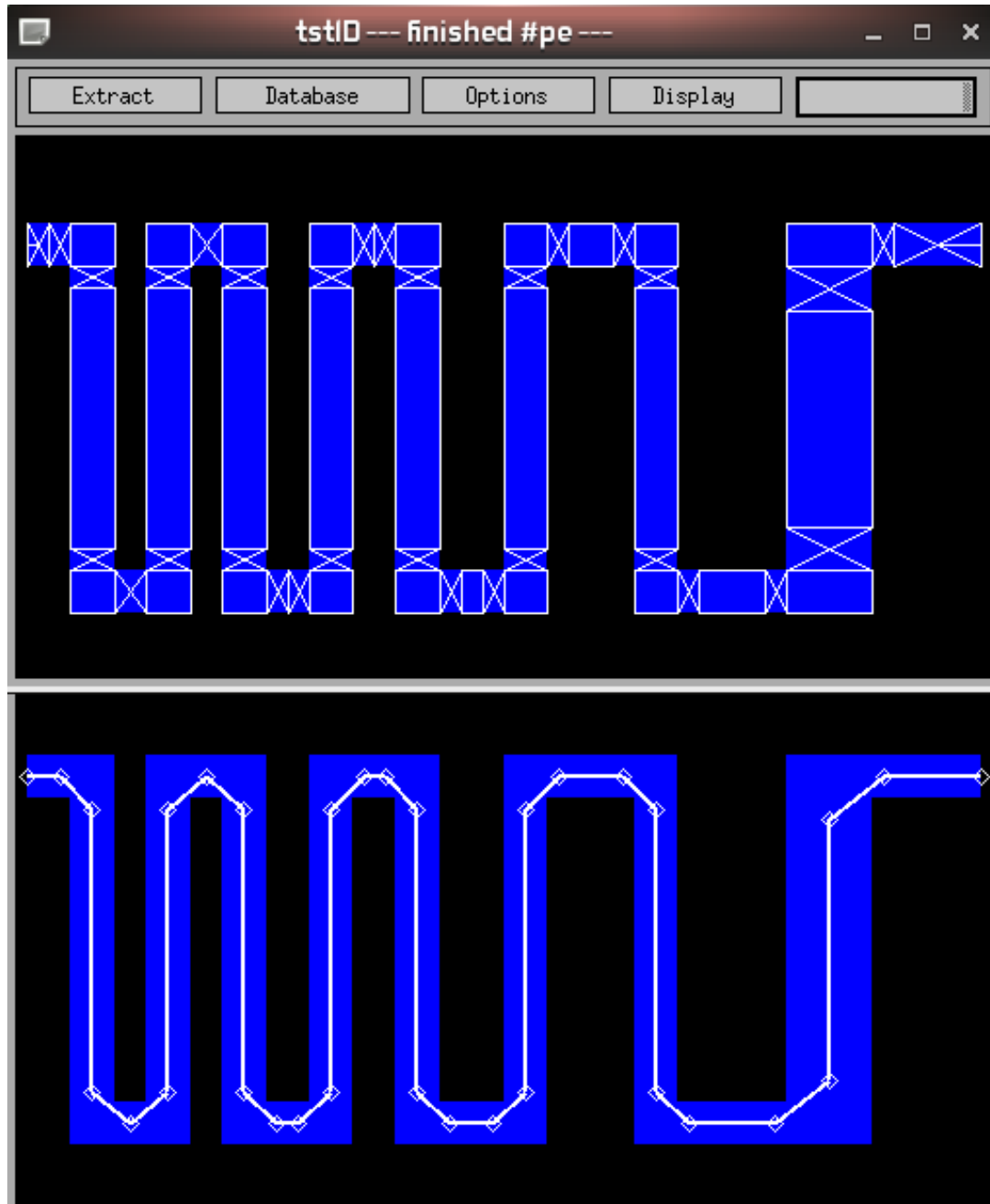


The above pictures demonstrate path preserving. The first picture gives the normally used tiles and boundaries. The first tile on the left side can not have line nodes because it has extra points on its right side. On the right side of the layout you see a tile which is split, because there are terminals defined. The second picture demonstrates what the preprocesses have done. The tiles have get extra splits and two stopping boundaries are layed done to stop the terminal splits.

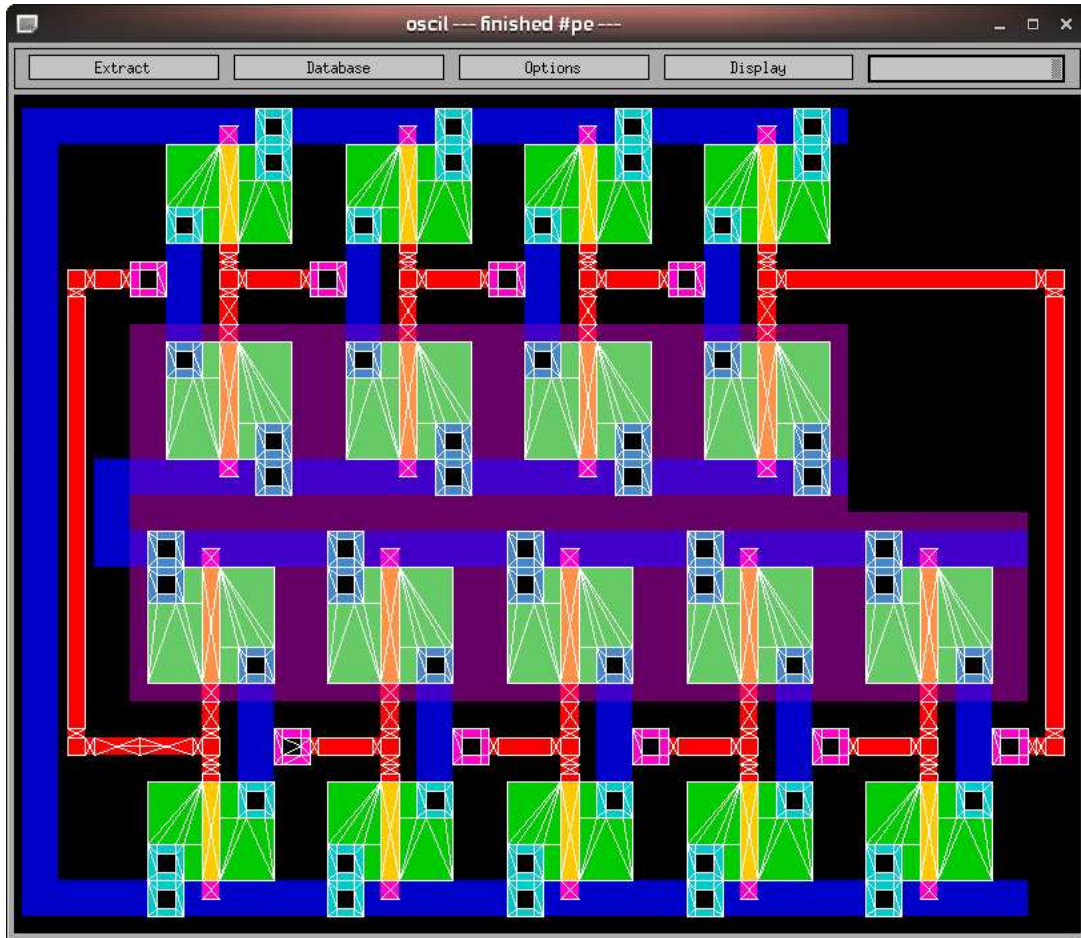
The third picture shows the resulting resistivity mesh by using path preserving. The fourth picture shows the resulting outputted resistivity path and nodes. Because there are only four terminals defined, some parts of the path are dangling. Therefore some special nodes are generated but not preserved.



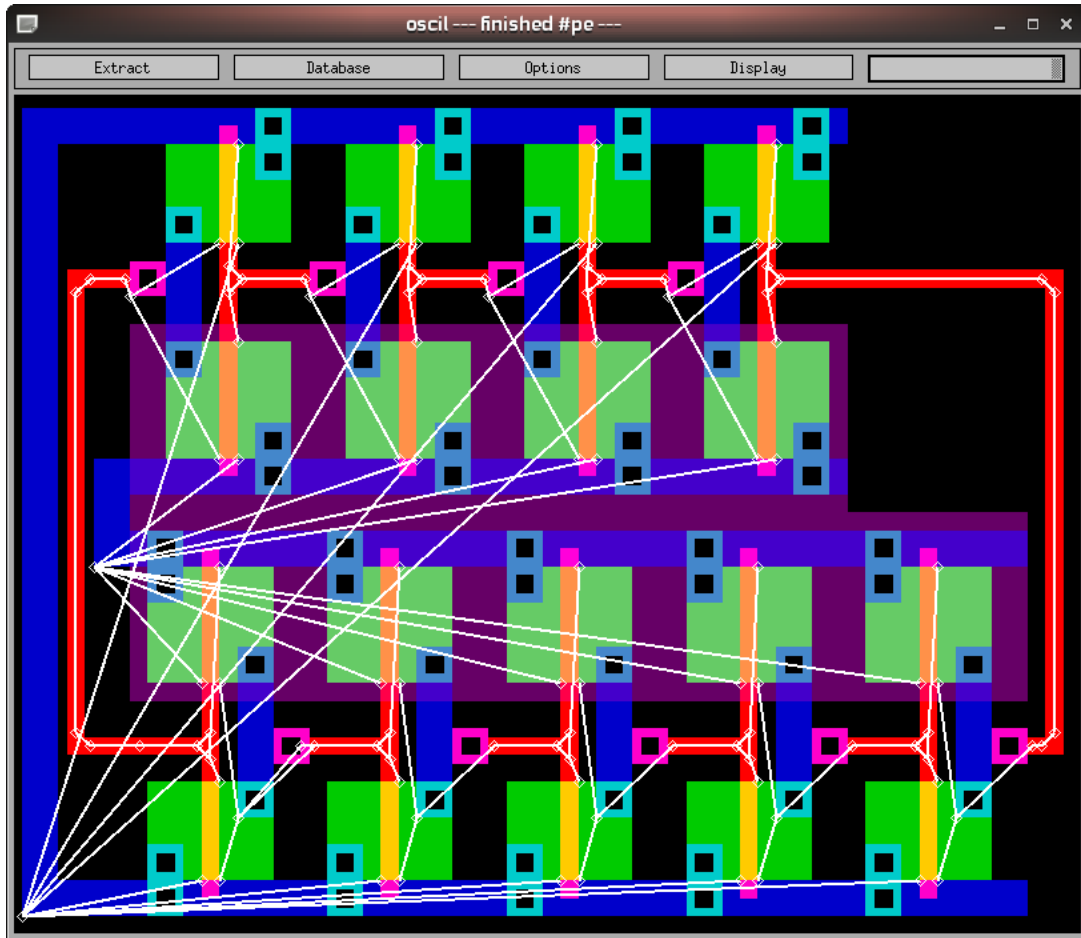
The above pictures demonstrate path preserving. The first picture shows the resulting resistivity mesh and the second picture shows the resulting outputted resistivity path and nodes.



Another example of path preserving. Depending on the distance not always two special nodes can be used. By the terminal node on left top a node is preserved very close to it. On the right side you see that a different path delta-x gives also a different height of the special equi-line rectangle.



This picture is made of the demo/suboscl project and shows the resistivity mesh. You see that only the poly interconnect/gate area's and the source/drain active area's have high resistivity.



This picture of the demo/suboscl project shows the outputted resistor network.

You see that each mos-transistor has three fixed terminal pins. Note that always the upper right node of the gate area is chosen as gate terminal. The vss rail is low res and has one node with coordinates on the lower left. A drain/source pin of each nenh-transistor is connected with a resistor to the vss rail. And also a drain/source pin of each penh-transistor is connected with a resistor to the vdd rail.

You can also see that the inputs of all invertors have an area=2 node with a degree=3, which nodes are retained in the network.

Using the min\_res heuristic shall try to remove the small resistors from the network. I made some arrangements to retain the resistors connected to the special area=1 nodes.