



# Cypress Automotive Products Roadmap

Corporate Presentation

Q2 2018



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# Automotive TrueTouch® Roadmap



# Automotive Portfolio: TrueTouch®

Gen6				Gen7
Touchscreen			Next Generation	
Gestures, AMS <sup>1</sup> Thick Glove <sup>2</sup> or Thick Overlay	In-Cell <sup>3</sup> , Gestures, AMS Thick Glove <sup>6</sup> or Thick/Curved Overlay	SLIM <sup>4</sup> , Force Touch <sup>5</sup> , Gestures, AMS Thick Glove or Thick/Curved Overlay		
10 Finger, AutoArmor™ <sup>7</sup> , DualSense™ <sup>8</sup> , H <sub>2</sub> O <sup>9</sup> , Glove Touch <sup>10</sup> , Grades: A <sup>11</sup> and S <sup>12</sup>				
<div>Active Touch Area</div> <div>&gt; 12"</div> <div>7-12"</div> <div>3-8"</div>	CYAT8168X 88 I/O, 100-Hz RR <sup>13</sup>	CYAT8268X 54 I/O, 100-Hz RR	CYAT8X68X 88 I/O, 100-Hz RR	CYAT8X7XX NDA Required, Contact Sales
	CYAT8168X 77/71 I/O <sup>14</sup> , 120-Hz RR	CYAT8268X 46/39 I/O, 120-Hz RR	CYAT8X68X 77/71 I/O, 120-Hz RR	
	CYAT8168X 61 I/O, 120-Hz RR	CYAT8268X 31 I/O, 120-Hz RR	CYAT8X68X 61 I/O, 120-Hz RR	CYAT8X7XX NDA Required, Contact Sales
	CYAT8165X 48 I/O, 100-Hz RR	CYAT8268X 17 I/O, 120-Hz RR	CYAT8X65X 48 I/O, 100-Hz RR	
	CYAT816XX 36 I/O, 120-Hz RR		CYAT8X6XX 36 I/O, 100-Hz RR	

<sup>1</sup> Automatic mode switching

<sup>2</sup> 1-mm to 5-mm glove thickness (ski gloves)

<sup>3</sup> A type of sensor stack-up in which the RX sensor is inside the LCD module under the color-filter glass

<sup>4</sup> Single-layer independent multi-touch

<sup>5</sup> The ability of touchscreen to distinguish between different levels of force being applied on the touchscreen

<sup>6</sup> Less than 1-mm glove thickness (normal leather gloves)

<sup>7</sup> Enables compliance with chip-level emission, immunity and system-level specifications

<sup>8</sup> Self-capacitance + mutual-capacitance

<sup>9</sup> Waterproofing and wet-finger tracking

<sup>10</sup> A feature that allows the detection of gloved fingers on a touch sensor

<sup>11</sup> AEC-Q100: -40°C to +85°C

<sup>12</sup> AEC-Q100: -40°C to +105°C

<sup>13</sup> Refresh rate

<sup>14</sup> Number of available I/Os depends on package selection

	Concept	Development	Sampling	Production
Industrial				
Automotive				
Availability				



# Automotive Portfolio: TrueTouch® Software<sup>1</sup>

Software	MPN	PSoC® Designer™	TrueTouch® Host Emulator <sup>2</sup>	TrueTouch Driver for Android <sup>3</sup>	Manufacturing Test Kit <sup>4</sup>
Current Version		5.4 SP1	3.4	3.5	1.9.0
Gen 1	CY8CTMA120	Production			
	CY8CTMG120	Production			
Gen 3	CY8CTMA616		Production	TTDA 2.5.1 Production	Production
	CY8CTMA884		Production		Production
Gen 4	CY8CTMA460		Production	TTDA 2.5 Production	Production
	CY8CTMA461		Production		Production
	CY8CTMA768		Production		Production
	CY8CTMA1036		Production		Production
Gen 6	CYAT8165X-48		Production	Contact Sales	Production
	CYAT8168X-61		Production		Production
	CYAT8168X-71		Production		Production
	CYAT8168X-77		Production		Production
	CYAT8168X-88		Production		Production

**Contact Cypress for the latest TrueTouch software, drivers, and tools**

<sup>1</sup> PSoC Designer, TTDE and MTK releases are backward compatible. The latest version is recommended for new designs.

<sup>2</sup> TrueTouch Host Emulator (TTHE) is a front-end tool used to configure, tune, debug and demonstrate TrueTouch devices

<sup>3</sup> TrueTouch Driver for Android (TTDA) is the driver for Android that translates touch information into Linux/Android events

<sup>4</sup> TrueTouch Manufacturing Test Kit (MTK) enables customers and ITO partners to test touch panels that use Cypress TrueTouch controllers through the manufacturing flow

# CYAT8168X

## Automotive TrueTouch® Gen6 Family

### Applications

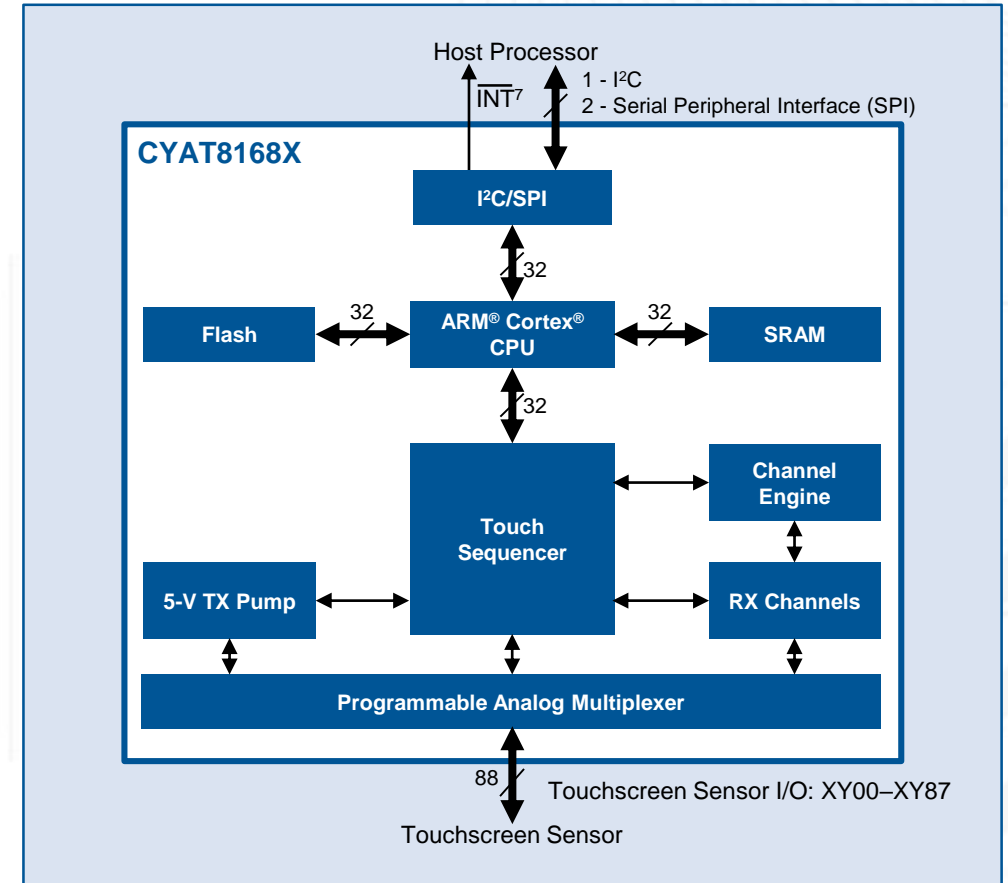
Large touchscreen human machine interface (HMI) systems

### Features

- **Advanced User Interface**
  - Waterproofing<sup>1</sup>: Works with water droplets, condensation, sweat and wet-finger tracking
  - Tracking with up to 5-mm thick gloves or thick overlay
- **Proprietary Analog Front End<sup>2</sup> (AFE) with AutoArmor™<sup>3</sup>**
  - True 5-V TX-Boost™ with Multi-Phase TX<sup>4</sup>
  - 54 Receive Channels to support ≥100-Hz refresh rates
  - DualSense™: Self<sup>5</sup>- and mutual<sup>6</sup>-capacitance AFE (U.S. Patents 8,773,146; 8,358,142; 8,319,505; and 8,067,948)
  - AutoArmor enables compliance with chip-level emissions (IEC 61967), immunity (IEC 62132) and system-level (CISPR 25) specifications
- **System Solutions**
  - Manufacturing test kits for production testing
- **Package**
  - 128-pin TQFP, 100-pin TQFP

### Collateral

Datasheet and Design Guide: [Contact Sales](#) or [automotive@cypress.com](mailto:automotive@cypress.com)



### Availability

**Production:** Now

<sup>1</sup> The ability of a touchscreen sensor to work properly in the presence of water droplets, condensation or sweat

<sup>2</sup> Analog circuit in the touchscreen controller used to measure self- and mutual-capacitance

<sup>3</sup> Cypress proprietary technology used to reduce emissions and improve EMI immunity to meet automotive EMC requirements

<sup>4</sup> A scanning method used to drive multiple TX lines simultaneously

<sup>5</sup> The capacitance of a row or column line in a touchscreen sensor

<sup>6</sup> The capacitance between a row and a column in a touchscreen sensor

<sup>7</sup> Interrupt

# Automotive TrueTouch® Packages

Family	Package	QFN	TQFP		
	Pins	56	64	100	128
	Body Size (mm)	8 x 8	10 x 10	14 x 14	14 x 20
	Pitch (mm)	0.5	0.5	0.5	0.5
Gen 4	CY8CTMA460	✓ <sup>1</sup>		✓	
	CY8CTMA461	✓ <sup>1</sup>		✓	
	CY8CTMA768			✓	
	CY8CTMA1036			✓	
Gen 6	CYAT8165X-48			✓	
	CYAT8168X-61			✓	
	CYAT8168X-71			✓	
	CYAT8168X-77			✓	
	CYAT8168X-88				✓

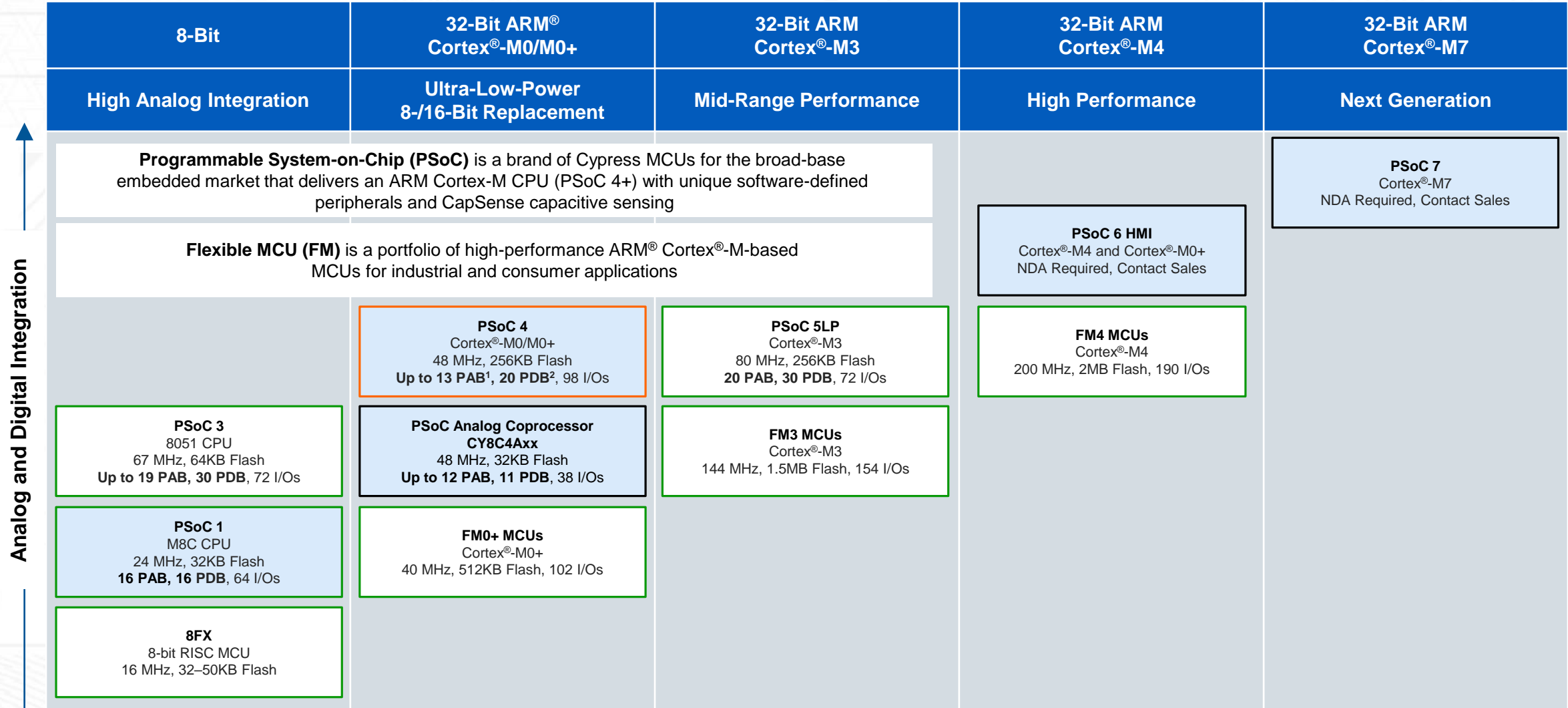
<sup>1</sup> Wettable flanks package to allow automated optical inspection (AOI)

# Automotive PSoC® Roadmap





# Automotive PSoC and MCU Portfolio



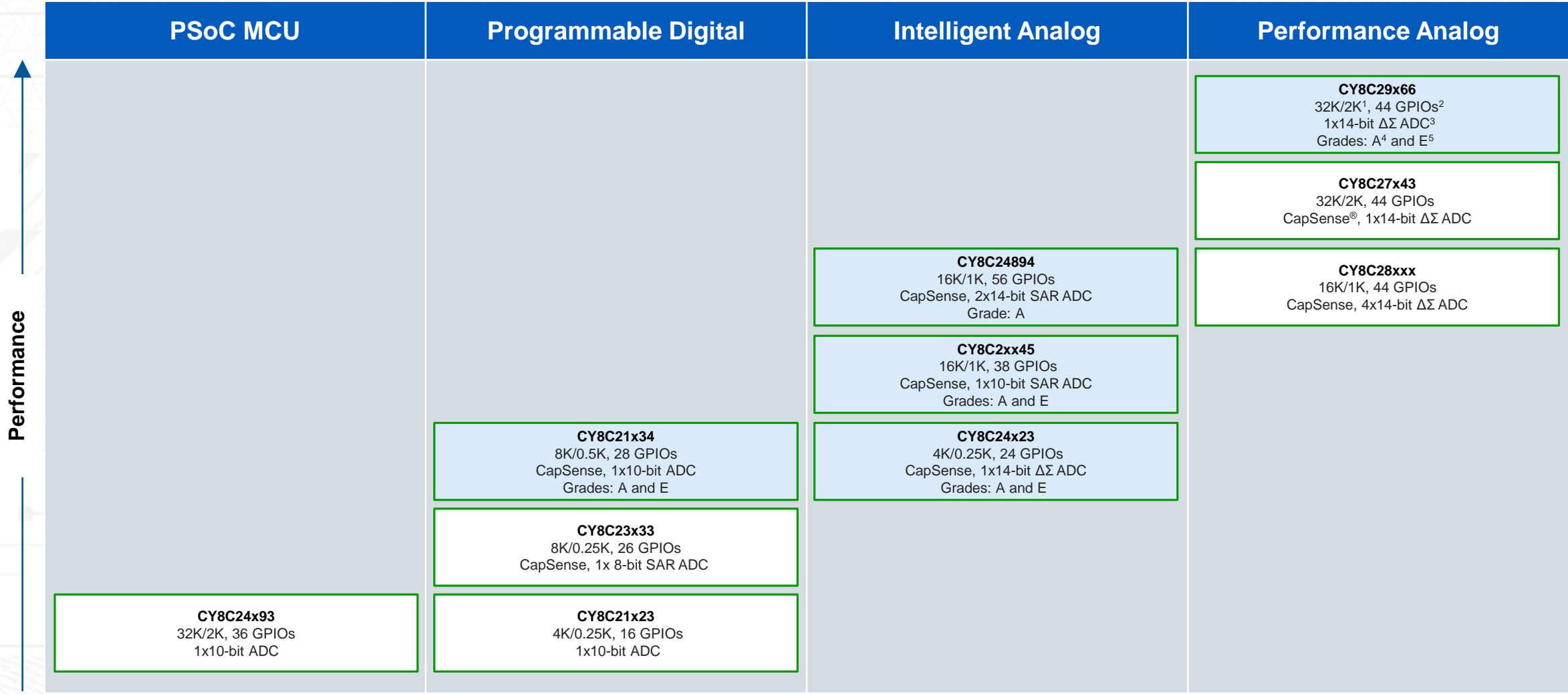
<sup>1</sup> A programmable analog block that is configured using PSoC software to create analog front ends, signal conditioning circuits with opamps and filters

<sup>2</sup> A programmable digital block that is configured using PSoC software to implement custom digital peripherals and glue logic



# Automotive Portfolio: PSoC® 1

## M8C CPU | 24 MHz



<sup>1</sup> Flash KB/SRAM KB

<sup>2</sup> General-purpose input/output pins

<sup>3</sup> Analog-to-digital converter: Includes incremental, successive approximation register (SAR) or Delta-Sigma (ΔΣ) ADCs

<sup>4</sup> AEC-Q100: -40°C to +85°C

<sup>5</sup> AEC-Q100: -40°C to +125°C



**Flexibility | CapSense® | Ease-of-Use**

## Flash



# Automotive Portfolio: PSoC<sup>®</sup> Software<sup>1</sup>

Software	PSoC Creator <sup>TM2</sup>	PSoC Designer <sup>TM3</sup>	PSoC Programmer <sup>4</sup>	EZ-Click <sup>TM5</sup>
Current Version	4.2	5.4 SP1	3.27.1	2.0 SP2
PSoC 1		Production	Production	
PSoC 4	Production		Production	

Download the latest PSoC software version [here](#)

<sup>1</sup> All software and tool releases are backward compatible. The latest versions are recommended for new designs

<sup>2</sup> PSoC Creator is an Integrated Design Environment (IDE) that allows concurrent hardware and firmware design of PSoC 3 and PSoC 4 systems

<sup>3</sup> PSoC Designer is an IDE that enables firmware design using a library of precharacterized peripherals for PSoC 1 systems

<sup>4</sup> PSoC Programmer can be used with PSoC Designer and PSoC Creator to program and debug any design onto a PSoC device

<sup>5</sup> EZ-Click is a Windows<sup>®</sup> GUI-based tool that enables development of CapSense MBR solutions. It allows you to set up sensor configuration, apply global system properties, monitor real-time sensor output, and run production-line system diagnostics

# PSoC® 4000S-Series

## PSoC MCU

### Applications

User interface for infotainment systems, user interface for heating, ventilation, and air conditioning

### Features

- **32-Bit MCU Subsystem**
  - 48-MHz ARM® Cortex®-M0+ CPU
  - Up to 32KB Flash
  - 4KB SRAM
  - Real-time clock (RTC) capability with a watch crystal oscillator (WCO)
- **Programmable Analog Blocks**
  - One 10-bit, 46.8-ksps single-slope analog-to-digital converter (ADC)<sup>1</sup>
  - Two low-power comparators (CMP)
  - One CapSense® block that supports low-power operation with self- and mutual-capacitance sensing
  - Two 7-bit current-output digital-to-analog converters (IDAC) configurable as a single 8-bit IDAC
- **Programmable Digital Blocks**
  - Five 16-bit timer/counter/pulse-width modulation (TCPWM) blocks
  - Two serial communication blocks (SCB) that are configurable as I<sup>2</sup>C, SPI, UART or LIN Slave
- **Packages**
  - 24-pin QFN and 28-pin SSOP
- **I/O Subsystem**
  - Up to 24 GPIOs, including 16 Smart I/Os<sup>2</sup>

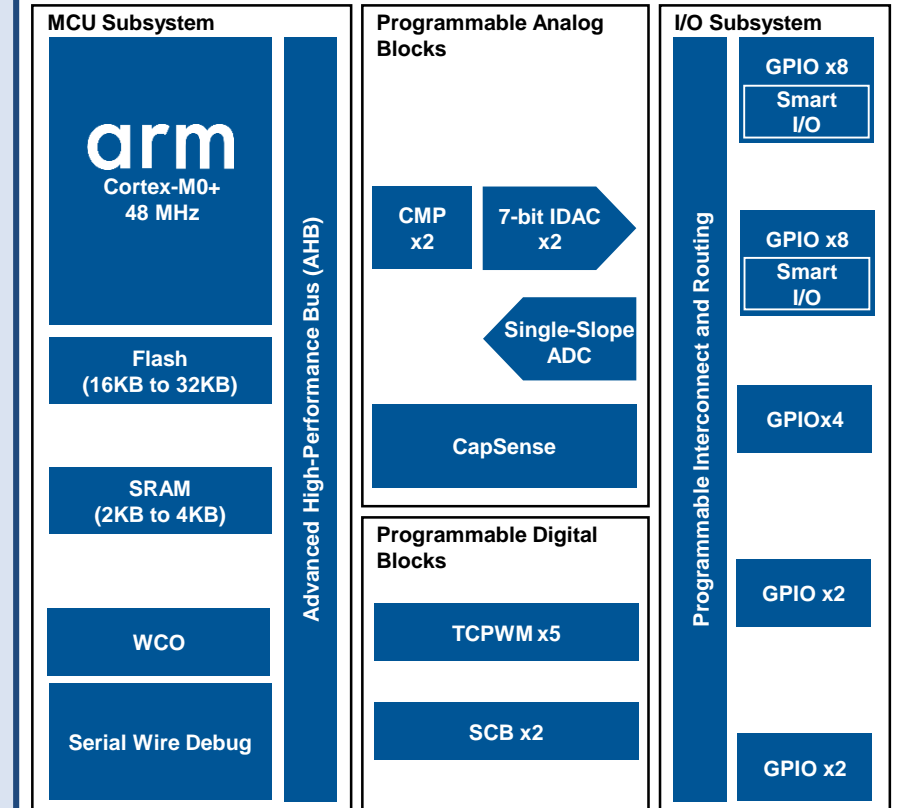
### Collateral

Datasheet: [Contact Sales](#)

<sup>1</sup> A simple ADC used to measure slow-moving signals

<sup>2</sup> Embedded programmable digital logic in the I/O subsystem

### PSoC® 4 One-Chip Solution



### Availability

Sampling: Now

Production: Q2 2018



# PSoC® 4100S-Series

## Intelligent Analog

### Applications

User interface for heating, ventilation, air conditioning, MCU, and discrete analog replacement

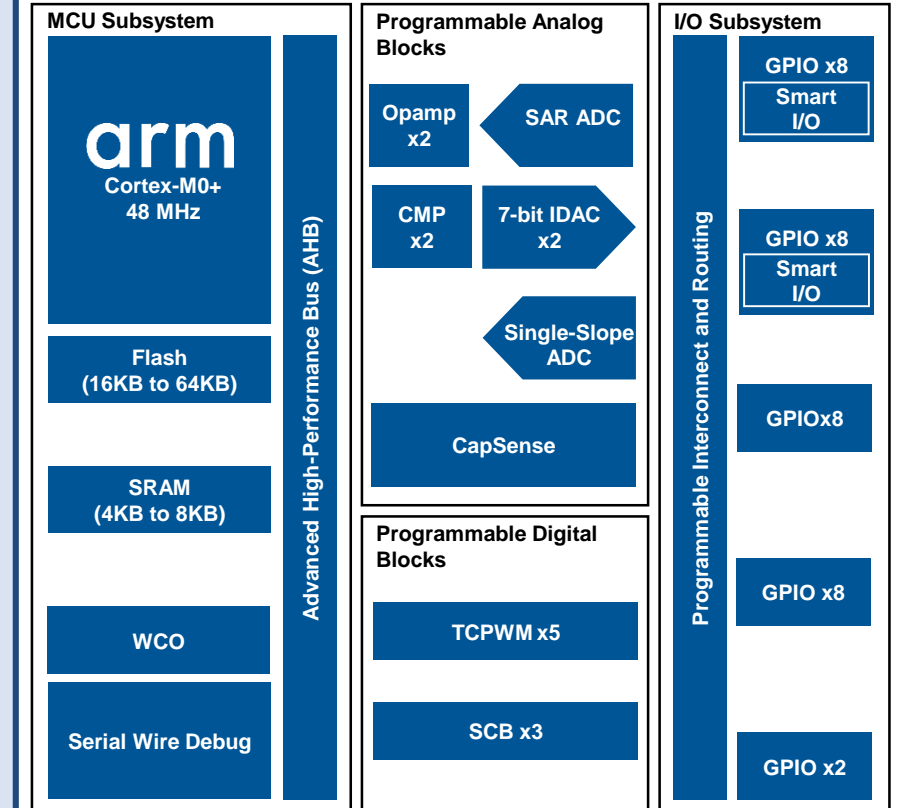
### Features

- **32-Bit MCU Subsystem**
  - 48-MHz ARM® Cortex®-M0+ CPU
  - Up to 64KB Flash
  - 8KB SRAM
  - Real-time clock (RTC) capability with a watch crystal oscillator (WCO)
- **Programmable Analog Blocks**
  - One 12-bit, 1-Msps successive approximation register (SAR) analog-to-digital converter (ADC)
  - One 10-bit, 46.8-kSPS single-slope ADC<sup>1</sup>
  - Two opamps configurable as programmable gain amplifiers (PGA), comparators, etc.
  - Two low-power comparators (CMP)
  - One CapSense® block that supports low-power operation with self- and mutual-capacitance sensing
  - Two 7-bit current-output digital-to-analog converters (IDAC) configurable as a single 8-bit IDAC
- **Programmable Digital Blocks**
  - Five 16-bit timer/counter/pulse-width modulation (TCPWM) blocks
  - Three serial communication blocks (SCBs) that are configurable as I<sup>2</sup>C, SPI, UART or LIN Slave
- **Packages**
  - 28-pin SSOP and 40-pin QFN
- **I/O Subsystem**
  - Up to 34 GPIOs, including 16 Smart I/Os<sup>2</sup>

### Collateral

Datasheet: [Contact Sales](#)

### PSoC® 4 One-Chip Solution



### Availability

Sampling: Now

Production: Q2 2018

<sup>1</sup> A simple ADC used to measure slow-moving signals

<sup>2</sup> Embedded programmable digital logic in the I/O subsystem

# PSoC® 4100S Plus-Series

## Intelligent Analog

### Applications

User interface for HMI applications, body control, and HVAC applications

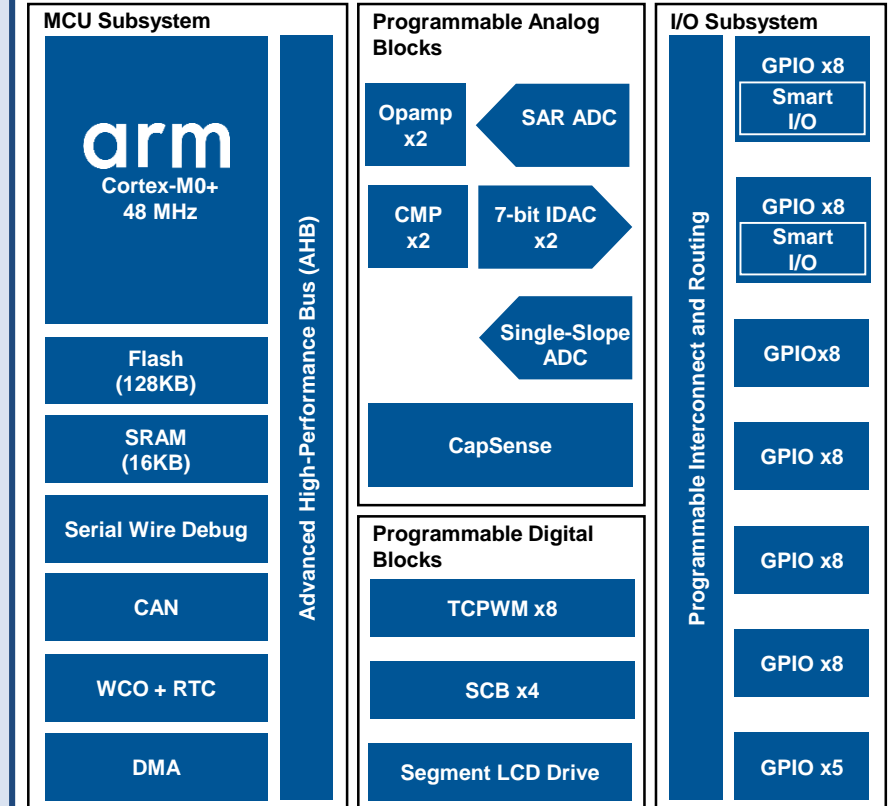
### Features

- **32-Bit MCU Subsystem**
  - 48-MHz ARM® Cortex®-M0+ CPU with DMA controller and real-time clock (RTC)
  - 128KB Flash and 16KB SRAM
  - External MHz oscillator (ECO) with PLL and 32KHz watch crystal oscillator (WCO)
- **Programmable Analog Blocks**
  - One 12-bit, 1-Msps successive approximation register (SAR) analog-to-digital converter (ADC)
  - One 10-bit, 46.8-ksps single-slope ADC<sup>1</sup>
  - Two opamps configurable as programmable gain amplifiers (PGA), comparators, etc.
  - Two low-power comparators (CMP)
  - One CapSense® block that supports low-power operation with self- and mutual-capacitance sensing
  - Two 7-bit current-output digital-to-analog converters (IDAC) configurable as a single 8-bit IDAC
- **Programmable Digital Blocks**
  - Eight 16-bit timer/counter/pulse-width modulation (TCPWM) blocks
  - Five serial communication blocks (SCBs) that are configurable as I<sup>2</sup>C, SPI, UART or LIN Slave
- **One Controller Area Network (CAN) Controller**
- **Packages**
  - 64-pin TQFP
- **I/O Subsystem**
  - Up to 54 GPIOs, including 16 Smart I/Os<sup>2</sup>

### Collateral

Datasheet: [Contact Sales](#)

### PSoC® 4 One-Chip Solution



### Availability

Sampling: Q2 2018

Production: Q3 2018

<sup>1</sup> A simple ADC used to measure slow-moving signals

<sup>2</sup> Embedded programmable digital logic in the I/O subsystem

# PSoC® 4100M-Series

## Intelligent Analog

### Applications

User interface for HMI applications, body control, and HVAC applications

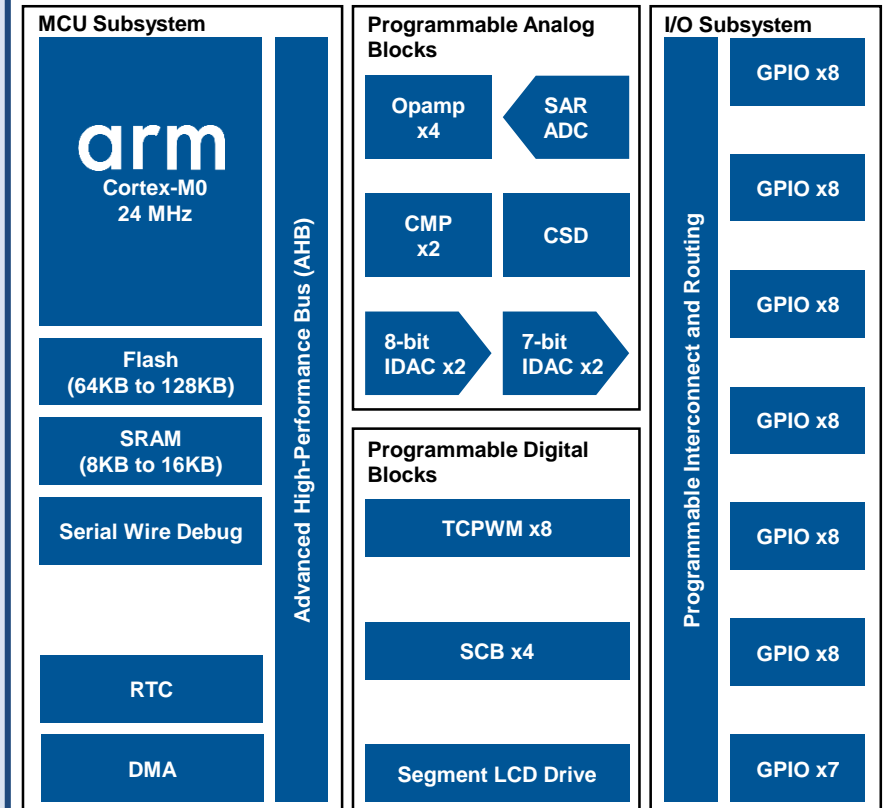
### Features

- **32-bit MCU Subsystem**
  - 24-MHz ARM® Cortex®-M0 CPU with a DMA controller and real-time clock (RTC)
  - Up to 128KB Flash and 16KB SRAM
- **Programmable Analog Blocks**
  - Two comparators (CMP)
  - Four opamps, programmed as PGAs, CMPs, filters, etc.
  - One 12-bit/1-Msps successive approximation register (SAR) ADC
  - One CapSense® block with self- and mutual-capacitance sensing
  - Four (2x 8-bit, 2x 7-bit) current-output digital-to-analog converters (IDACs)
- **Programmable Digital Blocks**
  - Eight programmable 16-bit timer/counter/pulse-width modulation (TCPWM) blocks
  - Four serial communication blocks (SCBs) configurable as I²C master or slave, SPI master or slave, or UART
- **Packages**
  - 48-pin LQFP and 64-pin TQFP
- **I/O Subsystem**
  - Up to 51 GPIOs

### Collateral

Datasheet: [Contact Sales](#)

### PSoC® 4 One-Chip Solution



### Availability

Sampling: Now

Production: Q3 2018

# PSoC® 4200M-Series

## Programmable Digital

### Applications

User interface for HMI applications, body control, and HVAC applications

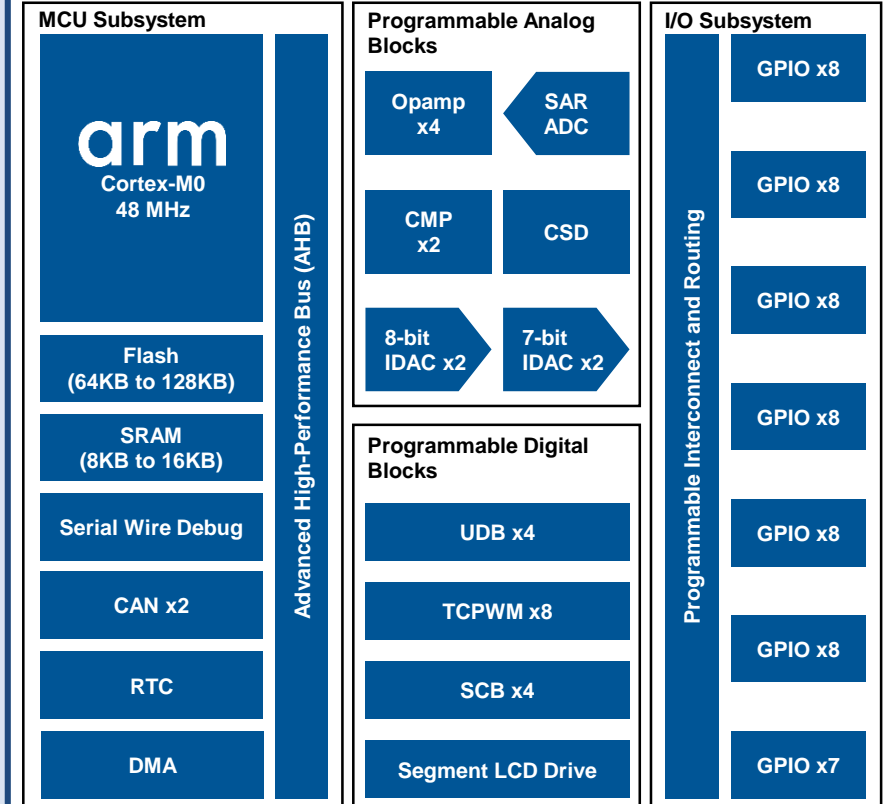
### Features

- **32-bit MCU Subsystem**
  - 48-MHz ARM® Cortex®-M0 CPU with a DMA controller and real-time clock (RTC)
  - Up to 128KB Flash and 16KB SRAM
- **Programmable Analog Blocks**
  - Two comparators (CMP)
  - Four opamps, programmed as PGAs, CMPs, filters, etc.
  - One 12-bit/1-Msps successive approximation register (SAR) analog-to-digital converter (ADC)
  - One CapSense® block with self- and mutual-capacitance sensing
  - Four (2x 8-bit, 2x 7-bit) current-output digital-to-analog converters (IDACs)
- **Programmable Digital Blocks**
  - Four universal digital blocks (UDBs): custom digital peripherals
  - Eight programmable 16-bit timer/counter/pulse-width modulation (TCPWM) blocks
  - Four serial communication blocks (SCBs) configurable as I²C master or slave, SPI master or slave, or UART
- **Two Controller Area Network (CAN) Controllers**
- **Packages**
  - 48-pin LQFP, 56-pin QFN and 64-pin TQFP

### Collateral

Datasheet: [Contact Sales](#)

### PSoC® 4 One-Chip Solution



### Availability

Sampling: Now

Production: Q3 2018

# Automotive PSoC Packages

Family	Package	QFN		SOIC	SSOP		
	Pins	24	56	16	20	28	48
	Body Size (mm)	4 x 4	8 x 8	3.8 x 9.9	5.3 x 7.3	5.3 x 10.3	7.5 x 15.8
	Pitch (mm)	0.5	0.5	1.27	0.65	0.65	0.635
PSoC 1	2XX45					✓	✓
	21X34				✓	✓	
	24X23				✓	✓	
	24894		✓				
	29X66					✓	✓
PSoC 4	4000	✓		✓			
	41/42XX					✓	



# Cypress Roadmap: Automotive RAM



# 2Mb-to-16Mb Excelon™ F-RAM Family

## Applications

Medical devices, wearables, industrial control and automation, automotive

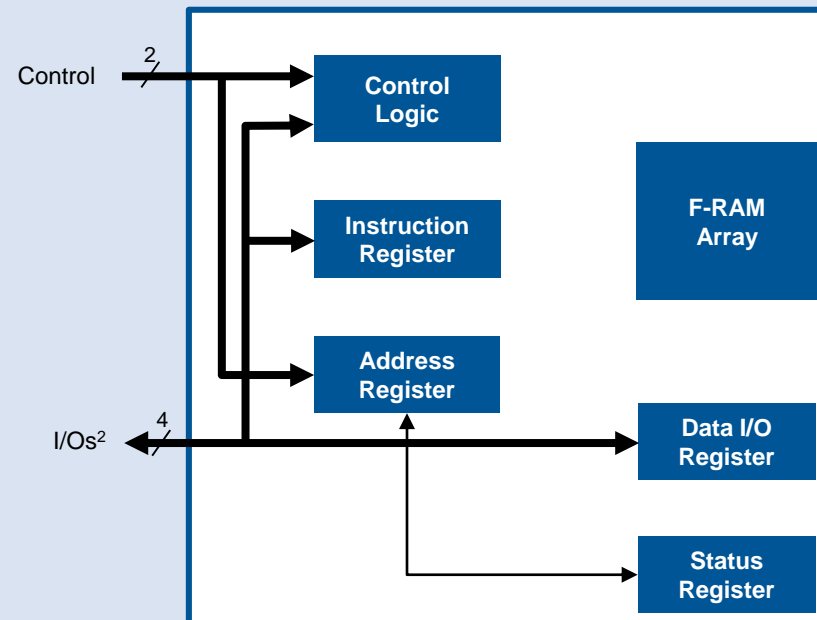
## Features

- **Excelon-Ultra**
  - 4Mb
  - 108-MHz Single Data Rate (SDR)/54-MHz Double Data Rate (DDR) Quad SPI
  - Industrial temperature range: -40°C to +85°C
- **Excelon-Auto**
  - 2Mb Auto E, 4Mb Auto A
  - 50-MHz SPI
  - Automotive (AEC-Q100) temperature range grade A: -40°C to +85°C
  - Automotive (AEC-Q100) temperature range grade E: -40°C to +125°C
- **Common Features for Excelon-Ultra/Auto**
  - Operating voltage range: 1.71–1.89 V, 1.80–3.60 V
  - 100-trillion read/write cycle endurance
  - 100-year data retention

## Collateral

Preliminary Datasheet: [Contact Sales](#) (Available Now)

## Excelon F-RAM



## Family Table

Density	Standby Current (Typ.)	Active Current (Typ.)	Packages
2Mb	1 µA	3 mA	SOIC (8)
4Mb	1 µA	3 mA	SOIC (8), GQFN (8)
8Mb	1 µA	3 mA	GQFN (8)
16Mb	1 µA	3 mA	SOIC (8), GQFN (8)

## Availability

**Samples:** Now (2Mb Auto, 4Mb, 8Mb), Q2 2019 (2Mb, 16Mb)

**Production:** Q4 2018 (2Mb Auto, 4Mb, 8Mb), Q4 2019 (2Mb, 16Mb)

**High Density | Wide Voltage Range | Automotive A<sup>1</sup>, E<sup>2</sup> | On-Chip ECC**

64Kb-1Mb      2Mb-16Mb      32Mb-64Mb

<sup>4</sup> A Fast SRAM with a deep-sleep mode in addition to the conventional standby



# Low-Power SRAM Family with ECC<sup>1</sup>

## Applications

Programmable logic controllers, handheld devices, multifunction printers, implantable medical devices, computation servers and automotive

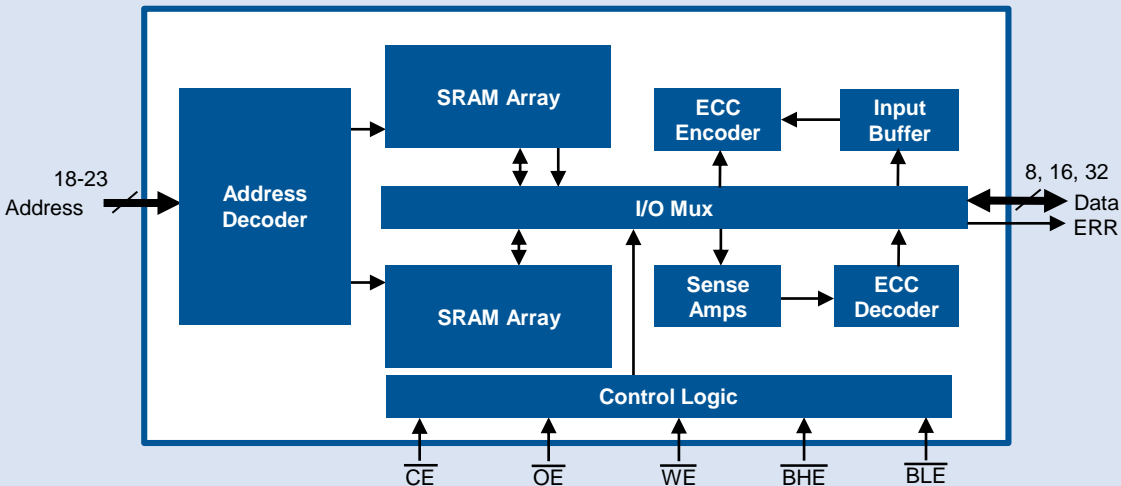
## Features

- **Speed**
  - Access time: 45 ns
  - Bus-width configurations: x8, x16 and x32
- **Low Power**
  - Standby current: 8.7  $\mu$ A for 4Mb
- **Features**
  - ECC<sup>1</sup> logic to detect and correct single-bit errors
- **Multiple Operating Temperatures**
  - Industrial and automotive temperature grades
- **RoHS<sup>2</sup>-Compliant Packages**
  - 48-ball and 119-ball BGA
  - 32-pin and 44-pin TSOP-II
  - 48-pin TSOP-I
  - 32-pin SOIC

## Collateral

**Datasheet:** [Asynchronous SRAM with ECC](#)

## SRAM with ECC



## Family Table

Density	MPN	Standby Current (Maximum at 85°C)	Standby Current (Typical at 25°C)
4Mb	CY6214x	8.7 $\mu$ A	3.5 $\mu$ A
8Mb	CY6215x	16.0 $\mu$ A	5.5 $\mu$ A
16Mb	CY6216x	16.0 $\mu$ A	5.5 $\mu$ A

## Availability

**Production:** Now

<sup>1</sup> Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation

<sup>2</sup> Restriction of Hazardous Substances. A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components

# Fast SRAM Family with PowerSnooze™<sup>1</sup>

## Applications

Programmable logic controllers, handheld devices, multifunction printers, computation servers and automotive

## Features

- **Speed**
  - Access time: 10 ns
  - Bus-width configurations: x8, x16 and x32
- **Low Power**
  - Deep-sleep current: 15 µA for 4Mb
- **Features**
  - ECC<sup>2</sup> logic to detect and correct single-bit errors
  - Bit-interleaving to avoid multi-bit errors
  - Error Indication (ERR) pin to indicate single-bit errors
- **Multiple Operating Temperatures**
  - Industrial and automotive temperature grades
- **RoHS<sup>3</sup>-Compliant Packages**
  - 48-ball BGA
  - 44-pin and 54-pin TSOP-II
  - 48-pin TSOP-I
  - 36-pin and 44-pin SOJ

## Collateral

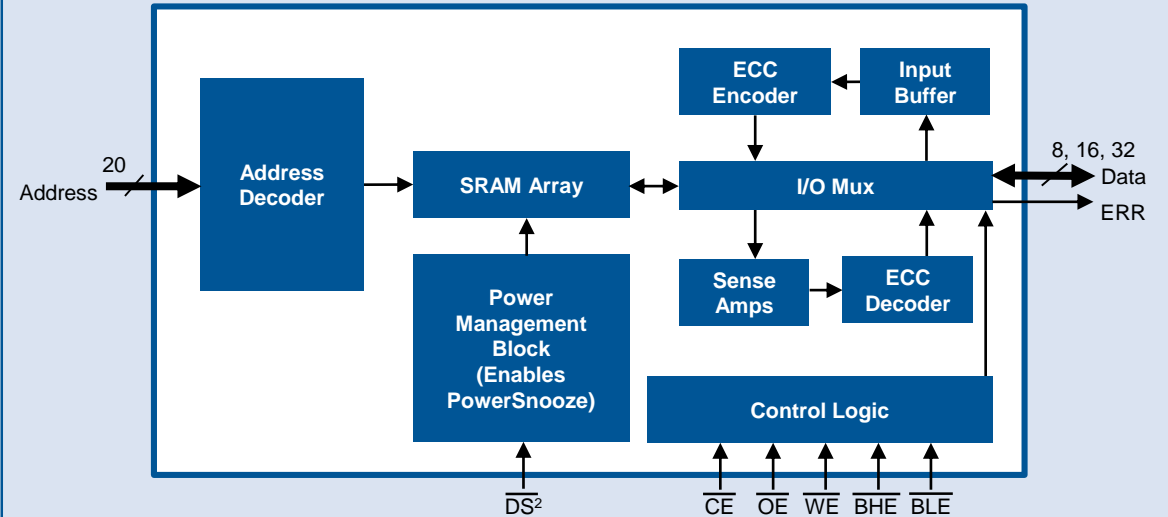
**Datasheet:** [Asynchronous SRAM with ECC](#)

<sup>1</sup> A Fast SRAM with a deep-sleep mode in addition to a conventional standby mode

<sup>2</sup> Error-correcting code

<sup>3</sup> Restriction of Hazardous Substances. A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components

## SRAM with PowerSnooze



## Family Table

Density	MPN	Access Time	Deep Sleep Current (Maximum at 85°C)
4Mb	CY7S104x	10 ns	15 µA
16Mb	CY7S106x	10 ns	22 µA

## Availability

**Production:** Now



# Fast SRAM Family with ECC<sup>1</sup>

## Applications

Switches and routers, IP phones, test equipment, computation servers, automotive, military and aerospace systems

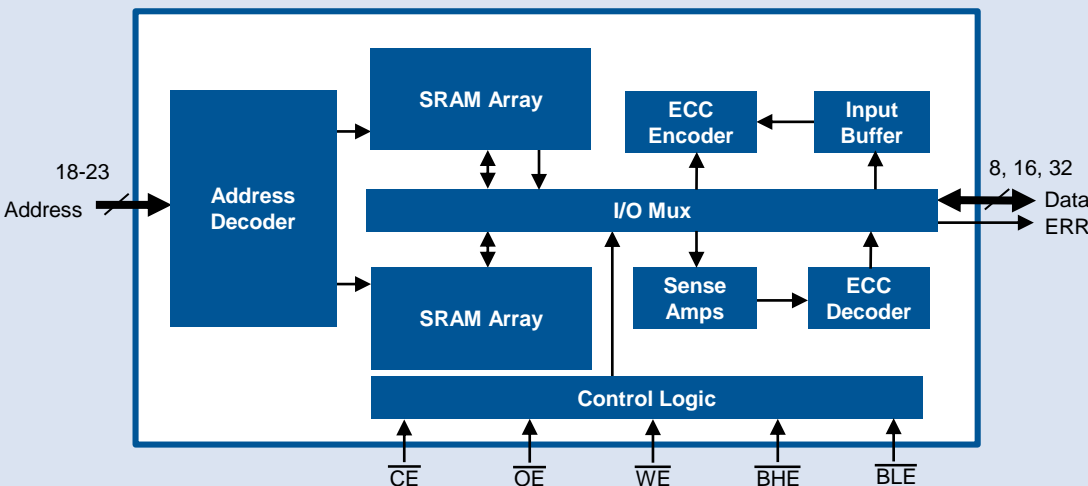
## Features

- **Speed**
  - Access time: 10 ns
  - Bus-width configurations: x8, x16 and x32
- **Features**
  - ECC logic to detect and correct single-bit errors
  - Bit-interleaving to avoid multi-bit errors
  - Error indication (ERR) pin to indicate single-bit errors
- **Multiple Operating Temperatures**
  - Industrial and automotive temperature grades
- **RoHS<sup>2</sup>-Compliant Packages**
  - 48-ball and 119-ball BGA
  - 44-pin and 54-pin TSOP-II
  - 48-pin TSOP-I
  - 34-pin and 36-pin SOJ

## Collateral

**Datasheet:** [Asynchronous SRAM with ECC](#)

## SRAM with ECC



## Family Table

Density	MPN	Access Time	Operating Current (Maximum at 85°C)
4Mb	CY7C104x	10 ns	45 mA
8Mb	CY7C105X	10 ns	110 mA
16Mb	CY7C106x	10 ns	110 mA

## Availability

**Production:** Now

<sup>1</sup> Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation

<sup>2</sup> Restriction of Hazardous Substances. A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components

# Standard Synchronous SRAM With On-Chip ECC<sup>1</sup>

## Applications

Switches and routers, radar and signal processing, test equipment, automotive, military and aerospace systems

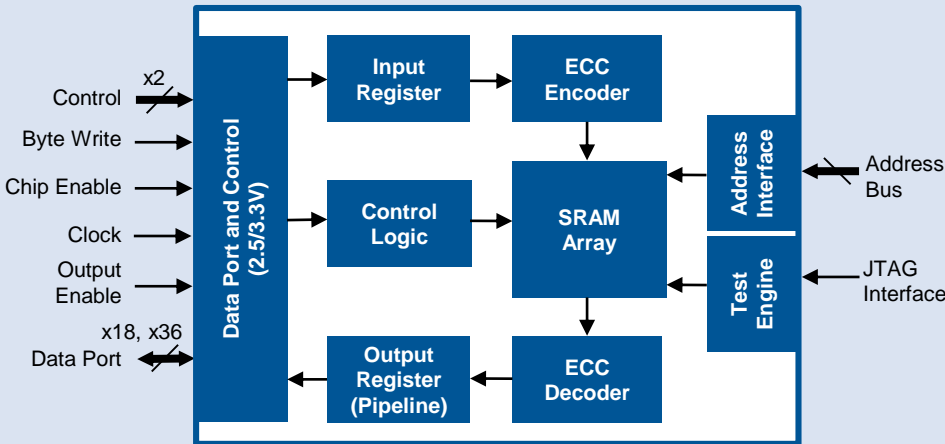
## Features

- **Speed**
  - Available in two modes<sup>2</sup>: Pipeline and Flow-Through
  - Bus widths: x18, x36
- **Features**
  - ECC to detect and correct single-bit errors
  - Two voltage options: 2.5 V and 3.3 V
  - SCD and DCD deselect options<sup>3</sup>
  - Industrial and commercial temperature grades
- **Packages**
  - 165-ball BGA
  - 100-pin TQFP

## Collateral

**Datasheets:** [36M Sync SRAM](#), [18M Sync SRAM](#)

## Synchronous SRAM



## Family Table

Option	Density	MPN	RTR	FIT/Mb <sup>4</sup>
Standard Sync with On-Chip ECC Pipeline	18Mb 36Mb	CY7C1370/2K CY7C1440/2K	250 MT/s	<0.01
Standard Sync with On-Chip ECC Flow-Through	18Mb 36Mb	CY7C1371/3K CY7C1441/3K	133 MT/s	<0.01

## Availability

**Production:** Now

<sup>1</sup> Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation

<sup>2</sup> Modes of synchronous SRAM operation that optimize either read latency (Flow-Through) or operating frequency (Pipeline)

<sup>3</sup> Modes of operation in Pipeline mode where the output driver is tri-stated after either a single cycle (SCD) or dual cycle (DCD) of issuing the deselect command

<sup>4</sup> The projected failure rate of a device; one FIT/Mb equals one failure per billion device hours per megabit of data

# NoBL<sup>®</sup> SRAM With On-Chip ECC<sup>1</sup>

## Applications

Switches and routers, radar and signal processing, test equipment, automotive, military and aerospace systems

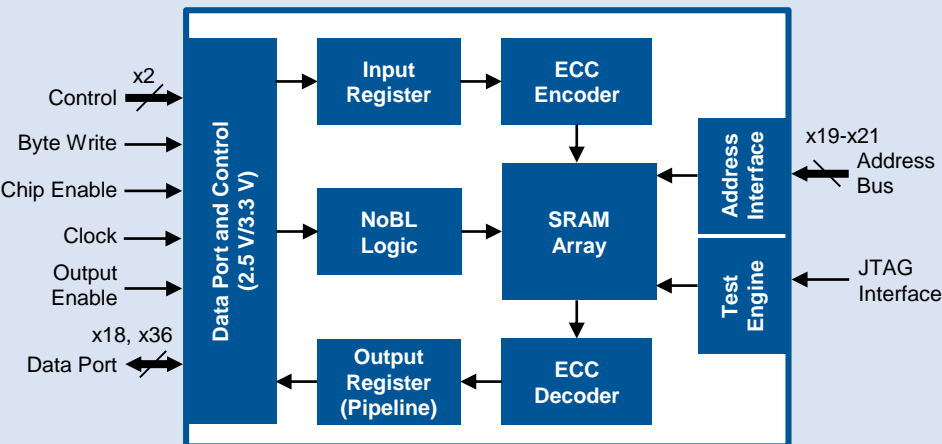
## Features

- **Speed**
  - Available in two modes<sup>2</sup>: Pipeline and Flow-Through
  - No Bus Latency™ (NoBL) architecture for balanced read and write
  - Bus widths: x18, x36
- **Features**
  - ECC to detect and correct single-bit errors
  - Two voltage options: 2.5 V and 3.3 V
  - Industrial and commercial temperature grades
- **Packages**
  - 165-ball BGA
  - 100-pin TQFP

## Collateral

**Datasheets:** [36M NoBL SRAM](#), [18M NoBL SRAM](#)

## NoBL SRAM



## Family Table

Option	Density	MPN	RTR	FIT/Mb <sup>4</sup>
NoBL with On-Chip ECC Pipeline	18Mb 36Mb	CY7C1380/2K CY7C1460/2K	250 MT/s	<0.01
NoBL with On-Chip ECC Flow-Through	18Mb 36Mb	CY7C1381/3K CY7C1461/3K	133 MT/s	<0.01

## Availability

**Production:** Now

<sup>1</sup> Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation

<sup>2</sup> Modes of synchronous SRAM operation that optimize either read latency (Flow-Through) or operating frequency (Pipeline)

<sup>3</sup> Modes of operation in Pipeline mode where the output driver is tri-stated after either a single cycle (SCD) or dual cycle (DCD) of issuing the deselect command

<sup>4</sup> The projected failure rate of a device; one FIT/Mb equals one failure per billion device hours per megabit of data

# Flash Memory Automotive Family

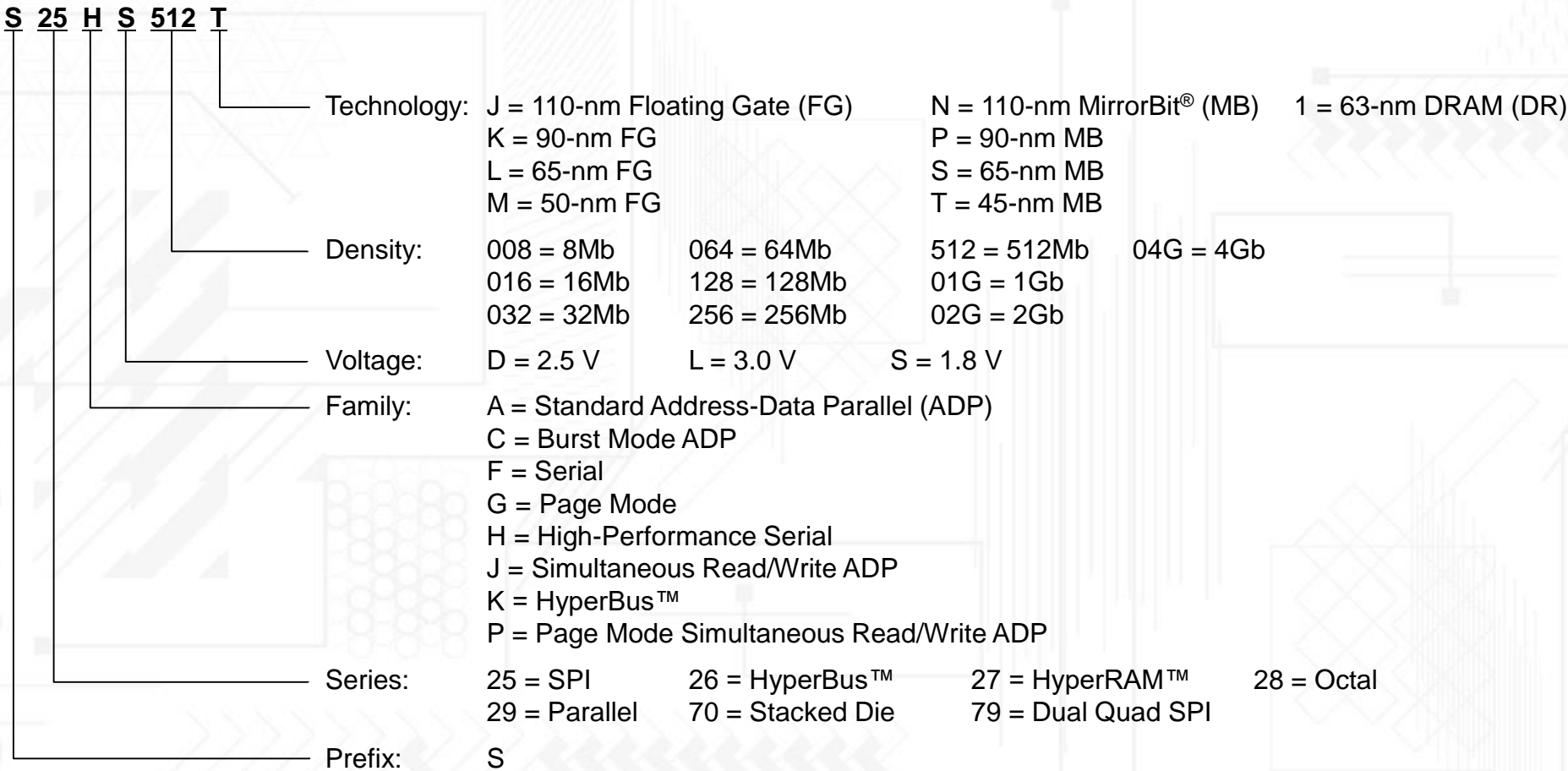


# NOR Flash Memory Automotive Family





# NOR Flash Memory Automotive Family Decoder



# NOR Flash Memory Automotive Product Portfolio: New Products

Family	Interface	Sector Size	Series	Voltage	Densities	Lead	Tech	2018	2019	2020	2021	2022		
Semper™ Flash	Quad SPI	Hybrid	S25HS-T S25HL-T	1.8 V 3.0 V	256Mb–4Gb	512Mb	45nm MB							
	HyperBus™ <sup>1</sup>		S26HS-T S26HL-T	1.8 V 3.0 V	256Mb–4Gb	512Mb	45nm MB							
	Octal <sup>1</sup>		S28HS-T S28HL-T	1.8 V 3.0 V	256Mb–4Gb	512Mb	45nm MB							
QSPI	QSPI	Hybrid	S25FS-S	1.8 V	64Mb–1Gb	-	65nm MB							
			S25FL-S	3.0 V	128Mb–1Gb	-	65nm MB							
			S25FL-L	3.0 V	64–256Mb	-	65nm FG							
Dual Quad SPI	QSPI	Hybrid	S79FS-S S79FL-S	1.8 V 3.0 V	256Mb–1Gb	-	65nm MB							
HyperFlash	HyperBus	Hybrid	S26KS-S S26KL-S	1.8 V 3.0 V	128–512Mb	-	65nm MB							
HyperRAM™	HyperBus	N/A	S27KS-1 S27KL-1	1.8 V 3.0 V	64–256Mb	-	63nm DR							
Parallel	Parallel	Hybrid	S29GL-T	3.0V	512Mb–2Gb	-	45nm MB							

<sup>1</sup> JEDEC xSPI Compliant

Concept Samples Production EOL

# x8 Memory Automotive Roadmap

Product Family	Density	(Prod <sup>1</sup> ) [EOL]	2018				2019				2020				2021				2022				2023				2024			
			Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
S28HS-T <sup>2</sup> (1.8 V) S28HL-T <sup>2</sup> (3.0 V) Semper™ Flash with Octal Interface 45-nm MB <sup>3</sup>	4Gb <sup>3</sup> 2Gb <sup>3</sup> 1Gb 512Mb 256Mb	(TBD) (TBD) (Q3'19) (Q1'19) (Q3'20)																												
S26HS-T <sup>2</sup> (1.8 V) S26HL-T <sup>2</sup> (3.0 V) Semper Flash with HyperBus™ Interface 45-nm MB <sup>3</sup>	4Gb <sup>3</sup> 2Gb <sup>3</sup> 1Gb 512Mb 256Mb	(TBD) (TBD) (Q3'19) (Q1'19) (Q3'20)																												
S26KS-S (1.8 V) S26KL-S (3.0 V) HyperFlash 65-nm MB <sup>3</sup>	512Mb 256Mb 128Mb																													
S79FS-S (1.8 V) S79FL-S (3.0 V) QSPI 65-nm MB <sup>3</sup>	1Gb <sup>5</sup> 512Mb <sup>5</sup> 256Mb <sup>5</sup>																													
S27KS-1 (1.8 V) S27KL-1 (3.0 V) HyperRAM 63-nm DRAM	256Mb <sup>6</sup> 128Mb <sup>6</sup> 64Mb	(TBD)																												

<sup>1</sup> AEC-Q100

<sup>2</sup> JEDEC xSPI Compliant

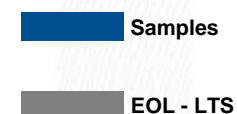
<sup>3</sup> Hybrid Sector

<sup>4</sup> Stacked Die

<sup>5</sup> S79 Series (stacked die)

<sup>6</sup> S70 series (stacked die)

Products supported by  
Longevity Program unless noted



# x8 Serial Memory Automotive Portfolio

	HyperRAM™ S27KL-1 63-nm DR, 3.0 V	HyperRAM S27KS-1 63-nm DR, 1.8 V	Dual Quad SPI S79FL-S <sup>1, 2</sup> 65-nm MB, 3.0 V	HyperFlash S26KL-S <sup>1</sup> 65-nm MB, 3.0 V	Semper™ Flash <sup>3</sup> S26HL-T <sup>1, 4</sup> 45-nm MB, 3.0 V	Semper Flash <sup>5</sup> S28HL-T <sup>1, 4</sup> 45-nm MB, 3.0 V	Dual Quad SPI S79FS-S <sup>1, 2</sup> 65-nm MB, 1.8 V	HyperFlash S26KS-S <sup>1</sup> 65-nm MB, 1.8 V	Semper Flash <sup>3</sup> S26HS-T <sup>1, 4</sup> 45-nm MB, 1.8 V	Semper Flash <sup>5</sup> S28HS-T <sup>1, 4</sup> 45-nm MB, 1.8 V
	<b>Density</b> Initial Access/DDR Clock * Temperature Range		<b>Density (S79)</b> SDR Clock / DDR Clock * Temperature Range							
	All parts supported by Longevity Program unless noted									
≥256Mb					4Gb <sup>7, 8</sup> 80 ns/166 MHz * A, B, M	4Gb <sup>7, 8</sup> 80 ns/166 MHz * A, B, M			4Gb <sup>7, 8</sup> 80 ns/200 MHz * A, B, M	4Gb <sup>7, 8</sup> 80 ns/200 MHz * A, B, M
					2Gb <sup>7, 8</sup> 80 ns/166 MHz * A, B, M	2Gb <sup>7, 8</sup> 80 ns/166 MHz * A, B, M			2Gb <sup>7, 8</sup> 80 ns/200 MHz * A, B, M	2Gb <sup>7, 8</sup> 80 ns/200 MHz * A, B, M
			1Gb 133 MHz/80 MHz * A, B		Q418 1Gb Q319 80 ns/166 MHz * A, B, M	Q418 1Gb Q319 80 ns/166 MHz * A, B, M	1Gb 133 MHz/102 MHz * A, B		Q418 1Gb Q319 80 ns/200 MHz * A, B, M	Q418 1Gb Q319 80 ns/200 MHz * A, B, M
			512Mb 133 MHz/80 MHz * A, B	512Mb 96 ns/166 MHz * A, B, M	Q218 512Mb Q119 80 ns/166 MHz * A, B, M	Q218 512Mb Q119 80 ns/166 MHz * A, B, M	512Mb 133 MHz/80 MHz * A, B	512Mb 96 ns/166 MHz * A, B, M	Q218 512Mb Q119 80 ns/200 MHz * A, B, M	Q218 512Mb Q119 80 ns/200 MHz * A, B, M
64–128Mb	256Mb <sup>6, 7</sup> 36 ns/100 MHz * I, A, V, B	256Mb <sup>6, 7</sup> 36 ns/166 MHz * I, A, V, B	256Mb 133 MHz/80 MHz * A, B	256Mb 96 ns/166 MHz * A, B, M	Q419 256Mb Q320 80 ns/166 MHz * A, B, M	Q419 256Mb Q320 80 ns/166 MHz * A, B, M	256Mb 133 MHz/80 MHz * A, B	256Mb 96 ns/166 MHz * A, B, M	Q419 256Mb Q320 80 ns/200 MHz * A, B, M	Q419 256Mb Q320 80 ns/200 MHz * A, B, M
	128Mb <sup>6</sup> 36 ns/100 MHz * A, B	128Mb <sup>6</sup> 36 ns/166 MHz * A, B		128Mb 96 ns/166 MHz * A, B, M				128Mb 96 ns/166 MHz * A, B, M		
	64Mb 36 ns/100 MHz * A, B	64Mb 36 ns/166 MHz * A, B								

<sup>1</sup> Hybrid Sector

<sup>2</sup> S79 series (stacked die)

<sup>3</sup> With HyperBus™ Interface

<sup>4</sup> JEDEC xSPI Compliant

<sup>5</sup> With Octal Interface

<sup>6</sup> S70 series (stacked die)

<sup>7</sup> Contact Sales

<sup>8</sup> Stacked die

\* A = Automotive, AEC-Q100 Grade 3: -40°C to +85°C

B = Automotive, AEC-Q100 Grade 2: -40°C to +105°C

M = Automotive, AEC-Q100 Grade 1: -40°C to +125°C

Status

Availability

EOL (Last-Time-Ship)

Concept

Development

Sampling

Production

Q418

Q419

Q319

Q320

Q119

Q119

Q320

Q320



# x4 NOR Flash Memory Automotive Roadmap

Product Family	Density	(Prod¹) [EOL]	2018				2019				2020				2021				2022				2023				2024			
			Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
S25HS-T (1.8 V) S25HL-T (3.0 V) Semper™ Flash with QSPI 45-nm MB²	4Gb³ 2Gb³ 1Gb 512Mb 256Mb	(TBD) (TBD) (Q3'19) (Q1'19) (Q3'20)																												
S25FS-S (1.8 V) S25FL-S³ (3.0 V) QSPI 65-nm MB²	1Gb⁶ 512Mb 256Mb 128Mb⁷ 64Mb⁸																													
S25FL-L (3.0 V) QSPI 65-nm FG⁴	256Mb 128Mb 64Mb																													
S25FL-P (3.0 V) QSPI 90-nm MB²	256Mb⁶ 128Mb⁹ 64Mb 32Mb																													
S25FL1-K (3.0 V) QSPI 90-nm FG⁴	64Mb 32Mb 16Mb	[Q1'20] [Q1'20] [Q1'20]																												

¹ AEC-Q100

² Hybrid Sector

³ VIO 1.8V to 3.0V

⁴ Uniform Sector

⁵ Stacked Die

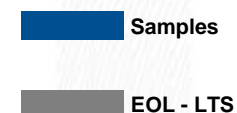
⁶ S70 Series (stacked die)

⁷ S25FL127S and S25FL128S

⁸ FS-S only

⁹ S25FL128P and S25FL129P

Products supported by  
Longevity Program unless noted





# x4 NOR Flash Memory Automotive Portfolio

	QSPI S25FL1-K <sup>1</sup> 90 nm, 3.0 V	QSPI S25FL-P <sup>1</sup> 90 nm, 3.0 V	QSPI S25FL-S <sup>1</sup> 65 nm, 3.0 V	QSPI S25FL-L <sup>2</sup> 65 nm, 3.0 V	Semper™ Flash <sup>3</sup> S25HL-T <sup>1</sup> 45 nm, 3.0 V	QSPI S25FS-S <sup>1</sup> 65 nm, 1.8 V	Semper Flash <sup>3</sup> S25HS-T <sup>1</sup> 45 nm, 1.8 V
≥256Mb	<b>Density (Name)</b> SDR Clock / DDR Clock * Temp Range				<b>4Gb<sup>4</sup></b> 166 MHz / 102 MHz * A, B, M		<b>4Gb<sup>4</sup></b> 166 MHz / 102 MHz * A, B, M
	All parts supported by Longevity Program unless noted				<b>2Gb<sup>4</sup></b> 166 MHz / 102 MHz * A, B, M		<b>2Gb<sup>4</sup></b> 166 MHz / 102 MHz * A, B, M
			<b>1Gb<sup>5</sup></b> 133 MHz / 80 MHz * A, B, M		<b>1Gb</b> 166 MHz / 102 MHz * A, B, M	<b>1Gb<sup>5</sup></b> 133 MHz / 80 MHz * A, B, M	<b>1Gb</b> 166 MHz / 102 MHz * A, B, M
			<b>512Mb</b> 133 MHz / 80 MHz * A, B, M		<b>512Mb</b> 166 MHz / 102 MHz * A, B, M	<b>512Mb</b> 133 MHz / 80 MHz * A, B, M	<b>512Mb</b> 166 MHz / 102 MHz * A, B, M
64–128Mb		<b>256Mb<sup>5</sup></b> 104 MHz / -- * A	<b>256Mb</b> 133 MHz / 80 MHz * A, B, M	<b>256Mb</b> 133 MHz / 66 MHz * A, B, M	<b>512Mb</b> 166 MHz / 102 MHz * A, B, M	<b>256Mb</b> 133 MHz / 80 MHz * A, B, M	<b>512Mb</b> 166 MHz / 102 MHz * A, B, M
		<b>128Mb<sup>6</sup></b> 104 MHz / -- * A, B	<b>128Mb<sup>8</sup></b> 133 MHz / 80 MHz * A, B, M	<b>128Mb</b> 133 MHz / 66 MHz * A, B, M		<b>128Mb</b> 133 MHz / 80 MHz * A, B, M	
		<b>128Mb<sup>7</sup></b> 104 MHz / -- * A, B	<b>128Mb<sup>9</sup></b> 108 MHz / -- * A, B				
	<b>64Mb</b> 108 MHz / -- * A, B	<b>64Mb</b> 104 MHz / -- * A, B		<b>64Mb</b> 108 MHz / 54 MHz * A, B, M		<b>64Mb</b> 133 MHz / 80 MHz * A, B, M	
≤32Mb	<b>32Mb</b> 108 MHz / -- * A, B	<b>32Mb</b> 104 MHz / -- * A, B					
	<b>16Mb</b> 108 MHz / -- * A, B						

<sup>1</sup> Hybrid Sector

<sup>2</sup> Uniform Sector

<sup>3</sup> With QSPI

<sup>4</sup> Stacked die

<sup>5</sup> S70 series (stacked die)

<sup>6</sup> S25FL129P Quad SPI

<sup>7</sup> S25FL128P Dual SPI

<sup>8</sup> S25FL128S 133-MHz SDR / 80-MHz DDR

<sup>9</sup> S25FL127S 108-MHz SDR

\* A = Automotive, AEC-Q100 Grade 3: -40°C to +85°C

B = Automotive, AEC-Q100 Grade 2: -40°C to +105°C

M = Automotive, AEC-Q100 Grade 1: -40°C to +125°C

Status

Availability

EOL (Last-Time-Ship)

Concept

Development

Engineering  
Sampling

AEC-Q100/  
Production

QYYY

QYYY

QYYY



# Parallel and Burst Parallel NOR Flash Memory Automotive Roadmap

Product Family	Density (Prod <sup>1</sup> ) [EOL]	2018				2019				2020				2021				2022				2023				2024			
		Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
S29GL-T <sup>2</sup> (3.0 V) 45-nm MB	2Gb <sup>4</sup> 1Gb 512Mb																												
S29GL-S <sup>2</sup> (3.0 V) 65-nm MB	2Gb <sup>4</sup> 1Gb 512Mb 256Mb 128Mb 64Mb																												
S29GL-N <sup>2</sup> (3.0 V) 110-nm MB	64Mb 32Mb																												
S29PL-J <sup>2,3</sup> (3.0 V) 110-nm FG	128Mb 64Mb 32Mb	[Q1'19]				[Q1'19]				[Q1'19]																			
S29JL-J <sup>3</sup> (3.0 V) 110-nm FG	64Mb 32Mb																												
S29AL-J (3.0 V) 110-nm FG	16M																												
S29AL-J (3.0 V) 110-nm FG	8Mb	[Q1'19]																											
S29AS-J (1.8 V) 110-nm FG	16Mb 8Mb																												
S29CD-J (2.5 V) Burst Parallel 110-nm FG	32Mb 16Mb																												
S29CL-J (3.0 V) Burst Parallel 110-nm FG	32Mb 16Mb																												

<sup>1</sup> AEC-Q100

<sup>2</sup> Supports Page Mode

<sup>3</sup> Supports Simultaneous Read/Write Operation

<sup>4</sup> S70 series (stacked die)

Products supported by  
Longevity Program unless noted

	Concept		Samples
	Production		EOL - LTB
	EOL - LTS		



# Parallel and Burst Parallel NOR Flash Memory Automotive Portfolio

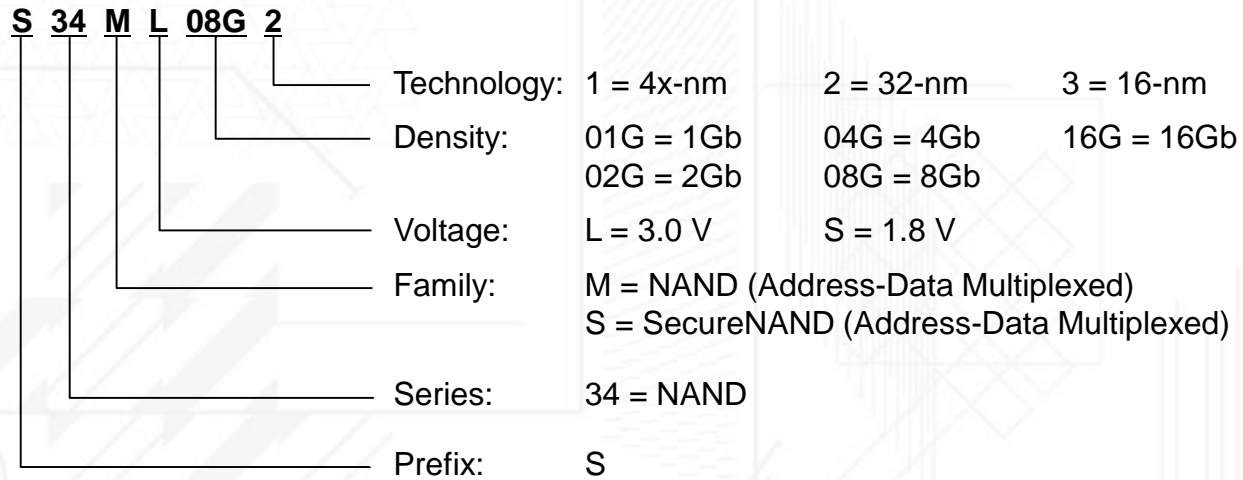
Burst Parallel S29CL-J <sup>1</sup> 110 nm, 3.0 V		Burst Parallel S29CD-J <sup>1</sup> 110 nm, 2.5 V		S29AS-J 110 nm, 1.8 V		S29AL-J 110 nm, 3.0 V		S29JL-J <sup>2</sup> 110 nm, 3.0 V		S29PL-J <sup>2, 3</sup> 110 nm, 3.0 V		S29GL-N <sup>3</sup> 110 nm, 3.0 V		S29GL-S <sup>3</sup> 65 nm, 3.0 V		S29GL-T <sup>3</sup> 45 nm, 3.0 V		
≥256Mb	<b>Density</b> Initial / Page Access * Temp Range														<b>2Gb<sup>4</sup></b> 110 ns / 20 ns * A, B		<b>2Gb<sup>4</sup></b> 110 ns / 20 ns * A, B	
	All parts supported by Longevity Program unless noted														<b>1Gb</b> 100 ns / 15 ns * A, B		<b>1Gb</b> 100 ns / 15 ns * A, B	
															<b>512Mb</b> 100 ns / 15 ns * A, B		<b>512Mb</b> 100 ns / 15 ns * A, B	
															<b>256Mb</b> 90 ns / 15 ns * A, B			
64–128Mb											<b>128Mb</b> 60 ns / 20 ns * A				<b>128Mb</b> 90 ns / 15 ns * A, B			
									<b>64Mb</b> 55 ns / -- * A		<b>64Mb</b> 55 ns / 20 ns * A		<b>64Mb</b> 90 ns / 25 ns * A		<b>64Mb</b> 70 ns / 15 ns * A, B			
≤32Mb	<b>32Mb</b> 54 ns / 75 MHz * A, M, T		<b>32Mb</b> 54 ns / 75 MHz * A, M, T						<b>32Mb</b> 60 ns / -- * A		<b>32Mb</b> 55 ns / 20 ns * A		<b>32Mb</b> 90 ns / 25 ns * A					
	<b>16Mb</b> 54 ns / 66 MHz * A, M, T		<b>16Mb</b> 54 ns / 66 MHz * A, M, T		<b>16Mb</b> 70 ns / -- * A		<b>16Mb</b> 55 ns / -- * A, M											
					<b>8Mb</b> 70 ns / -- * A		<b>8Mb</b> 55 ns / -- * A, M											



# NAND Flash Memory Automotive Family



# NAND Flash Memory Automotive Family Decoder





# SLC NAND Flash Memory Automotive Roadmap

Product Family	Density	(Prod <sup>1</sup> ) [EOL]	2018				2019				2020				2021				2022				2023				2024			
			Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
S34MS-2 (1.8 V) 32-nm SLC ONFI <sup>2</sup> 1.0	16Gb 8Gb 4Gb 2Gb 1Gb																													
S34MS-1 (1.8 V) 4x-nm SLC ONFI <sup>2</sup> 1.0	4Gb 2Gb 1Gb	[Q4'20] [Q4'20] [Q4'20]																												
S34SL-2 (3.0 V) 32-nm SLC ONFI <sup>2</sup> 1.0	4Gb 2Gb 1Gb																													
S34ML-3 (3.0 V) 16-nm SLC ONFI <sup>2</sup> 1.0	16Gb 8Gb 4Gb	(Q4'18) (Q4'18) (Q3'18)																												
S34ML-2 (3.0 V) 32-nm SLC ONFI <sup>2</sup> 1.0	16Gb 8Gb 4Gb 2Gb 1Gb																													
S34ML-1 (3.0 V) 4x-nm SLC ONFI <sup>2</sup> 1.0	8Gb 4Gb 2Gb 1Gb	[Q4'20] [Q4'20] [Q4'20] [Q4'20]																												

<sup>1</sup> AEC-Q100

<sup>2</sup> Open NAND Flash Interface

Products supported by  
Longevity Program unless noted

	Concept		Samples
	Production		EOL - LTB
	EOL - LTS		



# SLC NAND Flash Memory Automotive Portfolio

[illegible]<sup>1</sup> 1-bit error-correcting code (ECC)<sup>2</sup> Open NAND Flash Interface<sup>3</sup> 4-bit error-correcting code (ECC)

<sup>4</sup> SecureNAND™: Cypress's SLC NAND Flash Memory with full-capacity volatile and nonvolatile block protection





<sup>5</sup> Contact Sales

\* I = Industrial: -40°C to +85°C

A = Automotive, AEC-Q100 Grade 3: -40°C to +85°C

V = Industrial-plus: -40°C to +105°C

B = Automotive, AEC-Q100 Grade 2: -40°C to +105°C

	Concept	Development	Engineering Sampling	AEC-Q100/ Production
Status				
Availability			QYY	QYY
EOL (Last-Time-Ship)				QYY



# Flash and RAM Memory Automotive MCP



# Flash and RAM Memory Automotive MCP Decoder

**S 71 K S 512 R D**

RAM Density: A = 16Mb B = 32Mb C = 64Mb D = 128Mb E = 256Mb

Flash Technology: S = 65-nm MirrorBit (MB) T = 45-nm MB

Flash Density: 128 = 128Mb 256 = 256Mb 512 = 512Mb 01G = 1Gb

Voltage: L = 3.0 V S = 1.8 V

Family: H = High-Performance Serial  
K = HyperFlash

Series: 71 = NOR Flash + pSRAM

Prefix: S

# Flash and RAM Memory Automotive MCP Roadmap

Product Family Flash / RAM	Flash / RAM Density	(Prod <sup>1</sup> ) [EOL]	2018				2019				2020				2021				2022				2023				2024			
			Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
S71HS-T (1.8 V) 45-nm Semper™ Flash / HyperRAM™	1Gb / 64Mb 512Mb / 64Mb	(TBD) (TBD)																												
S71KS-S (1.8 V) 65-nm HyperFlash / HyperRAM	512Mb / 64Mb 256Mb / 64Mb 128Mb / 64Mb	(TBD) (TBD) (TBD)																												
S71HL-T (3.0 V) 45-nm Semper Flash / HyperRAM	1Gb / 64Mb 512Mb / 64Mb	(TBD) (TBD)																												
S71KL-S (3.0 V) 65-nm HyperFlash / HyperRAM	512Mb / 64Mb 256Mb / 64Mb 128Mb / 64Mb	(TBD) (TBD) (TBD)																												

<sup>1</sup> AEC-Q100



# Flash and RAM Memory Automotive MCP Portfolio

	S71KL-S 65-nm MB, 3.0 V	S71HL-T 45-nm MB, 3.0 V	S71KS-S 65-nm MB, 1.8 V	S71HS-T 45-nm MB, 1.8 V
≥256Mb	Flash Density RAM Density * Temp Range			
	All parts supported by Longevity Program unless noted	1Gb <sup>1</sup> 64Mb <sup>2</sup> * A, B		1Gb <sup>1</sup> 64Mb <sup>2</sup> * A, B
	512Mb <sup>1</sup> 64Mb <sup>2</sup> * A, B	512Mb <sup>1</sup> 64Mb <sup>2</sup> * A, B	512Mb <sup>1</sup> 64Mb <sup>2</sup> * A, B	512Mb <sup>1</sup> 64Mb <sup>2</sup> * A, B
64–128Mb	256Mb <sup>1</sup> 64Mb <sup>2</sup> * A, B		256Mb <sup>1</sup> 64Mb <sup>2</sup> * A, B	
	128Mb <sup>1</sup> 64Mb <sup>2</sup> * A, B		128Mb <sup>1</sup> 64Mb <sup>2</sup> * A, B	

<sup>1</sup> HyperFlash  
<sup>2</sup> HyperRAM™

\* A = Automotive, AEC-Q100 Grade 3: -40°C to +85°C  
B = Automotive, AEC-Q100 Grade 2: -40°C to +105°C



# x8 NOR Flash Memory Packages

Family	Interface	Series	Density	Device	SOIC-16 300 mil	BGA24 8 x 8 mm 5 x 5 Ball	BGA24 8 x 6 mm 5 x 5 Ball	KGD
Semper™ Flash	HyperBus™	HS-T	512Mb	S26HS512T & S28HS512T			UD	CF
			1Gb	S26HS01GT & S28HS01GT		UD		CF
			2Gb	S26HS02GT & S28HS02GT		CF		
			4Gb	S26HS04GT & S28HS04GT		CF		
		HL-T	512Mb	S26HL512T & S28HL512T			UD	CF
			1Gb	S26HL01GT & S28HL01GT		UD		CF
			2Gb	S26HL02GT & S28HL02GT		CF		
			4Gb	S26HL04GT & S28HL04GT		CF		
HyperFlash		KS-S	128Mb	S26KS128S			✓	CF
			256Mb	S26KS256S			✓	CF
			512Mb	S26KS512S			✓	CF
			1Gb	S70KS01GS			✓	
		KL-S	128Mb	S26KL128S			✓	CF
			256Mb	S26KL256S			✓	CF
			512Mb	S26KL512S			✓	CF
			1Gb	S70KL01GS			✓	
HyperRAM	HyperBus	KS-1	64Mb	S26KS0641			✓	CF
			128Mb	S70KS1281			✓	
			256Mb	S70KS2561			✓	
		KL-1	64Mb	S26KL0641			✓	CF
			128Mb	S70KL1281			✓	
			256Mb	S70KL2561			✓	
Dual Quad SPI	QSPI	FS-S Dual Quad	256Mb	S79FS256S	✓			
			512Mb	S79FS512S	✓			
			1Gb	S79FS01GS			✓	
		FL-S Dual Quad	256Mb	S79FL256S	✓			
			512Mb	S79FL512S	✓			
			1Gb	S79FL01GS			✓	

CF = Contact Factory  
UD = Under Development

# x4 NOR Flash Memory Packages

Family	Interface	Series	Density	Device	SOIC-8 150 mil	SOIC-8 208 mil	SOIC-16 300 mil	WSN 4 x 4 mm	WSN 6 x 5 mm	WSN 8 x 6 mm	BGA24 8 x 8 mm 5 x 5 Ball	BGA24 8 x 6 mm 5 x 5 Ball	BGA24 8 x 6 mm 4 x 6 Ball	KGD		
Semper™ Flash	QSPI	HS-T	512Mb	S25HS512T			CF					UD		CF		
			1Gb	S25HS01GT			CF				UD			CF		
			2Gb	S25HS02GT							CF					
			4Gb	S25HS04GT							CF					
		HL-T	512Mb	S25HL512T			CF					UD		CF		
			1Gb	S25HL01GT			CF				UD			CF		
			2Gb	S25HL02GT							CF					
			4Gb	S25HL04GT							CF					
QSPI		FS-S	64Mb	S25FS064S		✓				✓			✓		✓	
			128Mb	S25FS128S		✓	CF			✓	✓		✓	✓	CF	
			256Mb	S25FS256S			✓				✓		✓	✓	✓	
			512Mb	S25FS512S			✓				✓		✓	✓	CF	
			1Gb	S70FS01GS			✓						✓			
		FL-S	128Mb	S25FL127S		✓	✓			✓				✓	✓	
			128Mb	S25FL128S			✓				✓			✓	✓	
			256Mb	S25FL256S			✓				✓			✓	✓	
			512Mb	S25FL512S			✓							✓	✓	✓
			1Gb	S70FL01GS			✓							✓		
		FL-P	32Mb	S25FL032P		✓	✓			✓		✓		✓	✓	✓
			64Mb	S25FL064P			✓					✓		✓	✓	✓
			128Mb	S25FL128P			✓					✓				
			128Mb	S25FL129P			✓					✓		✓	✓	
			256Mb	S70FL256P			✓					✓		✓		
		FL-L	64Mb	S25FL064L		✓	UD		✓	UD				✓	✓	CF
	128Mb		S25FL128L		✓	UD			✓				✓	✓	CF	
	256Mb		S25FL256L			✓				✓			✓	✓	CF	
	FL1-K	16Mb	S25FL116K	✓	✓				✓				✓	✓	✓	
		32Mb	S25FL132K	✓	✓			✓	✓				✓	✓	✓	
64Mb		S25FL164K		✓	✓			✓				✓	✓	✓		

CF = Contact Factory  
UD = Under Development

# Parallel and Burst Parallel NOR Flash Memory Packages

Series	Density	Device	48-Ball FBGA (0.8-mm pitch)	48-Ball FBGA (0.5-mm pitch)	56-Ball BGA (0.8-mm pitch)	64-Ball BGA (0.8-mm pitch)	64-Ball Fortified BGA (1.0-mm pitch)	48-Pin TSOP	56-Pin TSOP	80-Ball FBGA (1.0-mm pitch)	80-Pin PQFP	KGD
GL-T	512Mb	S29GL512T			✓		✓		✓			
	1Gb	S29GL01GT			✓		✓		✓			
	2Gb	S70GL02GT					✓					
GL-S	64Mb	S29GL064S	✓				✓	✓	✓			
	128Mb	S29GL128S			✓		✓		✓			
	256Mb	S29GL256S			✓		✓		✓			
	512Mb	S29GL512S			✓		✓		✓			
	1Gb	S29GL01GS					✓		✓			
	2Gb	S70GL02GS					✓					
GL-N	32Mb	S29GL032N	✓				✓	✓	✓			
	64Mb	S29GL064N	✓				✓	✓	✓			
PL-J	32Mb	S29PL032J	✓		✓							
	64Mb	S29PL064J	✓		✓							
	128Mb	S29PL127J				✓		✓				
JL-J	32Mb	S29JL032J	✓					✓				
	64Mb	S29JL064J	✓					✓				
AL-J	8Mb	S29AL008J	✓					✓				
	16Mb	S29AL016J	✓				✓	✓				
AS-J	8Mb	S29AS008J	✓					✓				
	16Mb	S29AS016J	✓	✓				✓				
CD-J	16Mb	S29CD016J								✓	✓	✓
	32Mb	S29CD032J								✓	✓	
CL-J	16Mb	S29CL016J								✓	✓	
	32Mb	S29CL032J								✓	✓	

# SLC NAND and SecureNAND Flash Memory Packages

Family	Density	Device	63-Ball BGA (0.8-mm pitch)	67-Ball BGA (0.8-mm pitch)	48-Pin TSOP
MS-2	1Gb	S34MS01G2	✓	✓	✓
	2Gb	S34MS02G2	✓	✓	✓
	4Gb	S34MS04G2	✓		✓
	8Gb	S34MS08G2	✓		
	16Gb	S34MS16G2	✓		
MS-1	1Gb	S34MS01G1	✓		
	2Gb	S34MS02G1	✓		✓
	4Gb	S34MS04G1	✓		✓
ML-3	4Gb	S34ML04G3	✓		✓
	8Gb	S34ML08G3	✓		✓
	16Gb	S34ML16G3	✓		✓
ML-2	1Gb	S34ML01G2	✓	✓	✓
	2Gb	S34ML02G2	✓	✓	✓
	4Gb	S34ML04G2	✓		✓
	8Gb	S34ML08G2	✓		✓
	16Gb	S34ML16G2	✓		✓
ML-1	1Gb	S34ML01G1	✓		✓
	2Gb	S34ML02G1	✓		✓
	4Gb	S34ML04G1	✓		✓
	8Gb	S34ML08G1	✓		✓
SL-2	1Gb	S34SL01G2	✓		
	2Gb	S34SL02G2	✓		
	4Gb	S34SL04G2	✓		



# Flash and RAM Memory MCP Packages

Family	Flash Density	RAM Density	BGA24 8 x 6 mm, 1.0 mm pitch 5 x 5 Ball
S71HS-T	512Mb	64Mb	CF
	1Gb	64Mb	CF
S71KS-S	128Mb	64Mb	✓
	256Mb	64Mb	✓
	512Mb	64Mb	✓
S71HL-T	512Mb	64Mb	CF
	1Gb	64Mb	CF
S71KL-S	128Mb	64Mb	✓
	256Mb	64Mb	✓
	512Mb	64Mb	✓

CF = Contact Factory

# Cypress Roadmap: Automotive Timing Solutions



# Timing Solutions Portfolio

Programmable | High-Performance | EMI Reduction | Automotive

High Performance

Standard Performance

Clock Synthesizers		Oscillators		Clock Buffers	
<div>CY27410 4-PLL; Max Freq: 700 MHz 12 Outputs; Diff<sup>1</sup> &amp; SE<sup>1</sup>; PCIe 3.0 VCXO<sup>2</sup>; EMI<sup>3</sup>; 0.7-ps RMS Jitter<sup>4</sup> 1.8 V/2.5 V/3.3 V; Ind<sup>5</sup>; 48-QFN</div>	<div>CY27430<span>Q318</span> 4-PLL; Max Freq: 700 MHz 8 Outputs; Diff &amp; SE; PCIe 3.0 VCXO; EMI; 0.7-ps RMS Jitter 1.8 V/2.5 V/3.3 V; Auto A<sup>6</sup> S<sup>7</sup>; 48-QFN</div>	<div>CY2941x/2x 1-PLL; Max Freq: 2.1 GHz 1 Output; Diff &amp; SE; 40/100 GbE VCXO; 0.11-ps RMS Jitter; Ind 8-LCC (7 x 5, 5 x 3.2)</div>	<div>CY51x7 1-PLL; Max Freq: 2.1 GHz 1 Output; Diff &amp; SE; 40/100 GbE VCXO; 0.11-ps RMS Jitter; Ind 1.8 V/2.5 V/3.3 V; WAFER/DIE</div>	<div>CY2DPx/CPx Max Freq: 1.5 GHz 2–10 Outputs; LVPECL; 2.5/3.3 V 0.11-ps Additive Jitter<sup>8</sup>; Ind 8/20-TSSOP; 8-SOIC; 32-TQFP</div>	<div>CY2DMx/DLx Max Freq: 1.5 GHz 2–10 Outputs; LVDS, CML; 2.5/3.3 V 0.11-ps Additive Jitter; Ind 8/20-TSSOP; 32-TQFP</div>
<div>CY29430 1-PLL; Max Freq: 2.1 GHz 1 Output; Diff &amp; SE; 40/100 GbE VCXO; 0.11-ps RMS Jitter; Ind 16-QFN</div>		<div>CY2Xx (FleXO™)<span>Q320</span> 1 PLL; Max Freq: 690 MHz 1 Output; LVCMOS, LVDS, LVPECL Freq Margining; 0.6-ps RMS Jitter Ind : 6-LCC (7x5, 5x3.2); 8-TSSOP</div>			
<div>CY254x/CY251x 1–4 PLL; Max Freq: 200 MHz 3–9 Outputs; I<sup>2</sup>C; EMI; Low Power<sup>9</sup> 100-ps CCJ<sup>10</sup>; Ind; 1.8/2.5/3.0/3.3 V 8-SOIC; 8/16/20-TSSOP; 24-QFN</div>	<div>CY229x/CY2238x 3–4 PLL; Max Freq: 166 MHz 3–8 Outputs; CMOS; Low Power 200-ps PPJ<sup>11</sup>; VCXO; Ind; 3.3/5 V 8/16/20-SOIC; 16-TSSOP</div>	<div>CY25701 1-PLL; Max Freq: 166 MHz 1 Output; CMOS; EMI 85-ps CCJ; Ind 3.3 V; 4-LCC (5 x 3.2)</div>	<div>CY2037/ 5037 1-PLL; Max Freq: 133 MHz 1 Output; CMOS 100-ps CCJ; Ind 3.3/5.0 V; WAFER</div>	<div>CY230x/EP0x (Zero Delay) Max Freq: 220 MHz 2–9 Outputs; LVCMOS ; 2.5/3.3/5 V 22-ps CCJ; Ind<sup>5</sup>; Auto A 8/16-SOIC; 16-TSSOP; WAFER</div>	<div>CY230xNZ/ 2994x (Non-Zero Delay) Max Freq: 200 MHz 4–18 Outputs; LVCMOS 100-ps Op-Op Skew; Ind 2.5/3.3 V; 8-TSSOP, 16-SOIC</div>
<div>CY2429x 1-PLL; Max Freq: 200 MHz 2-5 Outputs; HCSL, CMOS; EMI 75-ps CCJ; PCIe 1.1; Ind; Auto A 3.3 V; 16-TSSOP; 32-QFN</div>	<div>CY2239x 3–4 PLL; Max Freq: 400 MHz 5–8 Outputs; LVPECL, CMOS; I<sup>2</sup>C 400-ps PPJ; VCXO; 3.3 V Ind; Auto A E<sup>12</sup>; 16-TSSOP; 32-QFN</div>	<div>CY5077 1-PLLMax Freq: 166 MHz 1 Output; CMOS 75-ps CCJ; Ind 1.8/2.5/3.0/3.3 V; WAFER</div>	<div>CY5057 1-PLL; Max Freq: 170 MHz 1 Output; CMOS; EMI &lt;200-ps CCJ; Ind 3.3/5.0 V; WAFER</div>	<div>CY23FS04/08/FP12 (Zero Delay) Max Freq: 200 MHz 4–12 Outputs; LVCMOS; Fail Safe 200-ps CCJ; Ind; 2.5/3.3 V 16/28-SSOP</div>	<div>CY7B99x (RoboClock™)<span>Q319</span> Max Freq: 200 MHz; 8–13 Outputs Configurable Skew; 2.5/3.3/5.0 V 50-ps CCJ; Ind; 24-SOIC; 32-PLCC 32/44/52/100-TQFP; 100-BGA</div>
<div>CY22800/801/CY2581x 1-PLL; Max Freq: 200 MHz 1-3 Outputs; CMOS; EMI 110-ps CCJ; VCXO; Ind 3.3 V; 8-SOIC; 8-TSSOP</div>	<div>CY22050/150 1-PLL; Max Freq: 200 MHz 6 Outputs; CMOS; I<sup>2</sup>C 250-ps PPJ; Ind<sup>5</sup> 2.5/3.3 V; 16-TSSOP</div>			<div>CY23S0x (Zero Delay) Max Freq: 133 MHz 5–9 Outputs; LVCMOS Spread Aware; 90-ps CCJ; Ind 2.5/3.3 V; 8,16-SOIC; 16-TSSOP</div>	

<sup>1</sup> Differential and single-ended outputs

<sup>2</sup> Voltage-controlled crystal oscillation

<sup>3</sup> Electromagnetic interference reduction using Lexmark profile

<sup>4</sup> Integrated phase noise across 12-kHz to 20-MHz offset

<sup>5</sup> Industrial grade: -40°C to +85°C

<sup>6</sup> AEC-Q100: -40°C to +85°C

<sup>7</sup> AEC-Q100: -40°C to +105°C

<sup>8</sup> Additive RMS phase jitter

<sup>9</sup> Power management options

<sup>10</sup> Cycle-to-cycle jitter

<sup>11</sup> Peak-to-peak period jitter

<sup>12</sup> AEC-Q100: -40°C to +125°C

Status	Concept	Development	Sampling	Production	EOL
Availability					
			QYYY	QYYY	QYYY

# Cypress Roadmap: Automotive PMIC



# Automotive PMIC Family Portfolio

	Typical Input Voltage	Single-channel PMIC	Multi-Channel PMIC		
			Compatible with Cypress Traveo II MCU for Body Control	Compatible with Cypress Traveo/Traveo II MCU for Instrument Cluster	Advanced Driver Assistance System (ADAS)
48 V		<b>Bi-Directional DC/DC</b> Conversion between 48 V and 12 V			
12 V		<b>CYBP211A (Pocono)</b> <sup>Q319</sup> Pre-Boost+Buck Converter <sup>1</sup> SSCG <sup>2</sup> , PG <sup>3</sup> , 12-V V <sub>BAT</sub> <sup>4</sup> 3.3-6.0-V/4-A Output 20-Pin TSSOP		<b>CYBP513A (Misano-L)</b> <sup>Q220</sup> 3x SMPS <sup>5</sup> , PG, SSCG 12-V V <sub>BAT</sub> , 2.0-A Output 40-Pin Side-Wettable <sup>6</sup> QFN	
		<b>S6BP202A/203A (Longbeach)</b> 1xBuck+Boost Converter, PG 12-V V <sub>BAT</sub> , 5-V or 3.3-V/2.4-A Output 16-Pin TSSOP		<b>CYBP511A (Misano)</b> <sup>Q219</sup> 4x SMPS, PG, SSCG 12-V V <sub>BAT</sub> , 2.0-A Output 40-Pin Side-Wettable QFN	
		<b>S6BP201A (Longbeach)</b> 1x Buck+Boost Converter, PG 12-V V <sub>BAT</sub> , 5-V/1-A Output 16-Pin TSSOP	<b>CYBP52xA (Brno)</b> <sup>Q418</sup> Multi-SMPS, PG, SSCG 12-V V <sub>BAT</sub> , 2.0-A Output 32-Pin Side-Wettable QFN	<b>S6BP501A/502A (Monza)</b> 3x SMPS, SSCG, PG 12-V V <sub>BAT</sub> , 2.0-A Output 32-Pin Side-Wettable QFN	<b>Radar ADAS PMIC</b> Multi-SMPS, Low-Noise LDO PG, SSCG 12-V V <sub>BAT</sub> , 4.0-A Output, 40-Pin Side-Wettable QFN
5.0 V/3.3 V		<b>CYBP411A (Iowa)</b> 1xBuck Converter, DVS <sup>7</sup> , PG 3.0-5.5-V Input 10-A Output			<b>S6BP401A (Silverstone)</b> 4x SMPS, 2x LDO, WDT <sup>8</sup> , PG 5-V Input, 3.0-A Output 40-Pin QFN
Market Segment					

<sup>1</sup> A general-purpose regulator IC that integrates power MOSFETs

<sup>2</sup> Spread-spectrum clock generator

<sup>3</sup> Power good: An output signal that PMICs provide to signify that the supplied power by PMICs is proper and ready

<sup>4</sup> Battery voltage

<sup>5</sup> Switch-mode power supply: A general-purpose regulator IC that uses a switching circuit to up-convert and/or down-convert a voltage source to a different voltage for powering other ICs

<sup>6</sup> A package whose flanks are processed to improve soldering adherence and to simplify the optical inspection, which follows soldering

<sup>7</sup> Dynamic voltage scaling

<sup>8</sup> Watchdog timer

Status Availability

Concept  Development  Sampling  Production 





# S6BP20x

## One-Channel Buck-Boost Automotive PMIC

### Applications

Instrument clusters, body electronics and ADAS

### Features

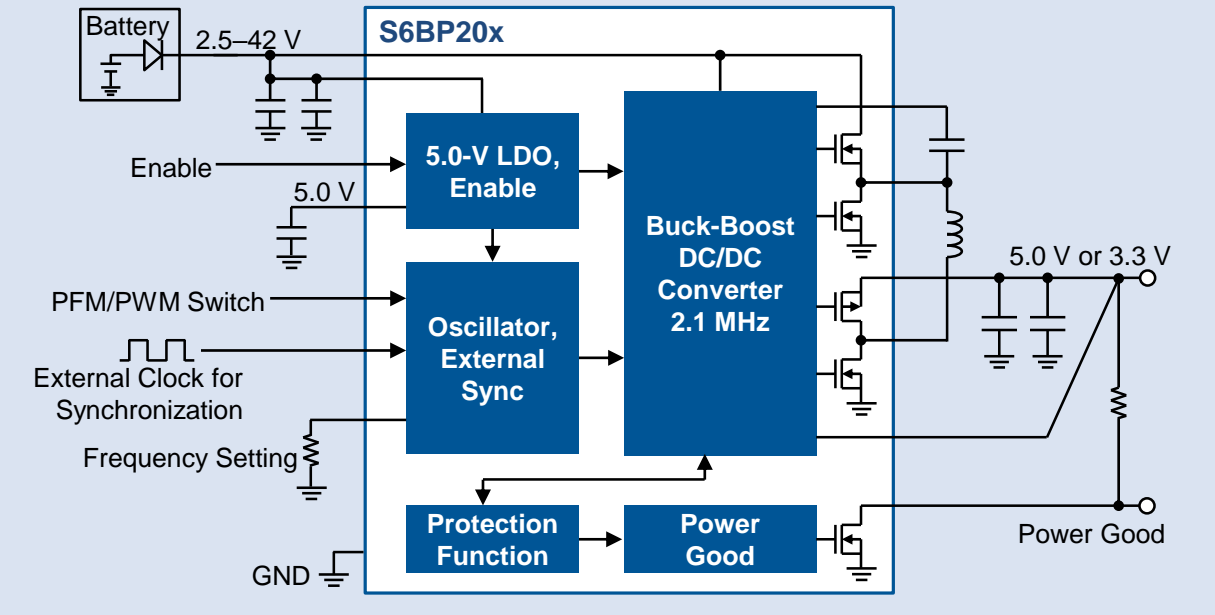
- **1-Channel PMIC:** Synchronous buck-boost converter
- **Wide Input Voltage Range:** 2.5–42 V
- **Low Quiescent Current:** 20  $\mu$ A
- **Programmable Switching Frequency:** 0.2–2.1 MHz
  - Synchronization with external clock from 200 kHz to 400 kHz
  - Autonomous PFM/PWM<sup>1</sup> switching
- **BOM Integration:** Built-in switching transistors
- **System Safety Function<sup>2</sup> Support:**
  - Overvoltage protection (OVP), overcurrent protection (OCP), undervoltage lock-out (UVLO), thermal shutdown (TSD)
  - Window-monitoring voltage supervisors with power good<sup>3</sup> pin
- **Operating Temperature Range:** -40°C to +125°C
- **Package:** 16-pin thermally enhanced TSSOP (5-mm x 6.4-mm)
- **Qualification:** AEC-Q100 Grade-1

### Collateral

**Datasheet:** [S6BP201A](#), [S6BP202A](#) and [S6BP203A](#)

**Evaluation Kit:** [S6BP201A](#), [S6BP202A](#) and [S6BP203A](#)

### S6BP20x: One-Channel Buck-Boost Automotive PMIC



### Family Table

Output Voltage <sup>4</sup>	Max. Output Current	MPN	UVP/OVP Threshold
5.0–5.2 V	1.0 A	S6BP201A	±4.5%
5.0–5.2 V	2.4 A	S6BP202A	±4.5%, ±8.0%
3.3 V	2.4 A	S6BP203A	±8.0%

### Availability

**Sampling:** Now    **Production:** Now

<sup>1</sup> Pulse-frequency modulation/pulse-width modulation

<sup>2</sup> A set of system functions that protect ECUs from damage and/or from generating erroneous results during abnormal power supply conditions

<sup>3</sup> An output signal that PMICs provide to signify that the supplied power by PMICs is proper and ready

<sup>4</sup> S6BP201A and S6BP202A have factory-selectable options of output voltage, power-on-reset time, UVP/OVP threshold, and SYNC Function



# S6BP50x

## Three-Channel Automotive PMIC

### Applications

Low-end to mid-range hybrid automotive cluster systems

### Features

- **3-Channels:** Buck controller with load switch, boost converter, buck converter
- **Wide Range Input:** 2.5-42 V
- **Low Quiescent Current:** 15  $\mu$ A
- **High Switching Frequency:**
  - Boost converter and buck converter: 2.1 MHz
  - Built-in spread-spectrum clock generator (SSCG)
  - Synchronization with external clock from 1.8–2.4 MHz
- **System Safety Function<sup>1</sup> Support:**
  - Overvoltage protection (OVP), overcurrent protection (OCP), undervoltage lock-out (UVLO), thermal shutdown (TSD)
  - Thermal warning
  - Window-monitoring voltage supervisors with independent power good<sup>2</sup> pins
- **Operating Temperature Range:** -40°C to +105°C
- **Package:** 32-pin thermally enhanced side-wettable<sup>3</sup> QFN (5-mm x 5-mm)
- **Qualification:** AEC-Q100 Grade-2

### Collateral

**Preliminary Datasheet:** [S6BP501A/S6BP502A](#)

**Evaluation Kit:** [S6SBP501A00VA1001/S6SBP502A00VA1001](#)

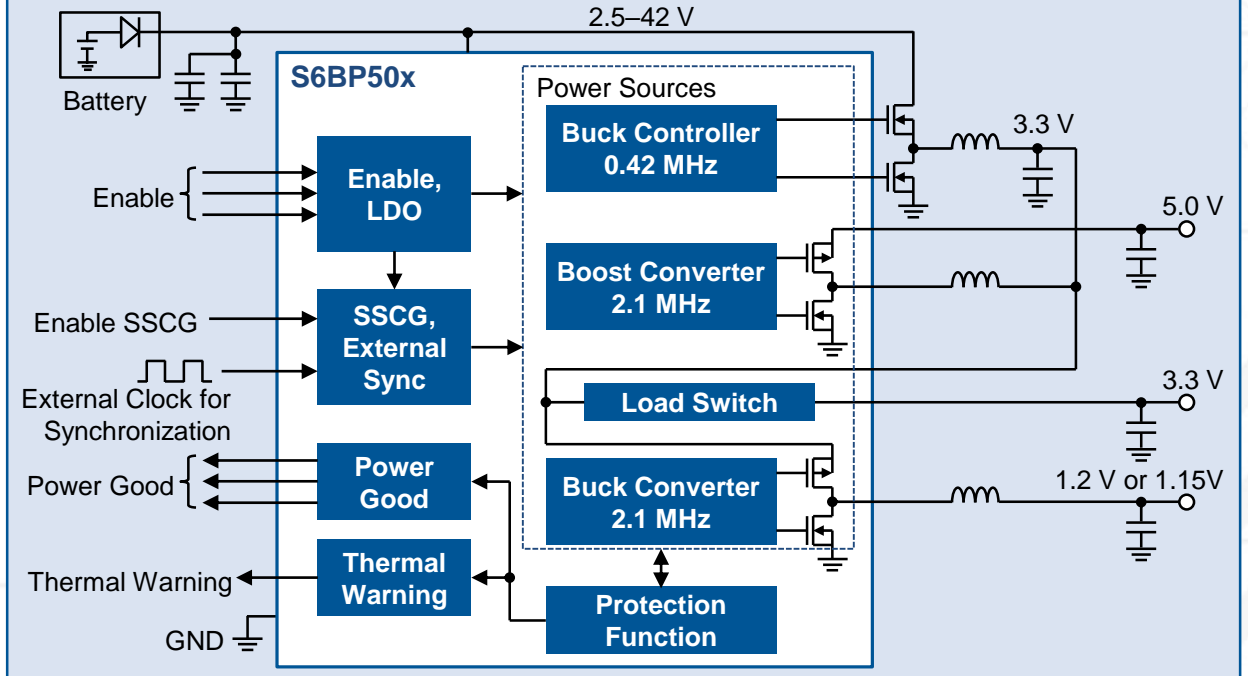
<sup>1</sup> A set of system functions that protect ECUs from damage and/or from generating erroneous results during abnormal power supply conditions

<sup>2</sup> An output signal that PMICs provide to signify that the supplied power by PMICs is proper and ready

<sup>3</sup> A package whose flanks are processed to improve soldering adherence and to simplify the optical inspection, which follows soldering

<sup>4</sup> Output voltages are finely adjustable with external resistive dividers

### S6BP50x: Three-Channel Automotive PMIC



### Family Table

Buck Converter Output Specification <sup>4</sup>	MPN	Buck Controller Output Specification	Boost Converter Output Specification
1.15 V, 1.4 A	S6BP501A	3.3 V, 1.6 A	5.0 V, 1.3 A
1.2 V, 2.0 A	S6BP502A	3.3 V, 1.9 A	5.0 V, 1.3 A

### Availability

**Sampling:** Now

**Production:** Now

# S6BP401A

## Six-Channel Automotive PMIC

### Applications

Advanced driver assistance systems (ADAS), security camera systems

### Features

- **6-Channel PMIC:** 4-channel buck converters, 2-channel LDOs
- **Input Voltage Range:** 4.5–5.5 V
  - Input voltage for LDO: 1.62–5.5 V
- **High Switching Frequency:** 2.1 MHz
  - Synchronization with external clock from 1.8–2.4 MHz
- **BOM Integration:**
  - Switching transistors, voltage setting resistors, and compensation circuitry
- **System Safety Function<sup>1</sup> Support:**
  - Overvoltage protection (OVP), overcurrent protection (OCP), undervoltage lock-out (UVLO), thermal shutdown (TSD)
  - Window-monitoring voltage supervisors with independent power good<sup>2</sup> pins
  - Built-in windowed watchdog timer (WDT)
  - Independent enable pins
- **Operating Temperature Range:** -40°C to +125°C
- **Package and Qualification:** 40-pin QFN (6-mm x 6-mm), AEC-Q100 Grade-1

### Collateral

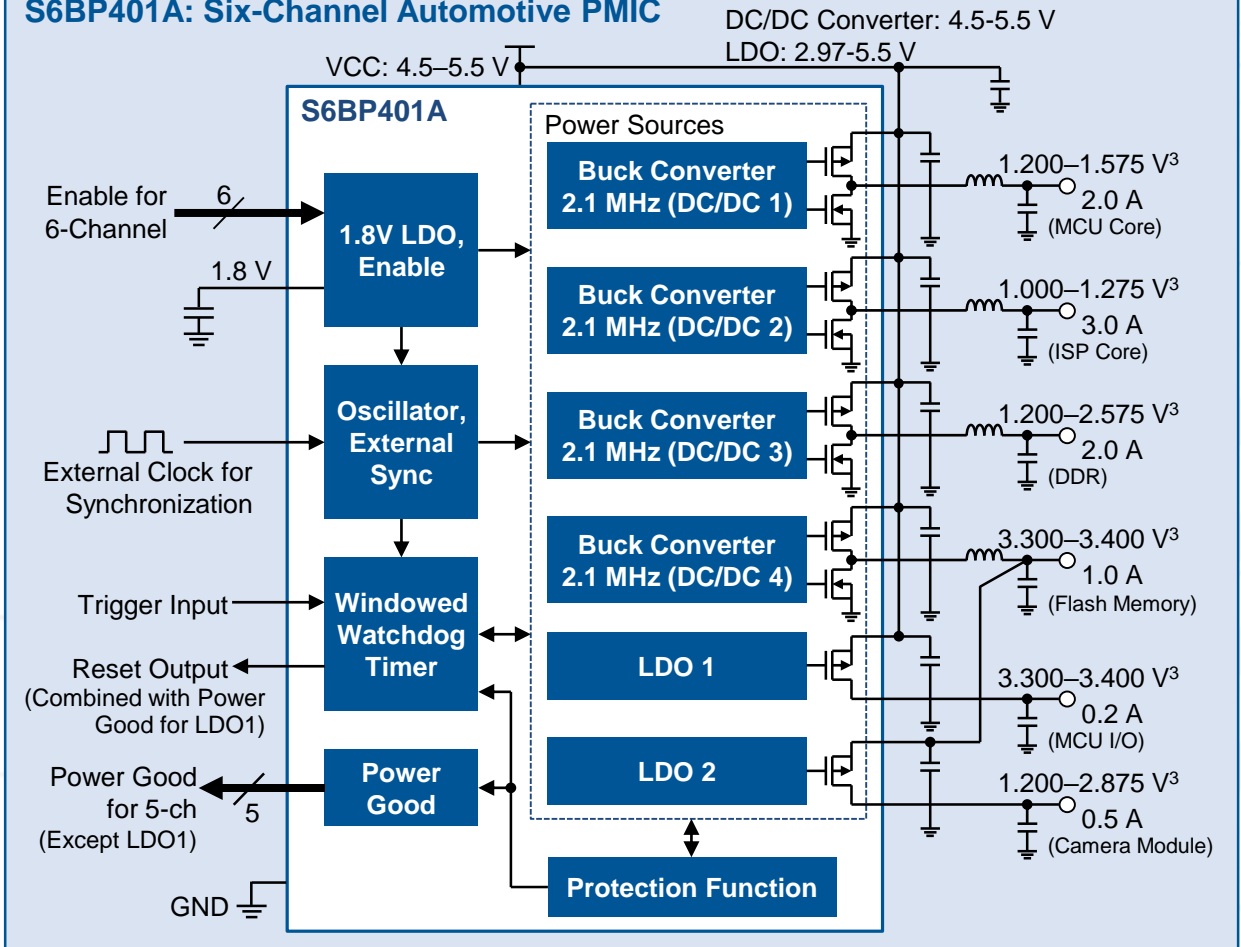
**Datasheet:** [S6BP401A](#)  
**Evaluation Kit:** [S6SBP401AJ0SA1001](#), [S6SBP401AM2SA1001](#)

<sup>1</sup> A set of system functions that protect ECUs from damage and/or from generating erroneous results during abnormal power supply conditions

<sup>2</sup> An output signal that PMICs provide to signify that the supplied power by PMICs is proper and ready

<sup>3</sup> S6BP401A has factory-selectable options of output voltage for each channel

### S6BP401A: Six-Channel Automotive PMIC



### Availability

**Sampling:** Now    **Production:** Now

