PolarFire Design Document

Base Design

rev 1.00.000

1. Overview

The goal of this Base Mi-V design is to provide a starting point to develop complex designs that will use LEDs, pushbuttons and the DDR3 memory.

Some features of the Avalanche board are included in this design: UART, user LEDs, user pushbuttons (BasicIO interface) and the DDR3 interface. On the RISC-V side: Interrupts (External IRQs), DDR3 test routines, GPIO and UART configuration and management and access to different memory devices.

2. Description

Platform	Avalanche Development Board
Target	PolarFire MPF300TS-1FGC484
Clock(s)	Main: 133 MHz MMIO Sub-system: 133 MHz
FPGA usage	Around 32.7k LE (10.9%)

Steps to run the design

1. Once the Avalanche board is powered up and USB connected, configure your preferred terminal software (ie PuTTY) on your host PC for serial communication (115200 / 8 / 1 / No parity / No Flow Control) with the FPGA. You can press the Reset pushbutton to see the demo Welcome message on the terminal.
2. The heartbeat will be visible on LED1 green, the DDR3 test result.

3. Functions

Device	Description
Basic IO - UART	- Echo info from the design power-up.
System Timer	- Generate a 0.5 Hz heartbeat on the green LED 2.
Basic IO - Pushbutton #1	- Upon depression, toggle LED1 green
Basic IO - Pushbutton #2	- Upon depression, toggle LED1 red
Basic IO - LEDs	- After power-up, red LED1 active when the DDR3 test has failed - After power-up, green LED1 active when the DDR3 test is successful.

4. FPGA Blocks Configuration

Device	Configuration
BasicIO_Interface	UART for Terminal communication configured through Mi-V code (115200 / 8 / 1 / No parity / No Flow Control) User pushbutton #1: USER_PB1_IRQ connected to Mi-V External IRQ 30 User pushbutton #2: USER_PB2_IRQ connected to Mi-V External IRQ 29 Other ports pushed as Top Level ports to be mapped on I/O pads.
DDR3_Crtrl	Memory timing used is JEDEC DDR3-1066E (6-6-6) – 4Gb x 16 – CL7 – CWL6

5. Memory Description

Memory Device	Type	Size
Mi-V Boot	LSRAM	128KB (32768 x 32 bits)
Board Memory	DDR3	512MB (256MB x 16 bits)

6. Memory Map

Device	First Address	Last Address
MMIO – BasicIO_Interface	0x7000 0000	0x7000 0FFF
Memory – Mi-V Boot (LSRAM)	0x6000 0000	0x600F FFFF
Memory – Board memory (DDR3)	0x8000 0000	0x8FFF FFFF