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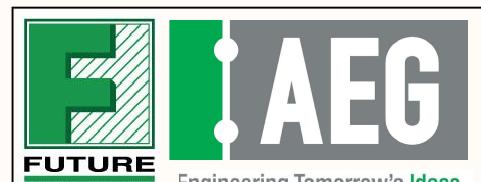
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Checked by H. Letourneau	Approved by M. Bernier

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Project Name
Microsemi_Avalanche Rev 2

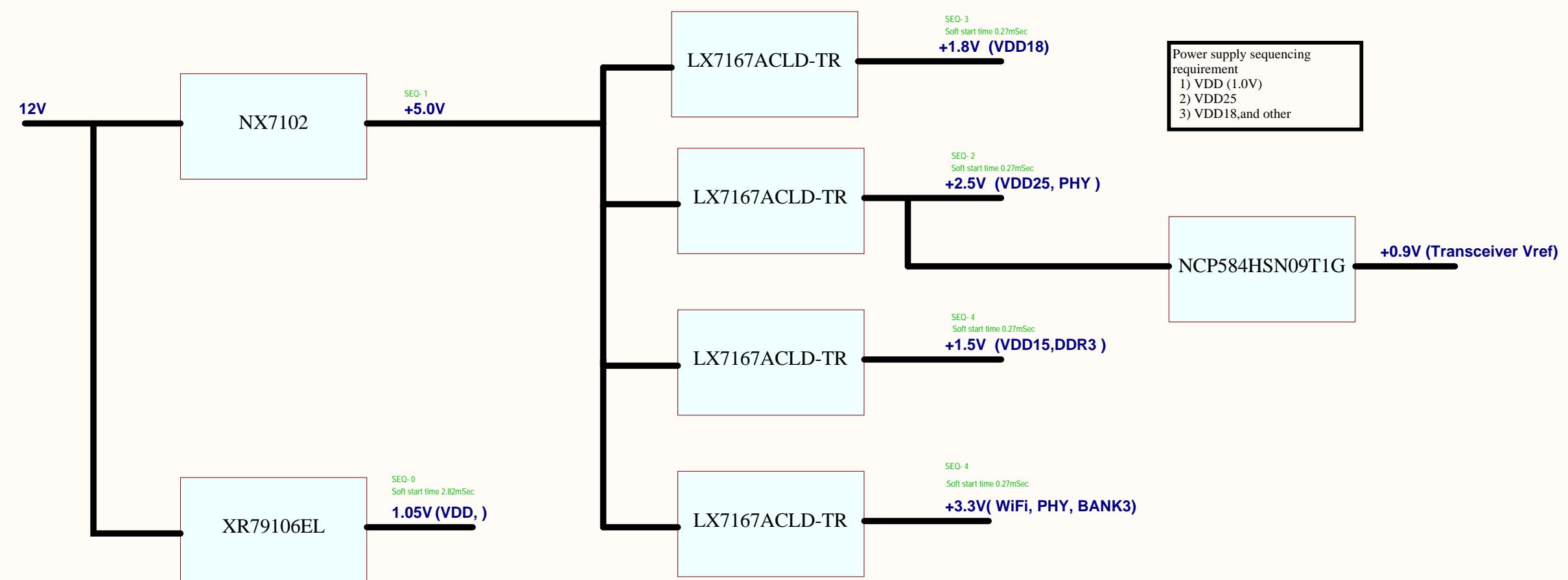
Title
Block Diagram

Size **B** Dwg No. **FEN-412728-SCH-R2**

Rev **2**

Date **12/14/2017** Sheet **1** of **15** Variant: **MCP3903**

Power supply block diagram

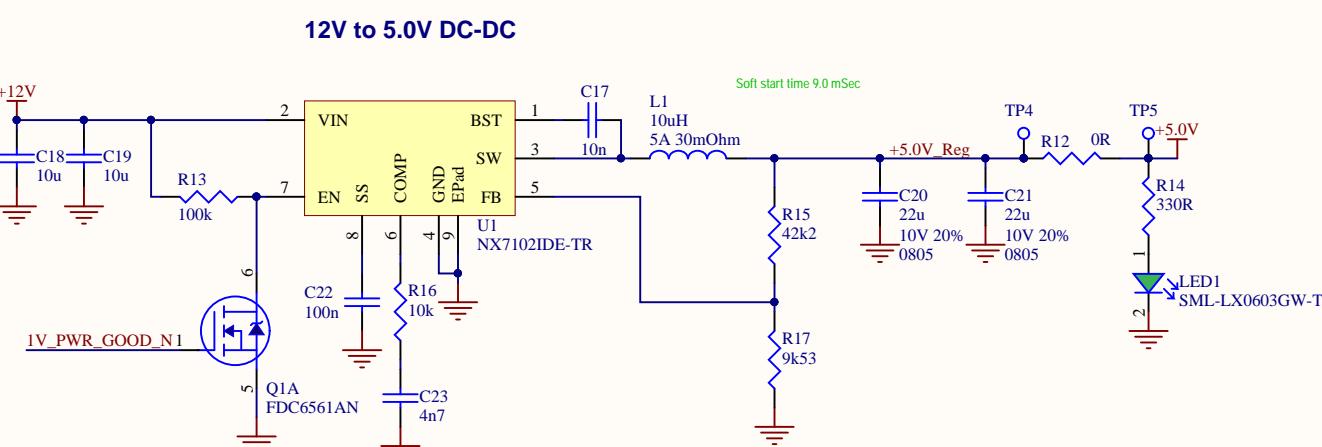
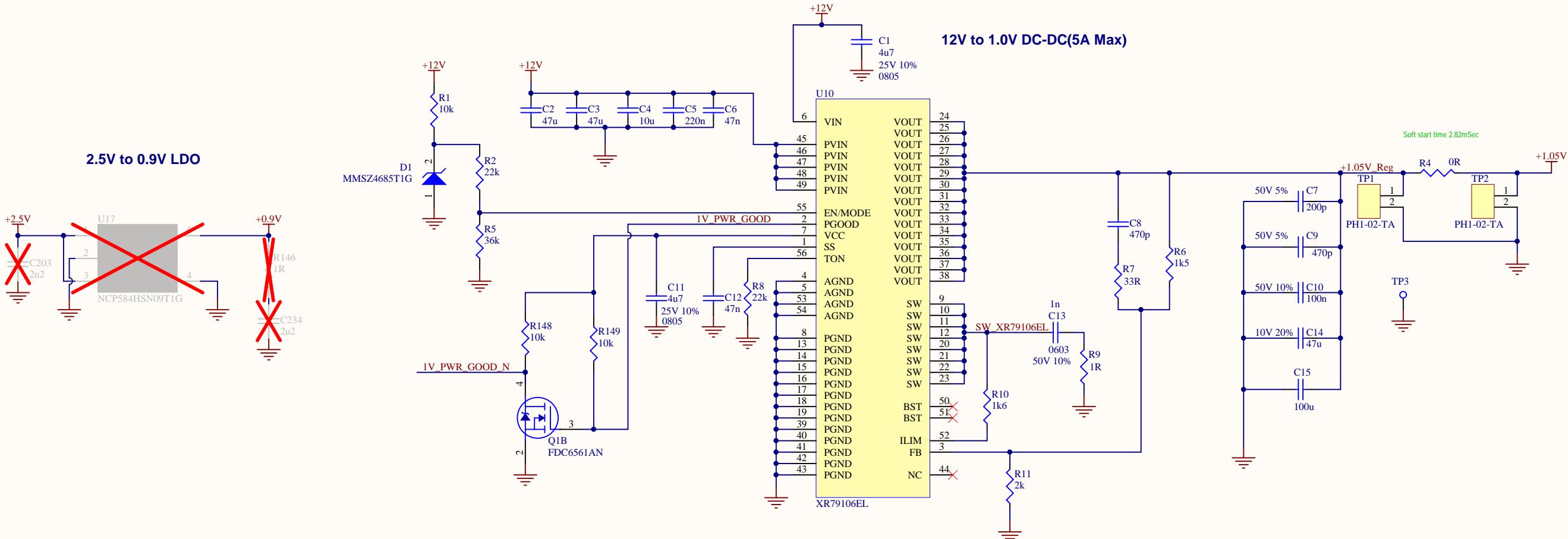


Power supply sequencing requirement
 1) VDD (1.0V)
 2) VDD25
 3) VDD18, and other



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Project Name Microsemi_Avalanche Rev 2		
Title Power supply Block diagram		
Size B Dwg No. FEN-412728-SCH-R2 Rev 2		
Designed by N. Gautam Drawn by D. Ouellette		
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Date 12/6/2017 Sheet 2 of 15 Variant: MCP3903		

Power supply



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Project Name
Microsemi Avalanche Rev 2

Title

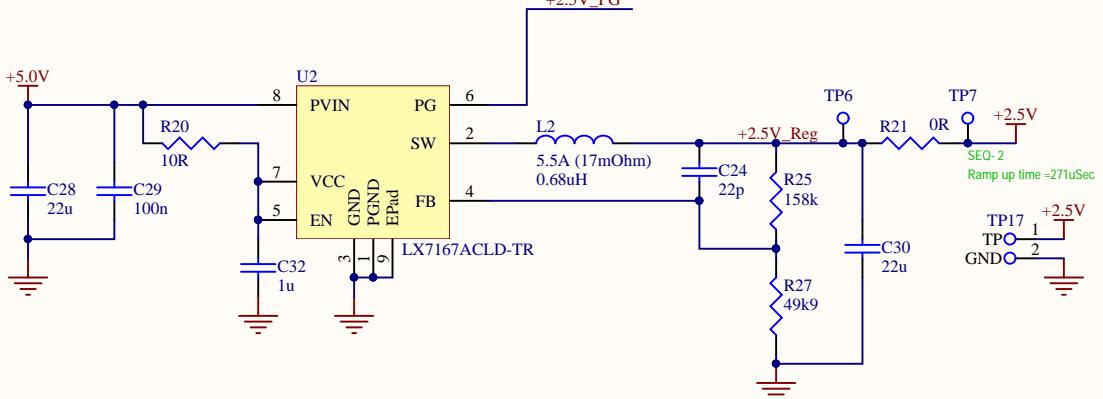
Power supply 1

12/6/2017 3:51:15 MCP2003

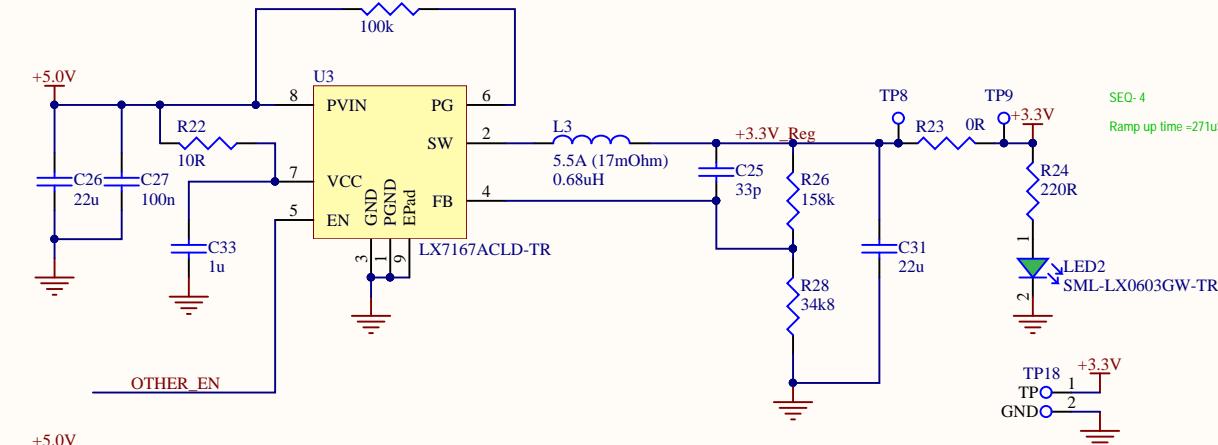
Date 12/6/2017 Sheet 5 OF 15 Variant: MCP5503

Power supply

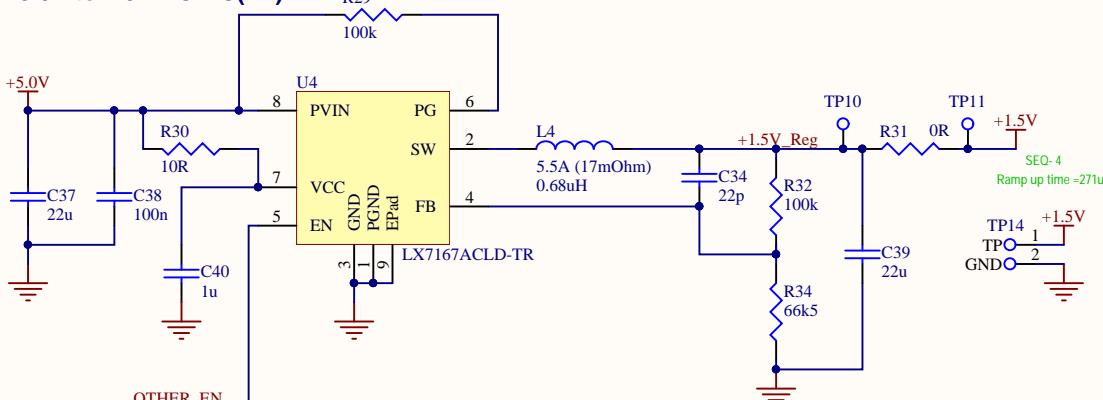
5.0V to 2.5V DC-DC(2A)



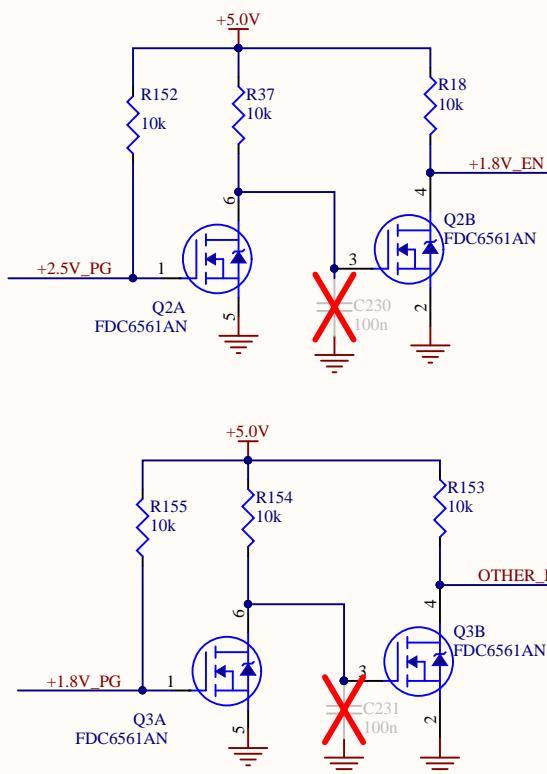
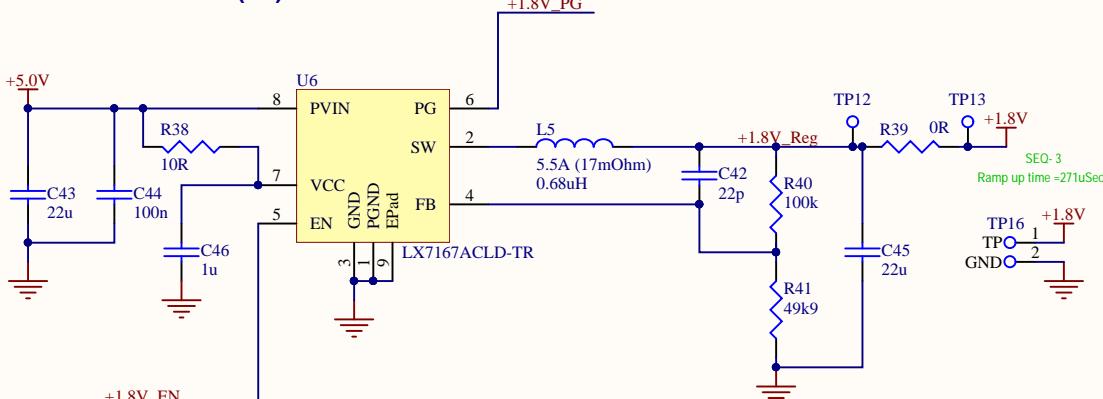
5.0V to 3.3V DC-DC(2A)



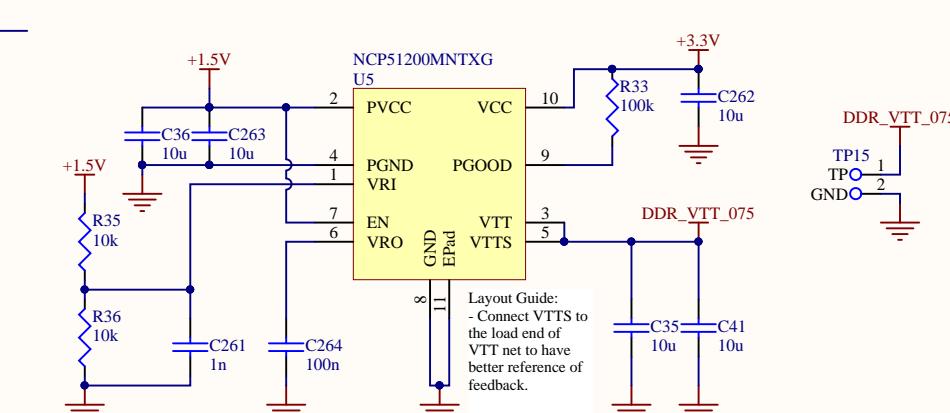
5.0V to 1.5V DC-DC(2A)



5.0V to 1.8V DC-DC(2A)



0.75V for DDR



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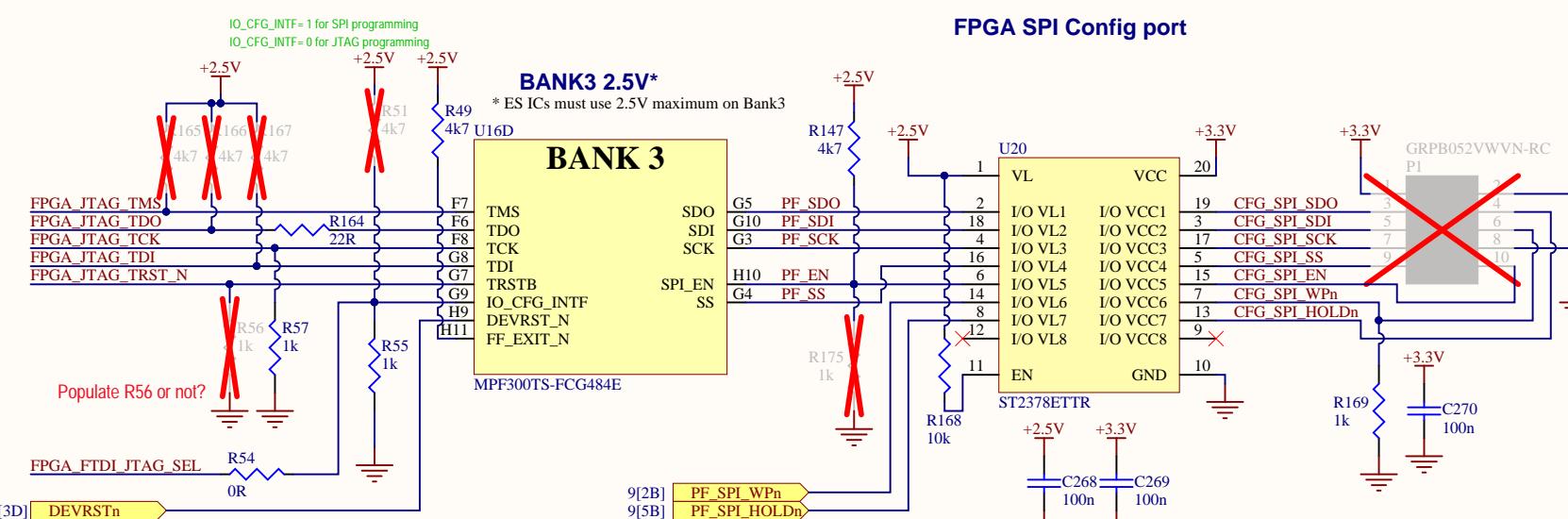
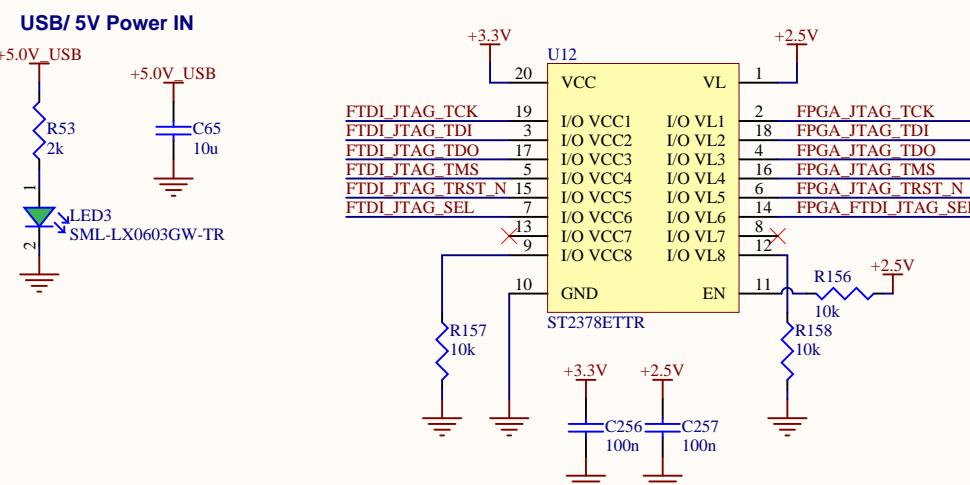
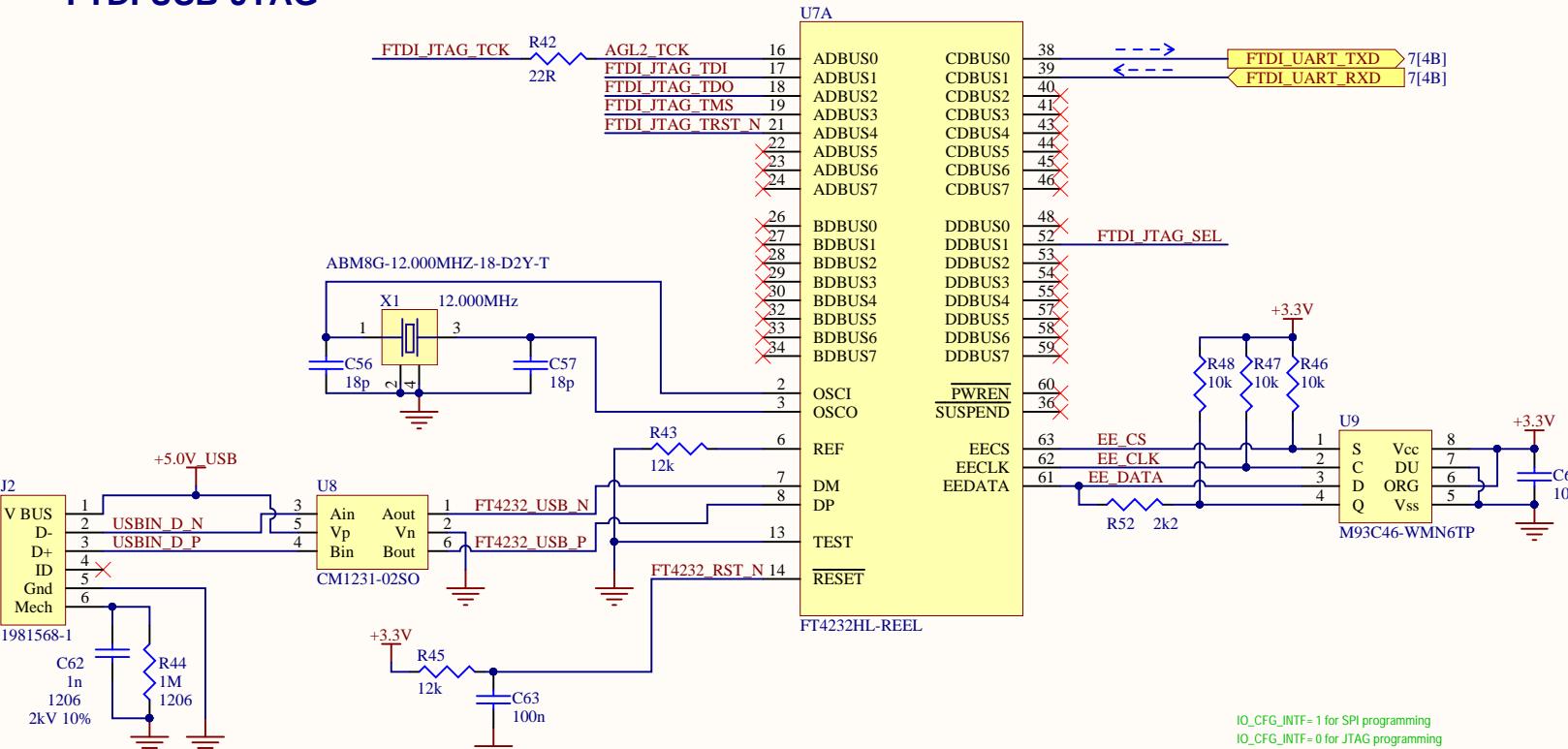
Title
Power Supply 2

Size **B** Dwg No. **FEN-412728-SCH-R2**

Rev **2**

Checked by **H. Letourneau** Approved by **M. Bernier**

Date **12/6/2017** Sheet **4** of **15** Variant: **MCP3903**

FTDI USB-JTAG

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Project Name
Microsemi_Avalanche Rev 2

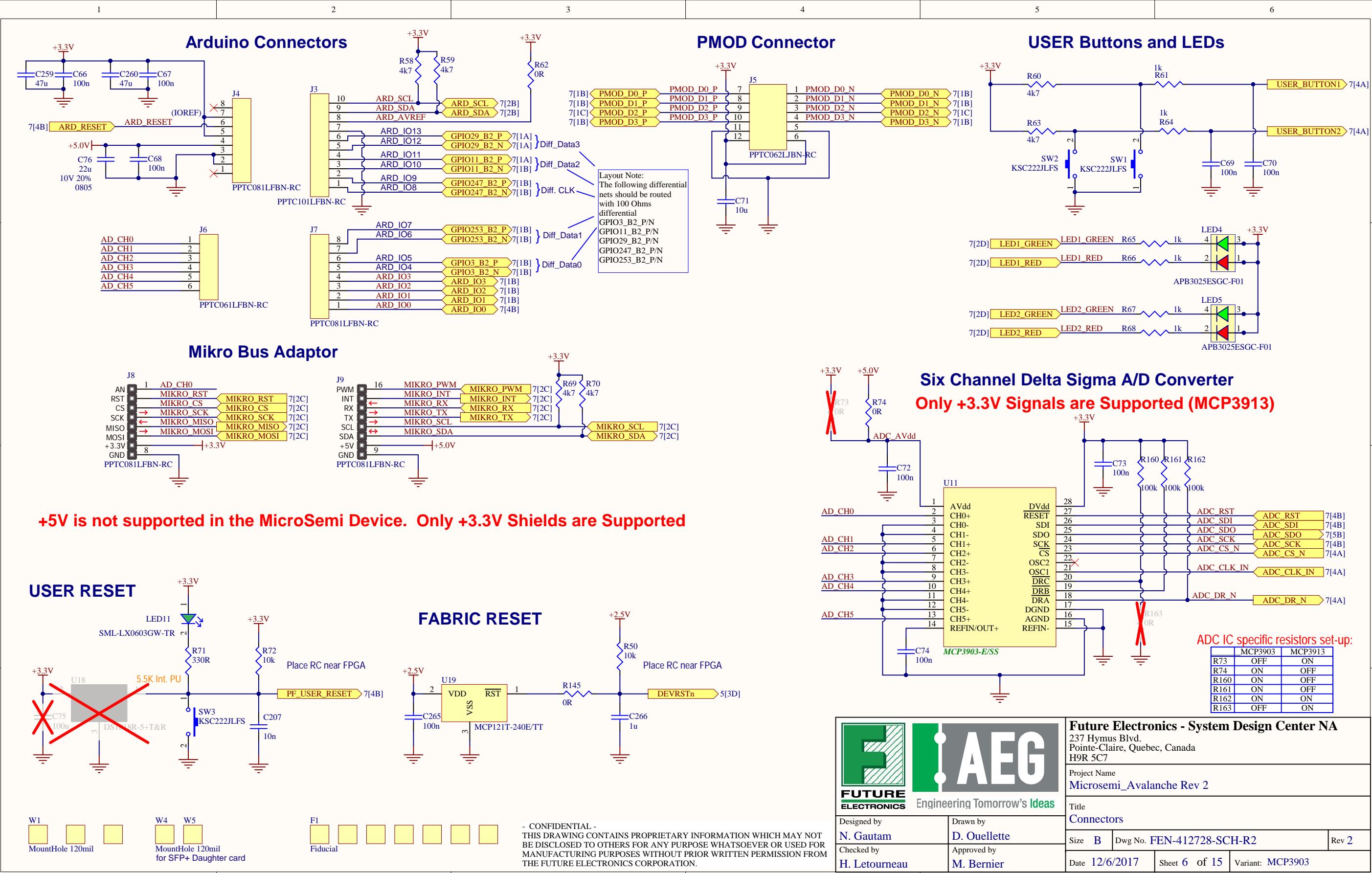
Title

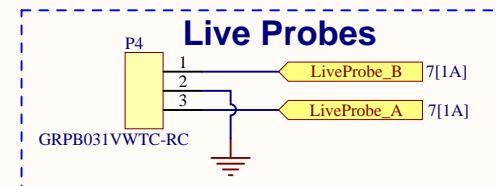
USB - JTAG

Size B Dwg No. FEN-412728-SCH-R2

Rev 2

Date 12/19/2017 Sheet 5 of 15 Variant: MCP3903





Bank - 2 (3.3V)

A
Layout Note:
The Following differential nets
should be routed with 100 Ohms
differential.

Length matching:

Intra-Pair : 10mils

Inter-pairs : 50mils

GPIO3_B2_P/N

GPIO11_B2_P/N

GPIO29_B2_P/N

GPIO247_B2_P/N

GPIO253_B2_P/N

Diff. Pairs

Diff. CLK

7[2A] LiveProbe_A

7[2A] LiveProbe_B

6[2A] GPIO29_B2_P

6[2A] GPIO29_B2_N

6[2A] GPIO11_B2_P

6[2A] GPIO11_B2_N

6[2A] GPIO247_B2_P

6[2A] GPIO247_B2_N

6[2B] GPIO253_B2_P

6[2B] GPIO253_B2_N

6[2B] GPIO3_B2_P

6[2B] GPIO3_B2_N

13[2B] FACT_RST_w

6[2B] ARD_IO3

6[2B] ARD_IO2

6[2B] ARD_IO1

6[3A] PMOD_D1_P

6[3A] PMOD_D1_N

6[3A] PMOD_D0_P

6[3A] PMOD_D0_N

6[4A] PMOD_D2_P

6[4A] PMOD_D2_N

6[3A] PMOD_D3_P

6[4A] PMOD_D3_N

13[4B] RXD_w

6[2A] ARD_SCL

6[2A] ARD_SDA

13[4B] TXD_w

13[4B] RTS_w

6[3A] PMOD_D2_P

6[4A] PMOD_D2_N

13[2B] BT_FREQ_w

13[2B] WAKE_UP_w

6[3B] MIKRO_PWM

6[3B] MIKRO_INT

6[3B] MIKRO_RX

6[3B] MIKRO_TX

6[3B] MIKRO_SCL

6[3B] MIKRO_SDA

6[2B] MIKRO_RST

6[2B] MIKRO_CS

6[2B] MIKRO_SCK

6[2B] MIKRO_MISO

6[2B] MIKRO_MOSI

15[5C] SFP_TXFault

15[5C] SFP_RS

15[5C] SFP_LOS

13[4B] CTS_w

13[4B] DUAL_SW_w

13[4B] DUAL_STAT_w

6[5B] LED1_GREEN

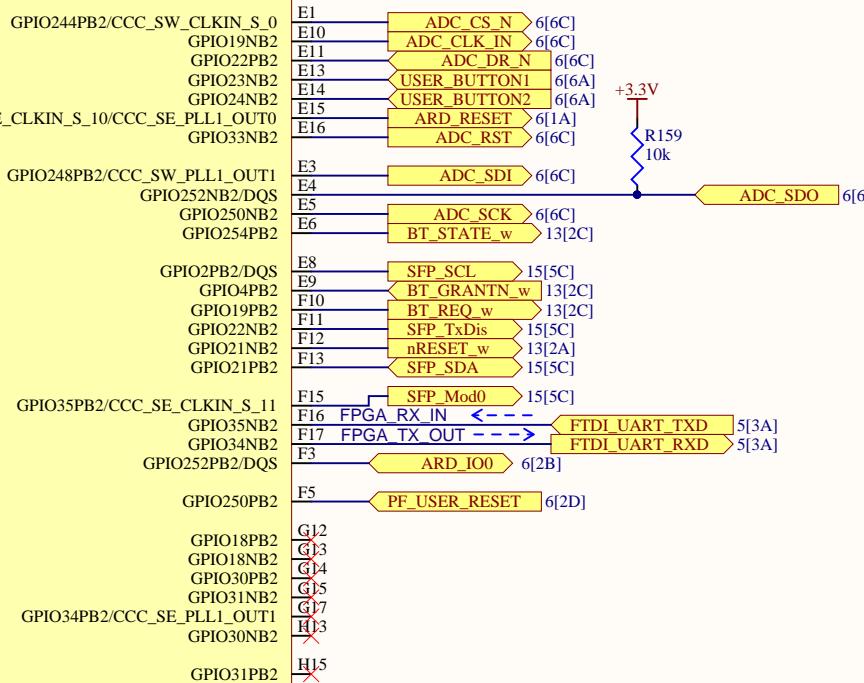
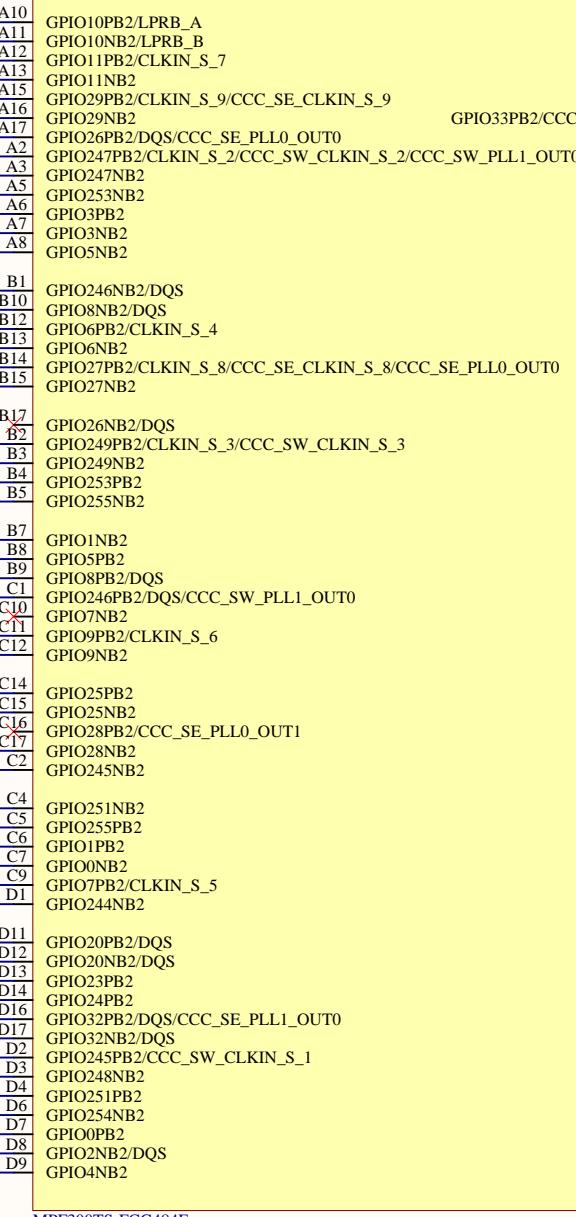
6[5B] LED1_RED

6[5B] LED2_GREEN

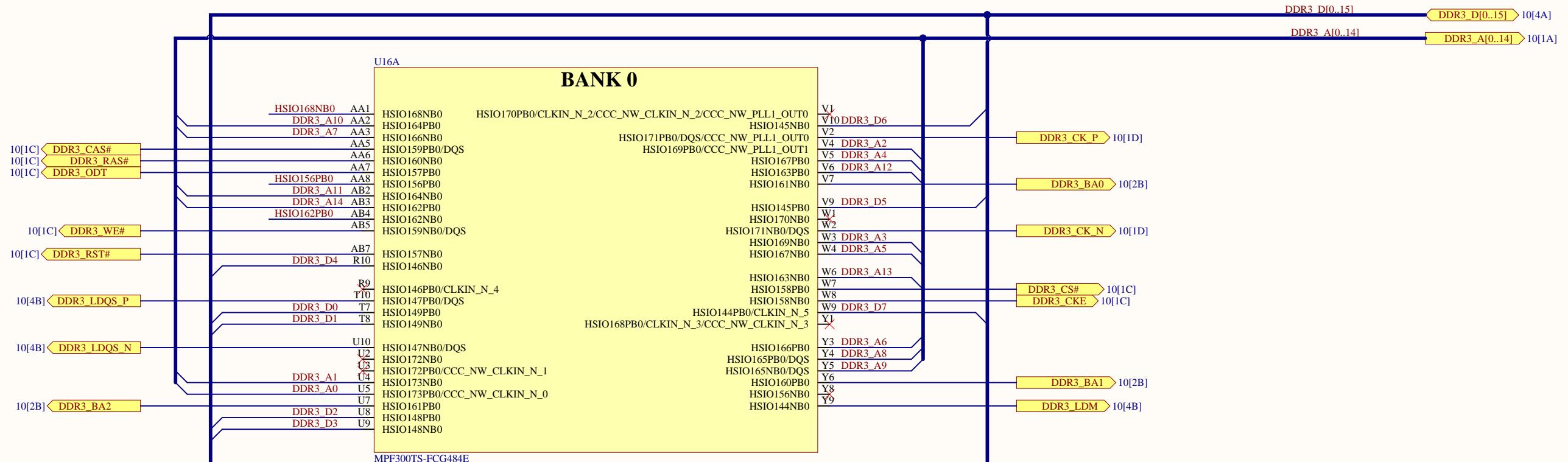
6[5B] LED2_RED

U16C

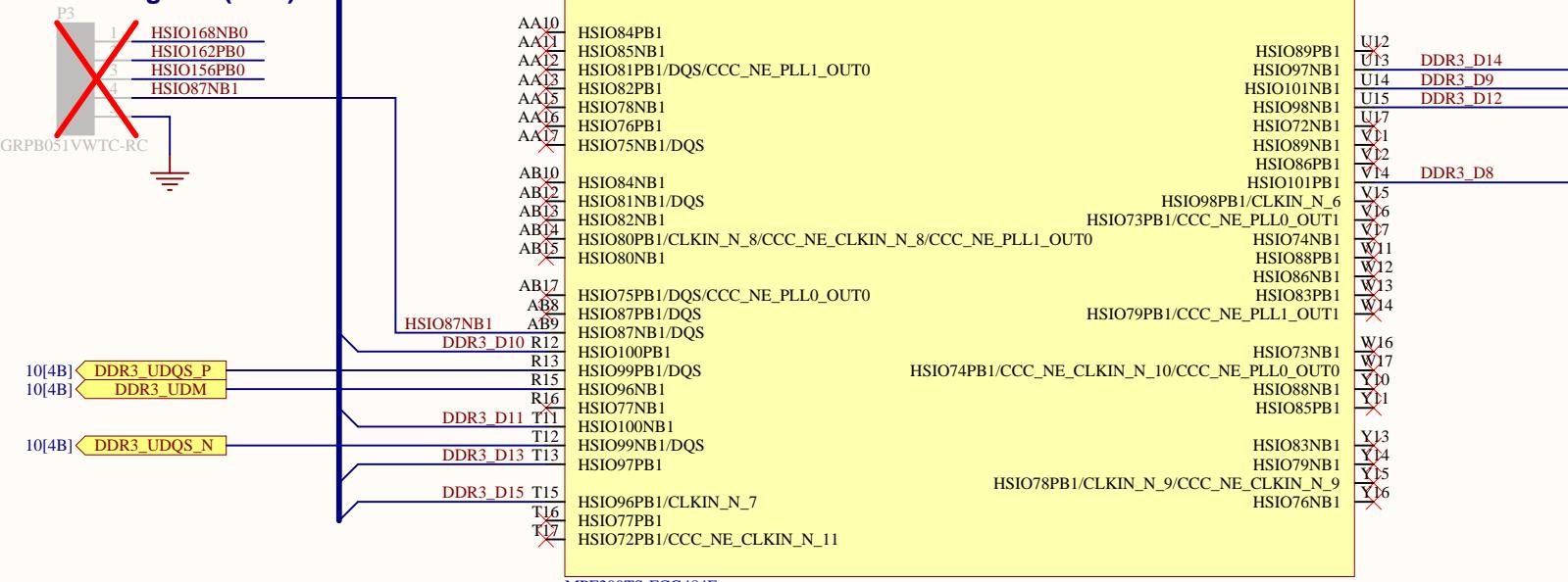
BANK 2



Bank - 0, 1 (1.5V)



Test Signals (1.5V)



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Project Name
Microsemi Avalanche Rev 2

Title

Designed by _____ Drawn by _____

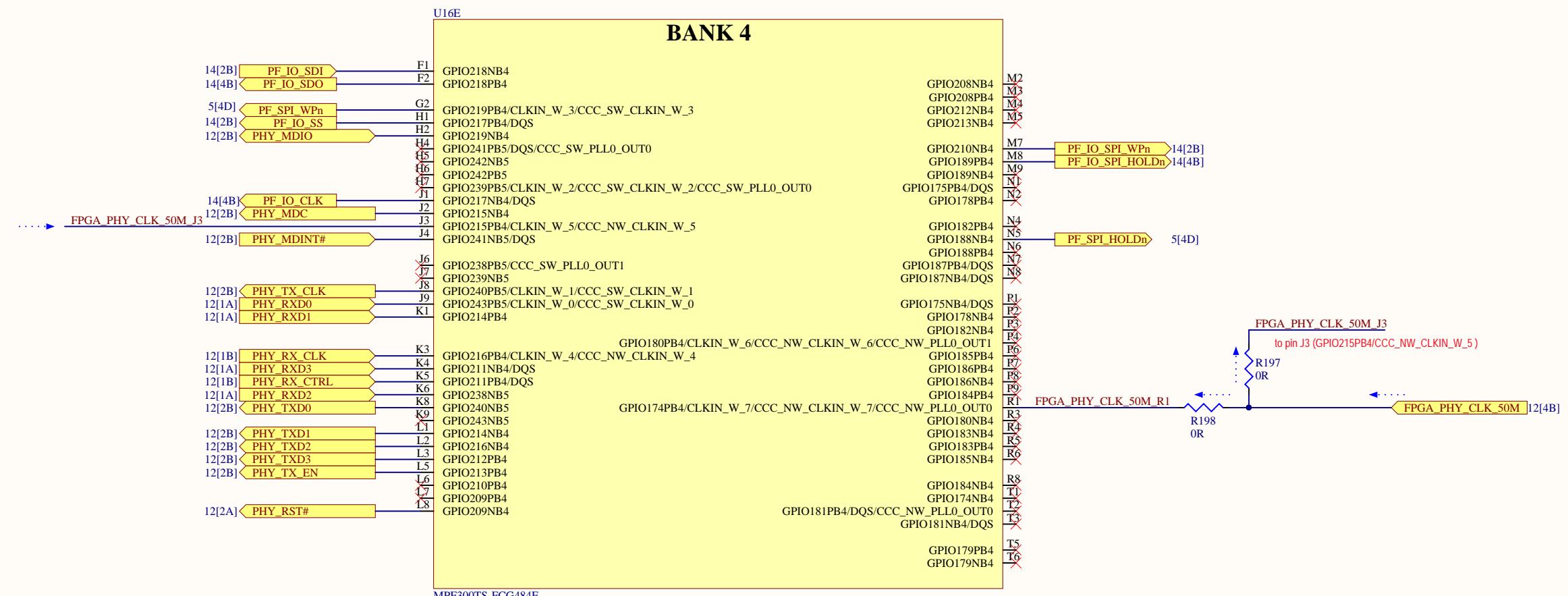
N. Gautam D. Ouellette

Checked by H. J. Approved by M. D.

Page 12/14/2017 | Step 8 of 15 | Version MGR2003

Date 12/14/2017 | Sheet 8 of 15 | Variant: MCP5903

Bank - 4 (2.5V)



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Project Name
Microsemi_Avalanche Rev 2

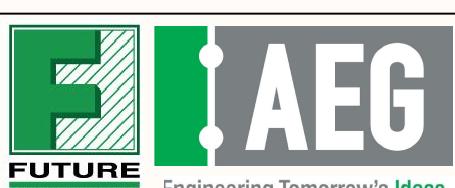
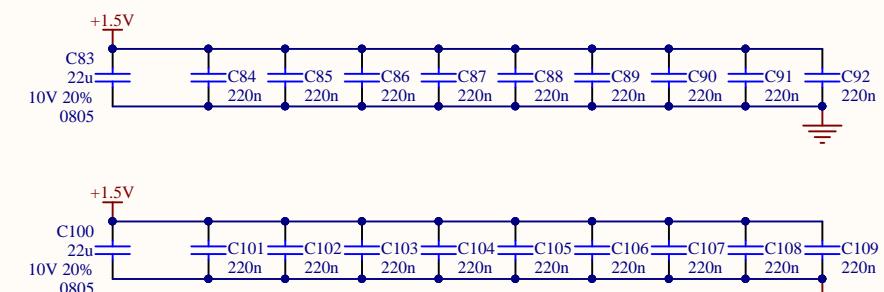
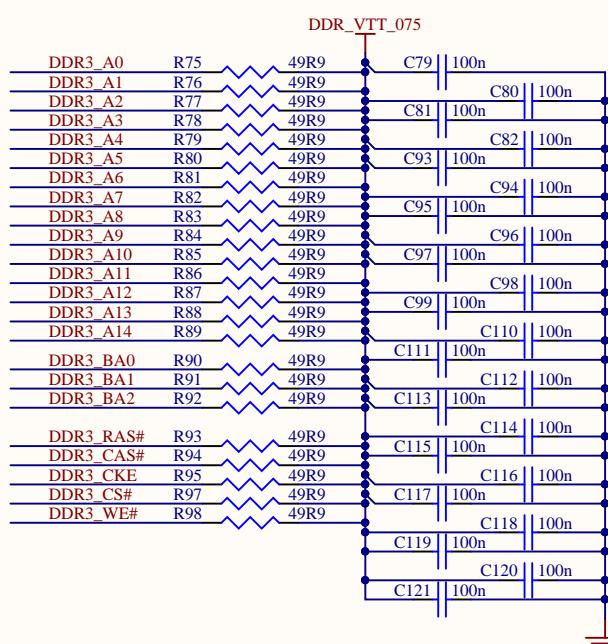
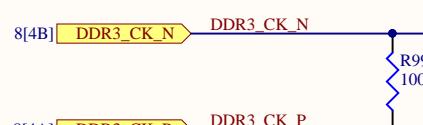
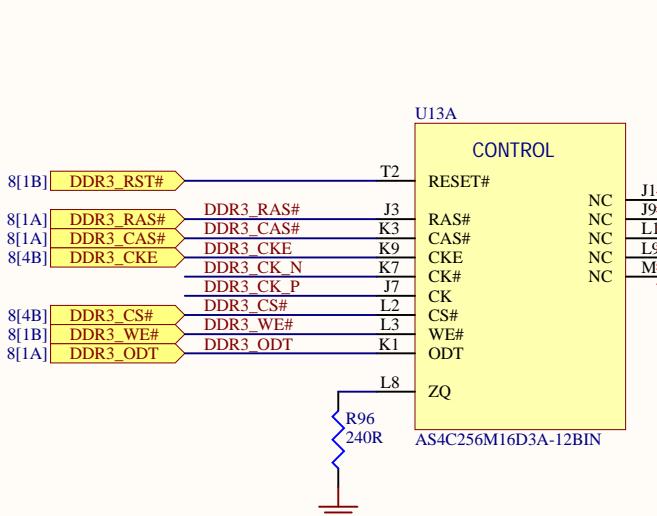
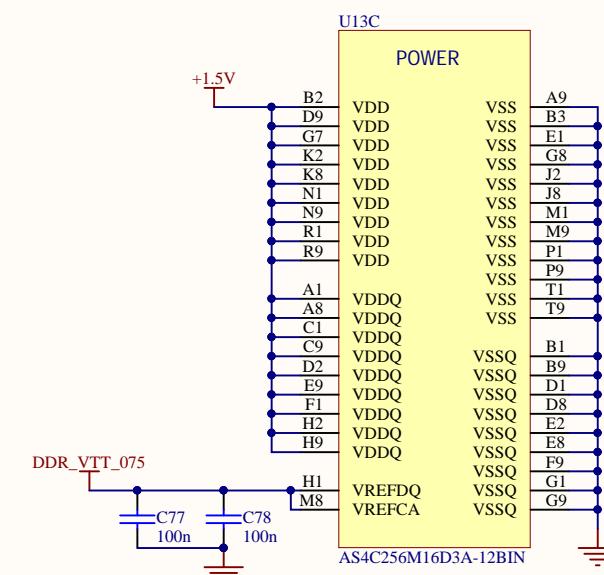
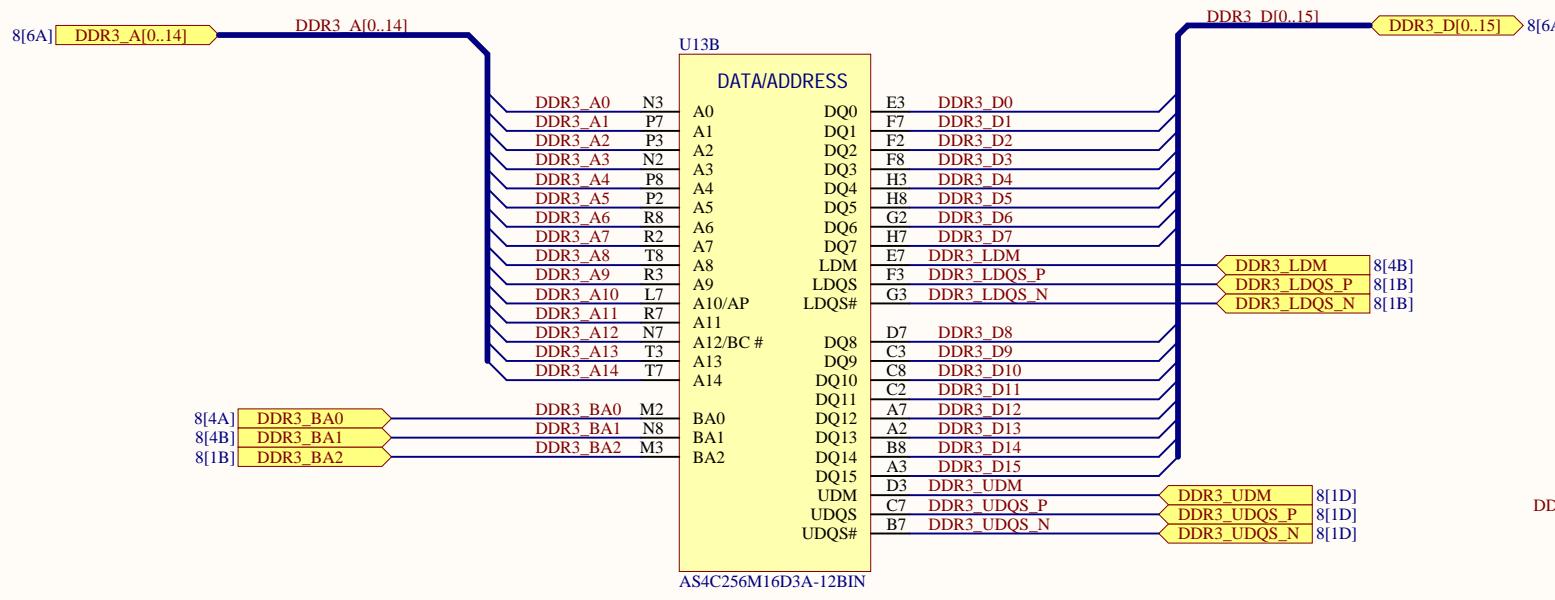
Title
FPGA Bank 4

Size **B** Dwg No. **FEN-412728-SCH-R2**

Rev **2**

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Date **12/14/2017** Sheet **9** of **15** Variant: **MCP3903**

DDR3

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Project Name
Microsemi_Avalanche Rev 2

Title

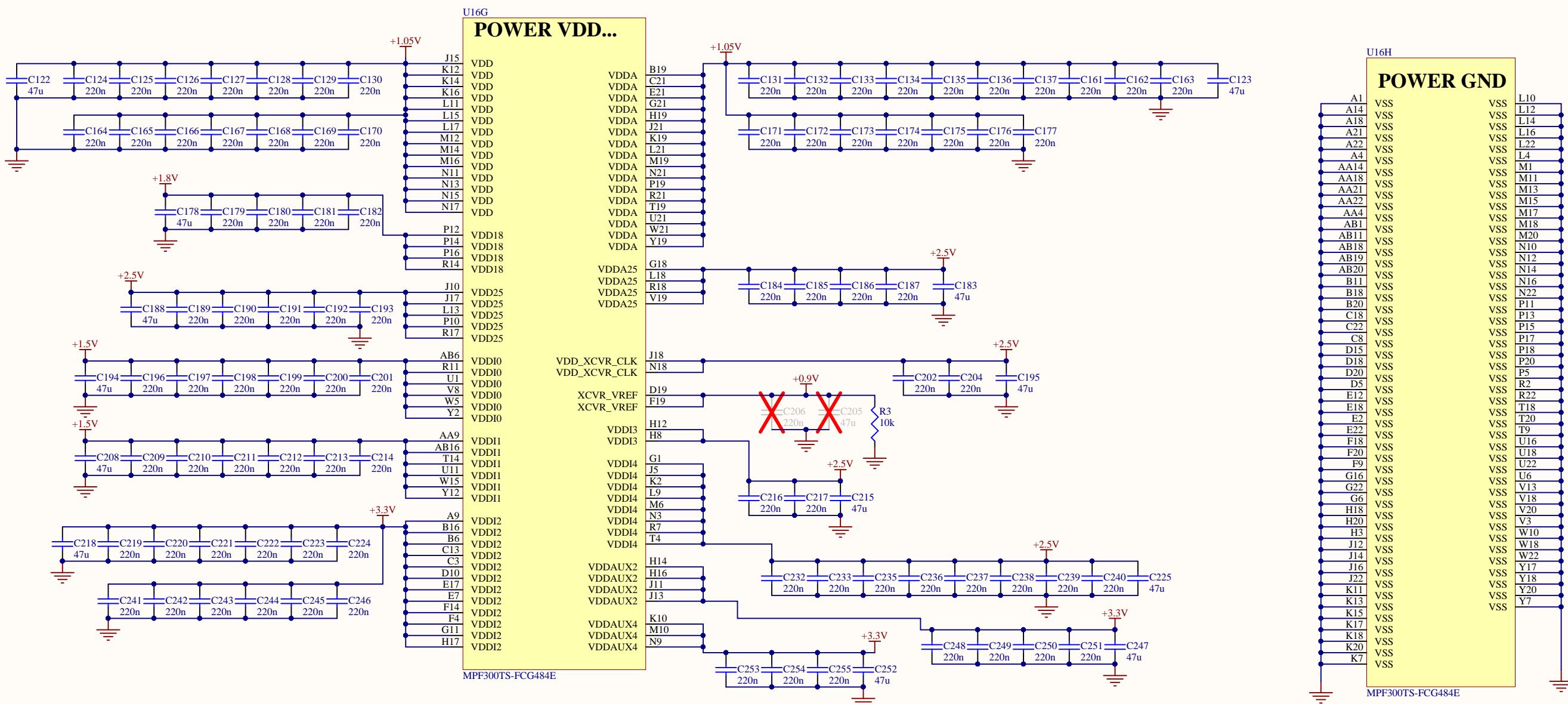
DDR3

Size **B** Dwg No. **FEN-412728-SCH-R2**

Rev **2**

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Date **12/6/2017** Sheet **10 of 15** Variant: **MCP3903**



AEG

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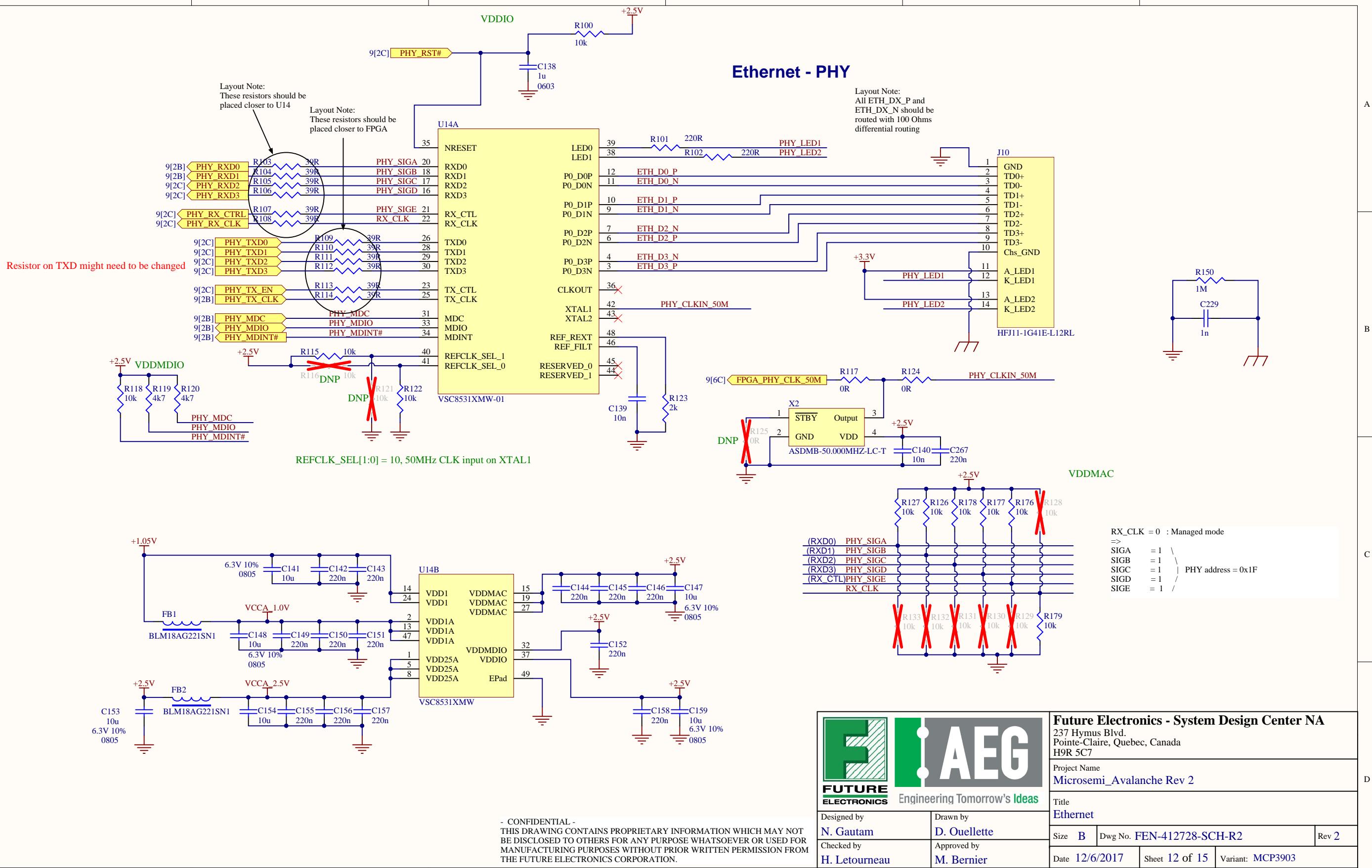
Project Name
Microsemi_Avalanche Rev 2

Title
FPGA Power

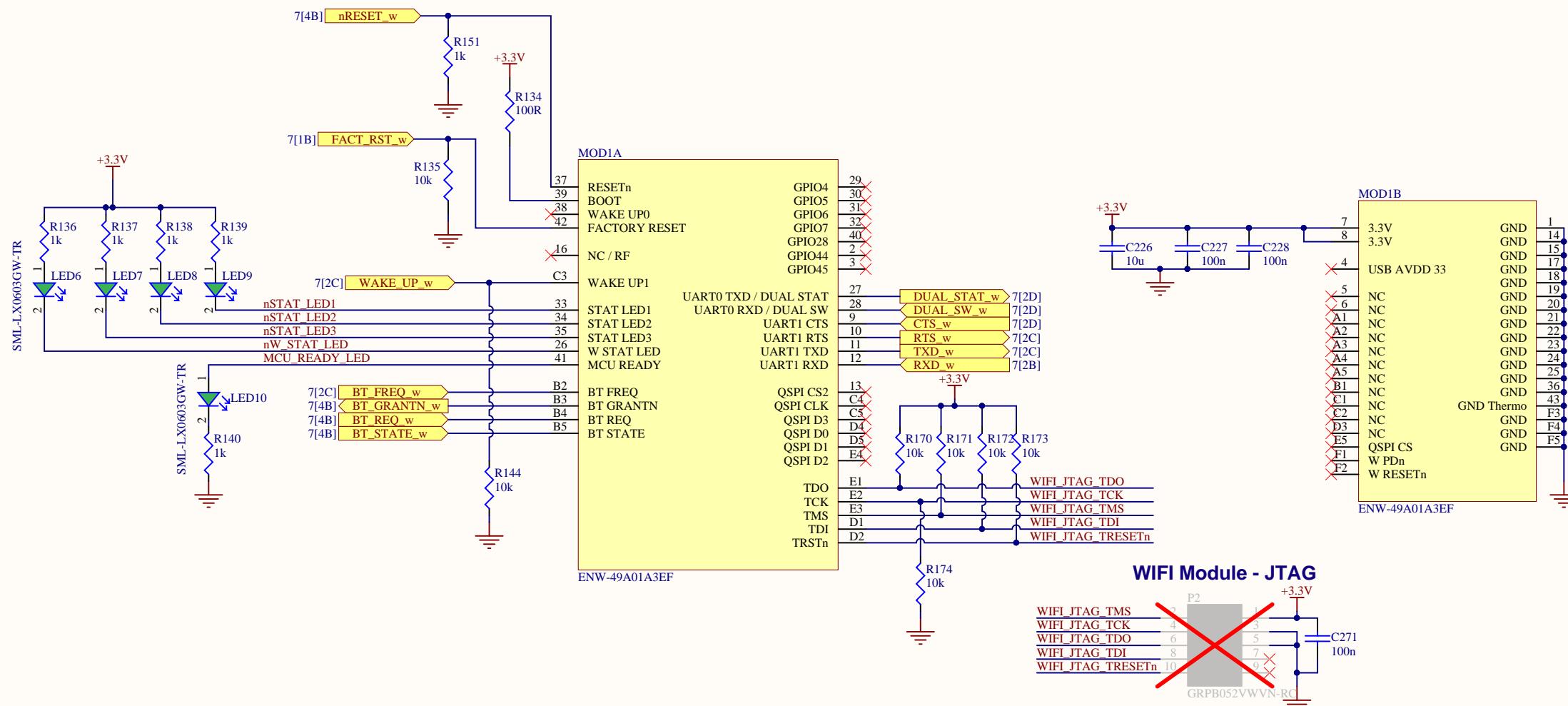
Size **B** Dwg No. **FEN-412728-SCH-R2**

Rev **2**

Designed by **N. Gautam** Drawn by **D. Ouellette**
Checked by **H. Letourneau** Approved by **M. Bernier**
Date **12/14/2017** Sheet **11 of 15** Variant: **MCP3903**



WiFi- (PAN9320)



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Project Name
Microsemi_Avalanche Rev 2

Title
WiFi BLE Combo

Size **B** Dwg No. **FEN-412728-SCH-R2**

Rev **2**

Date **1/12/2018** Sheet **13 of 15** Variant: **MCP3903**

A

A

B

B

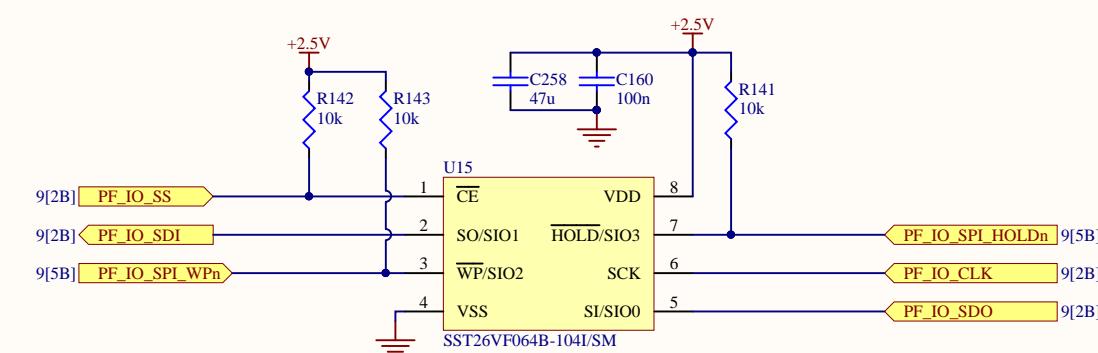
C

C

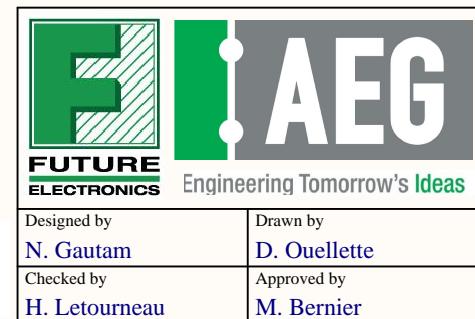
D

D

64 Mbit Serial Flash



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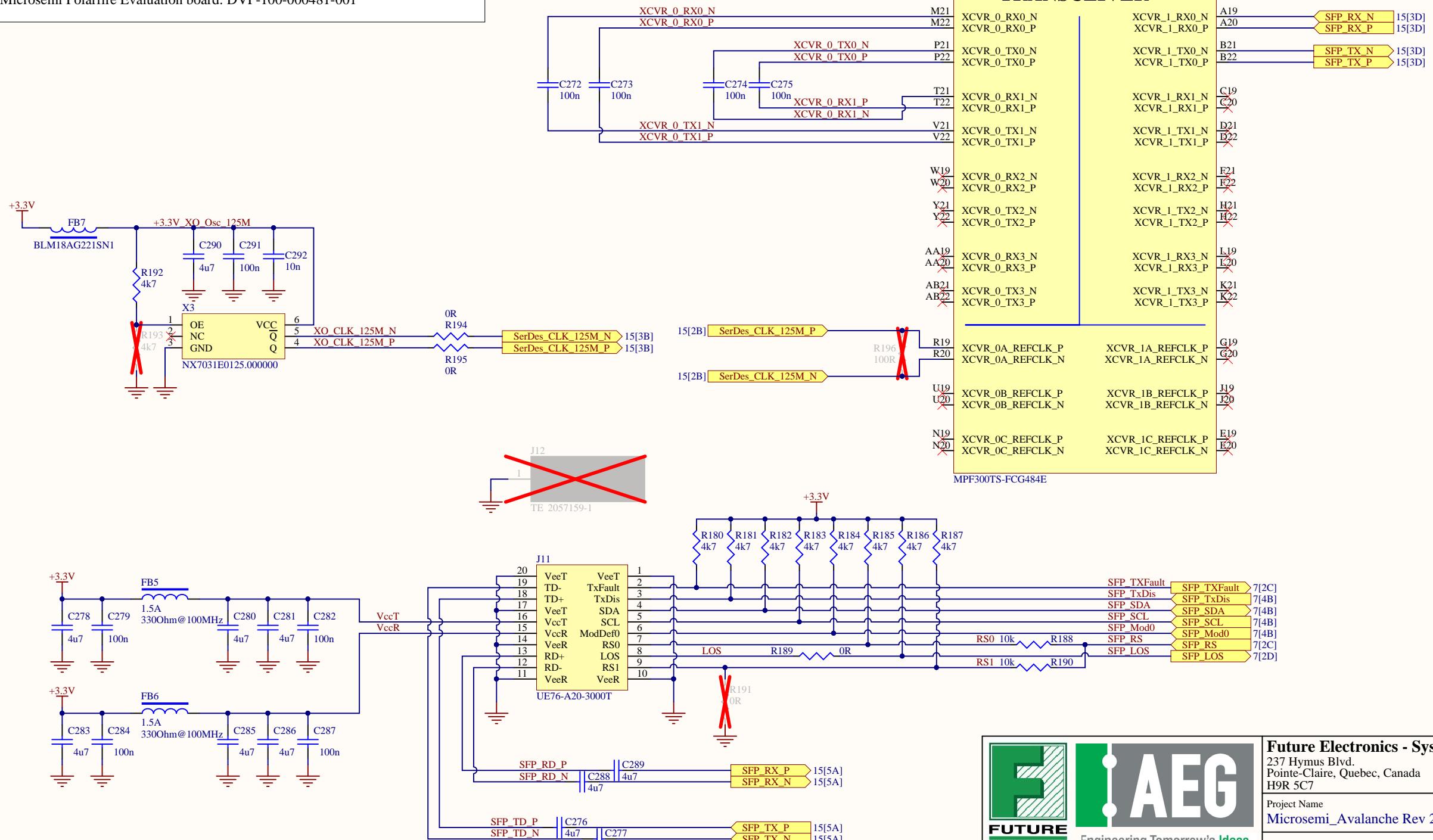


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Project Name Microsemi_Avalanche Rev 2	
Title SPI Memory	
Size B Dwg No. FEN-412728-SCH-R2 Rev 2	
Designed by N. Gautam Drawn by D. Ouellette	
Checked by H. Letourneau Approved by M. Bernier	
Date 12/6/2017 Sheet 14 of 15 Variant: MCP3903	

Note on Serdes:

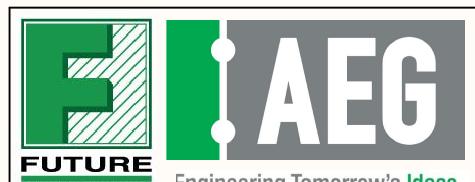
The SerDes implementation provided is for basic evaluation purpose only.
 For high performance evaluation, please call your Future Electronics Representative:
 => Microsemi Polarfire Evaluation board: DVP-100-000481-001

Transceiver - (3.3V)



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Project Name
Microsemi_Avalanche Rev 2

Title
Transceiver

Size **B** Dwg No. **FEN-412728-SCH-R2** Rev **2**

Date **12/14/2017** Sheet **15 of 15** Variant: **MCP3903**

Impedance Requirements

Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)	
Top Layer	5mil	5mil	10mil	4mil	10mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Bottom Layer	5mil	5mil	10mil	4mil	10mil	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0,40mil	3,5	
3	Top_Sig_1	Copper	2,10mil		
4	Dielectric1	FR-4 HTg	3,80mil	4,6	
5	GND_1	Copper	0,70mil		
6	Dielectric 4		7,00mil	4,6	
7	Mid1_Sig_2	Copper	0,70mil		
8	Dielectric2	FR-4 HTg	12,00mil	4,6	
9	Power_1	Copper	1,40mil		
10	Dielectric 5		5,00mil	4,6	
11	Power_2	Copper	1,40mil		
12	Dielectric 7		12,00mil	4,6	
13	Mid2-Sig_3	Copper	0,70mil		
14	Dielectric 8		7,00mil	4,6	
15	GND_2	Copper	0,70mil		
16	Dielectric3	FR-4 HTg	3,80mil	4,6	
17	Bottom_Sig_4	Copper	2,10mil		
18	Bottom Solder	Solder Resist	0,40mil	3,5	
19	Bottom Overlay				

NOTES: < UNLESS OTHERWISE SPECIFIED >

1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET
ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)2. BASE MATERIAL - FR4 High Tg Metal Core Other
- Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL
TO 170°C

3. COPPER FOIL WEIGHT - SEE TABLE FOR STACK-UP DETAIL

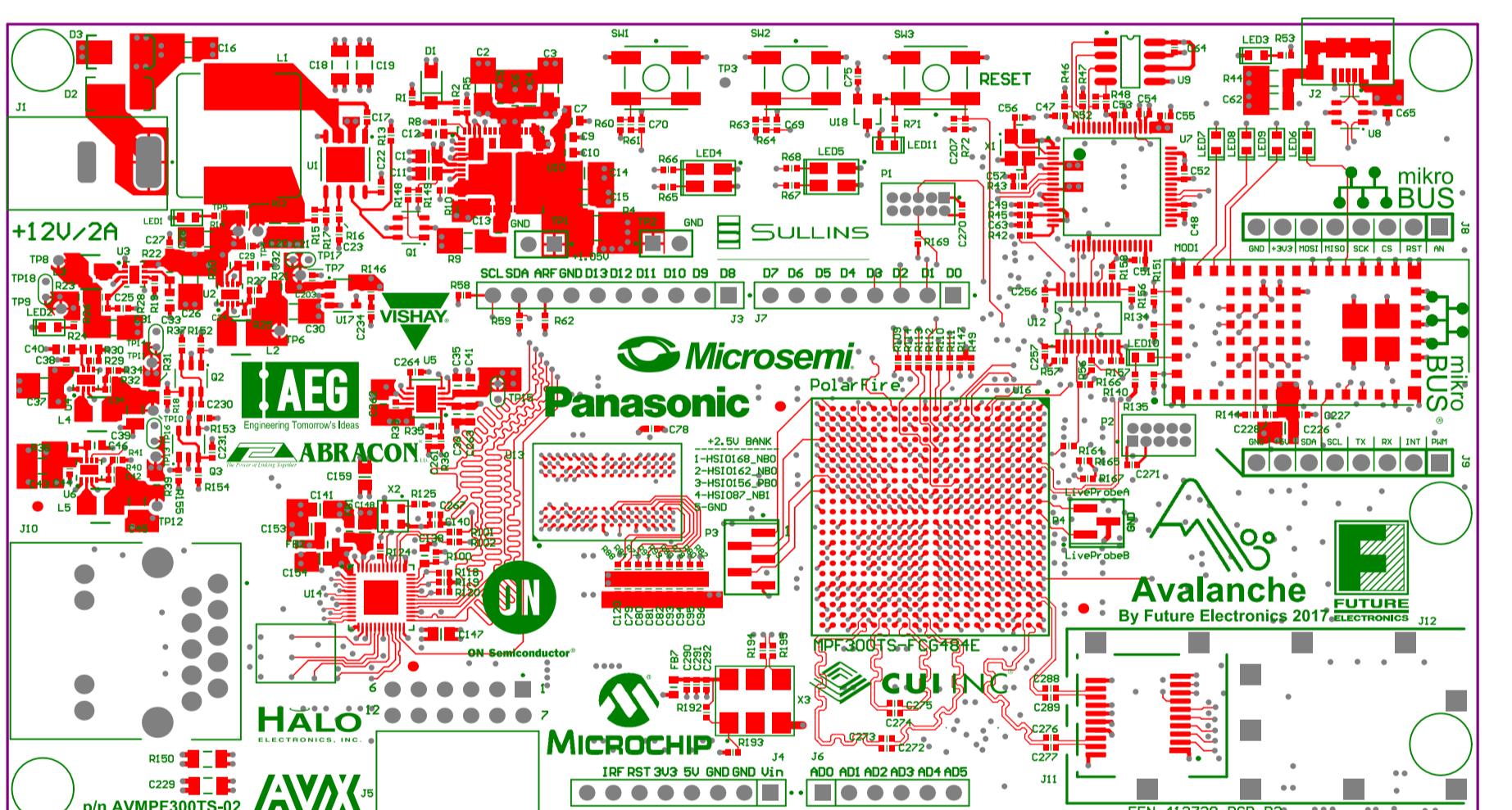
4. PLATING - 0.5oz 0.75oz 1oz Other 5. FINISH - HASL RoHS HASL Immersion Silver Immersion Tin ENIG
Other 6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-840 ON PCB OVER BARE COPPER
- GREEN WHITE BLUE Other 7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
- TOP/BOTTOM TOP ONLY BOTTOM ONLY NONE
- WHITE BLACK Other 8. IMPEDANCE CONTROL - NO YES SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

10. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP
- ALL HOLES LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM

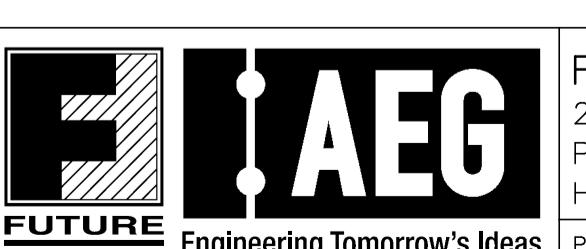
11. GERBER FILES - SUPPLIED GERBER FILES MUST NOT BE MODIFIED WITHOUT PRIOR PERMISSION FROM THE CLIENT

12. LOGO - ONLY LOGOS SUPPLIED IN GERBER FILES WILL BE ACCEPTED ON PCB

13. TOOLING HOLES - NO HOLES SHALL BE PERMITTED WITHIN THE BOARD AREA, EXCEPT THOSE INDICATED
IN THE DRILL LEGEND14. REGISTRATION - REGISTRATION OF PATTERNS TO BE WITHIN +/- .005 LOCATION OF PATTERN ON BOARD
TO DIMENSION SHOWN

Top_Sig_1

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Project #	Microsemi_Avalanche
Title:	Board Name
Size:	B
DWG NO:	FEN-412728-PCB-R2
REV:	2

Checked by: H. Letourneau Approved by: M. Bernier
Date: 1/12/2018 Sheet 1 of 1

Impedance Requirements

Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)	
Top Layer	5mil	5mil	10mil	4mil	10mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Bottom Layer	5mil	5mil	10mil	4mil	10mil	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0,40mil	3,5	
3	Top_Sig_1	Copper	2,10mil		
4	Dielectric1	FR-4 HTg	3,80mil	4,6	
5	GND_1	Copper	0,70mil		
6	Dielectric 4		7,00mil	4,6	
7	Mid1_Sig_2	Copper	0,70mil		
8	Dielectric2	FR-4 HTg	12,00mil	4,6	
9	Power_1	Copper	1,40mil		
10	Dielectric 5		5,00mil	4,6	
11	Power_2	Copper	1,40mil		
12	Dielectric 7		12,00mil	4,6	
13	Mid2-Sig_3	Copper	0,70mil		
14	Dielectric 8		7,00mil	4,6	
15	GND_2	Copper	0,70mil		
16	Dielectric3	FR-4 HTg	3,80mil	4,6	
17	Bottom_Sig_4	Copper	2,10mil		
18	Bottom Solder	Solder Resist	0,40mil	3,5	
19	Bottom Overlay				

NOTES: < UNLESS OTHERWISE SPECIFIED >

1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET
ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)2. BASE MATERIAL - FR4 High Tg Metal Core Other
- Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL
TO 170°C

3. COPPER FOIL WEIGHT - SEE TABLE FOR STACK-UP DETAIL

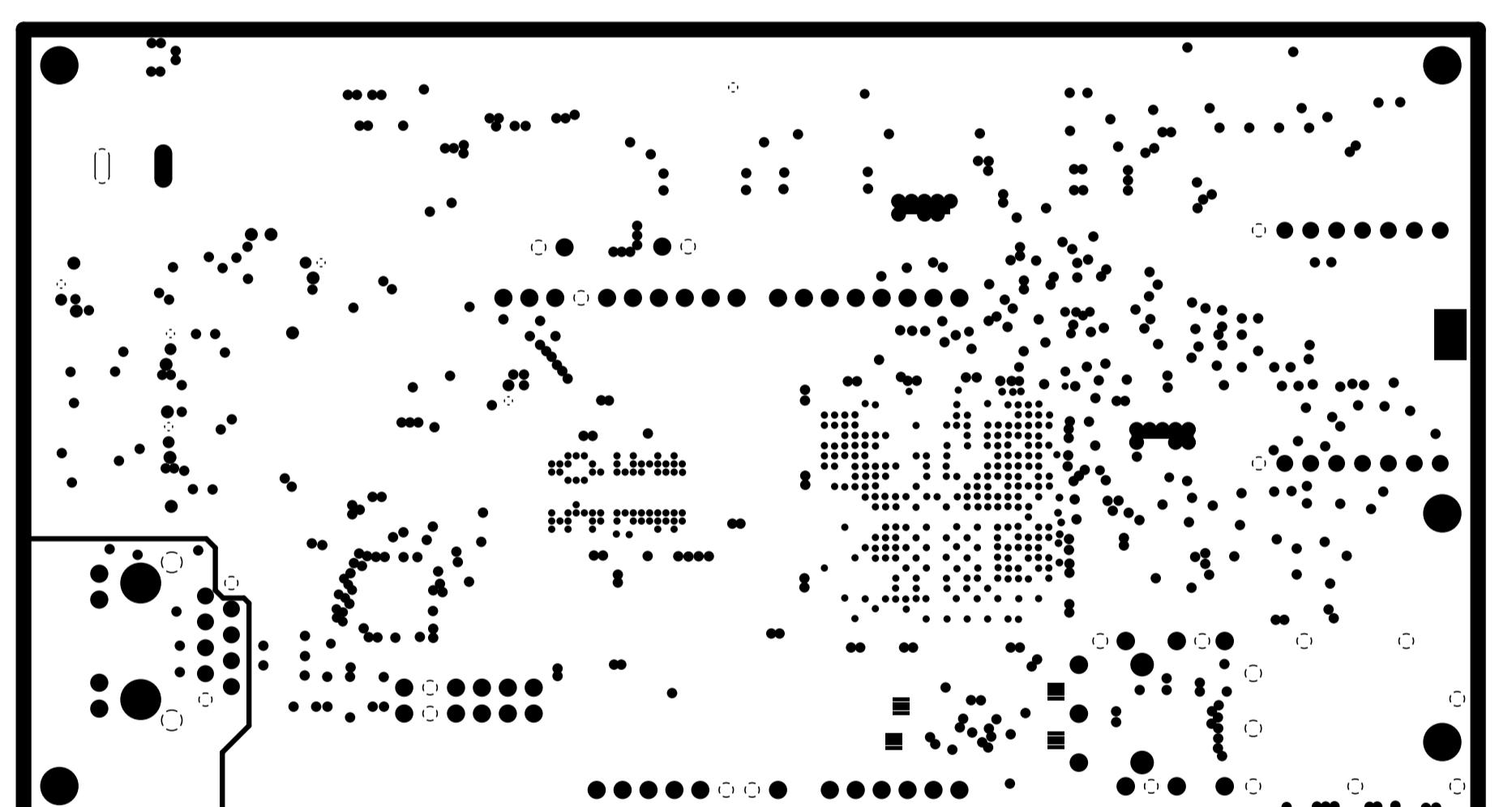
4. PLATING - 0.5oz 0.75oz 1oz Other 5. FINISH - HASL RoHS HASL Immersion Silver Immersion Tin ENIG
Other 6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-810 ON PCB OVER BARE COPPER
- GREEN WHITE BLUE Other 7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
- TOP/BOTTOM TOP ONLY BOTTOM ONLY NONE
- WHITE BLACK Other 8. IMPEDANCE CONTROL - NO YES SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

10. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP
- ALL HOLES LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM

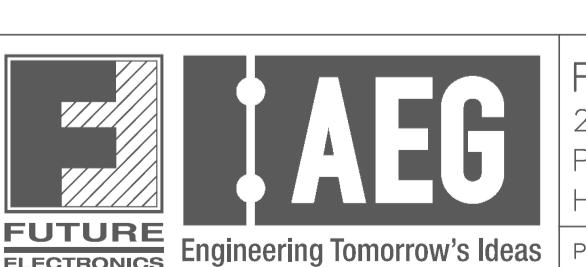
11. GERBER FILES - SUPPLIED GERBER FILES MUST NOT BE MODIFIED WITHOUT PRIOR PERMISSION FROM THE CLIENT

12. LOGO - ONLY LOGOS SUPPLIED IN GERBER FILES WILL BE ACCEPTED ON PCB

13. TOOLING HOLES - NO HOLES SHALL BE PERMITTED WITHIN THE BOARD AREA, EXCEPT THOSE INDICATED
IN THE DRILL LEGEND14. REGISTRATION - REGISTRATION OF PATTERNS TO BE WITHIN +/- .005 LOCATION OF PATTERN ON BOARD
TO DIMENSION SHOWN

GND_1

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237 Hymus Blvd
Pointe-Claire, Quebec, Canada
H9R 5C7

Project #	Microsemi_Avalanche
Title:	Board Name
Size:	DWG NO: FEN-412728-PCB-R2
Date:	1/12/2018
Sheet	1 of 1

Impedance Requirements

Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)	
Top Layer	5mil	5mil	10mil	4mil	10mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Bottom Layer	5mil	5mil	10mil	4mil	10mil	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0,40mil	3,5	
3	Top_Sig_1	Copper	2,10mil		
4	Dielectric1	FR-4 HTg	3,80mil	4,6	
5	GND_1	Copper	0,70mil		
6	Dielectric 4		7,00mil	4,6	
7	Mid1_Sig_2	Copper	0,70mil		
8	Dielectric2	FR-4 HTg	12,00mil	4,6	
9	Power_1	Copper	1,40mil		
10	Dielectric 5		5,00mil	4,6	
11	Power_2	Copper	1,40mil		
12	Dielectric 7		12,00mil	4,6	
13	Mid2-Sig_3	Copper	0,70mil		
14	Dielectric 8		7,00mil	4,6	
15	GND_2	Copper	0,70mil		
16	Dielectric3	FR-4 HTg	3,80mil	4,6	
17	Bottom_Sig_4	Copper	2,10mil		
18	Bottom Solder	Solder Resist	0,40mil	3,5	
19	Bottom Overlay				

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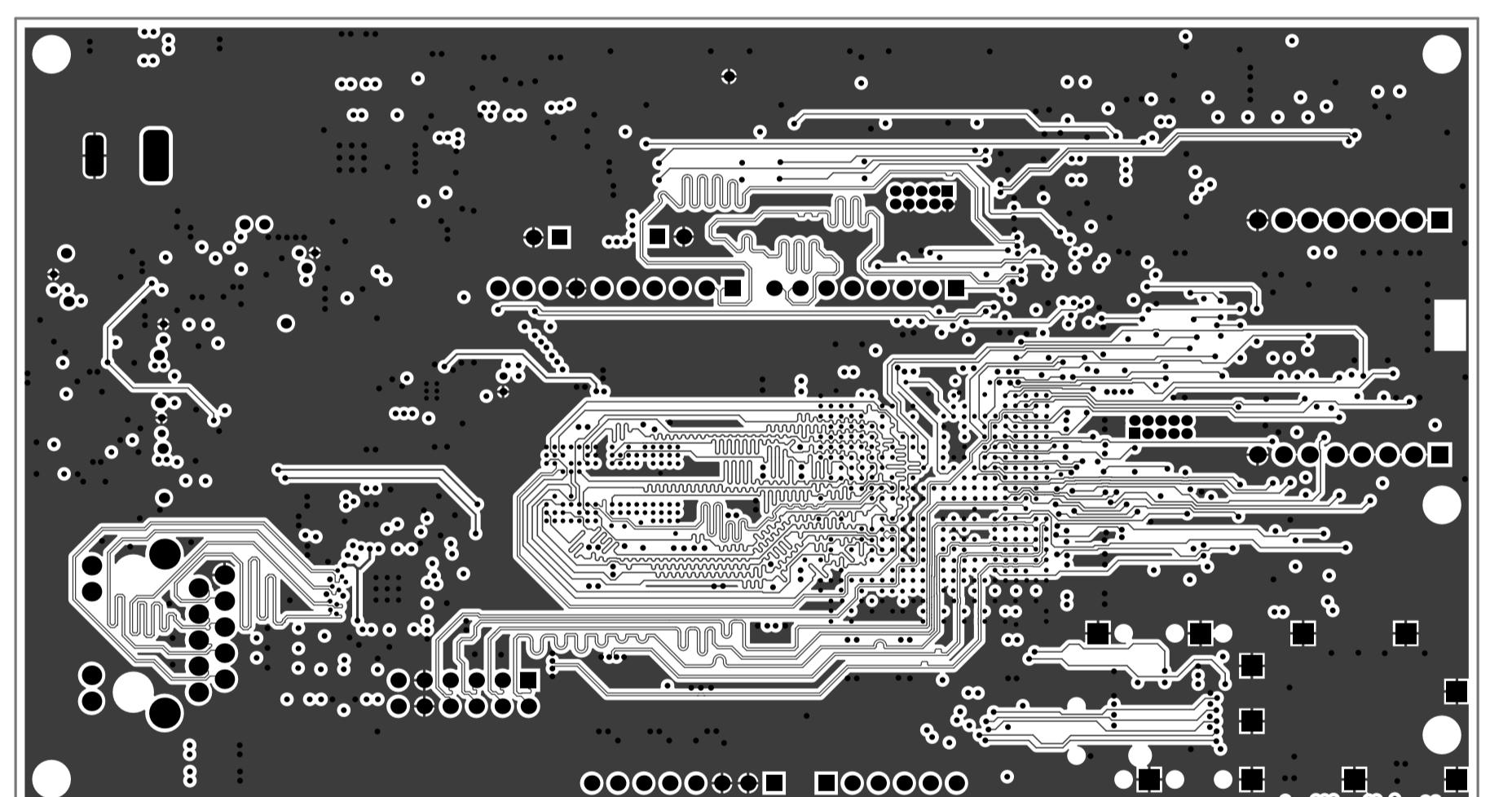
4. PLATING - 0.5oz 0.75oz 1oz Other 5. FINISH - HASL RoHS HASL Immersion Silver Immersion Tin ENIG
Other 6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-810 ON PCB OVER BARE COPPER
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- TOP/BOTTOM TOP ONLY BOTTOM ONLY NONE
- WHITE BLACK Other 8. IMPEDANCE CONTROL - NO YES SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

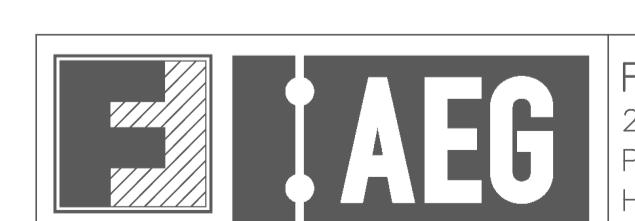
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TO DIMENSION SHOWN

Mid1_Sig_2



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237 Hymus Blvd
Pointe-Claire, Quebec, Canada
H9R 5C7

Project #	Microsemi_Avalanche
Title:	Board Name
Size: B	DWG NO: FEN-412728-PCB-R2
Date:	1/12/2018
Sheet	1 of 1

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Impedance Requirements

Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)	
Top Layer	5mil	5mil	10mil	4mil	10mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Bottom Layer	5mil	5mil	10mil	4mil	10mil	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0,40mil	3,5	
3	Top_Sig_1	Copper	2,10mil		
4	Dielectric1	FR-4 HTg	3,80mil	4,6	
5	GND_1	Copper	0,70mil		
6	Dielectric 4		7,00mil	4,6	
7	Mid1_Sig_2	Copper	0,70mil		
8	Dielectric2	FR-4 HTg	12,00mil	4,6	
9	Power_1	Copper	1,40mil		
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12	Dielectric 7		12,00mil	4,6	
13	Mid2-Sig_3	Copper	0,70mil		
14	Dielectric 8		7,00mil	4,6	
15	GND_2	Copper	0,70mil		
16	Dielectric3	FR-4 HTg	3,80mil	4,6	
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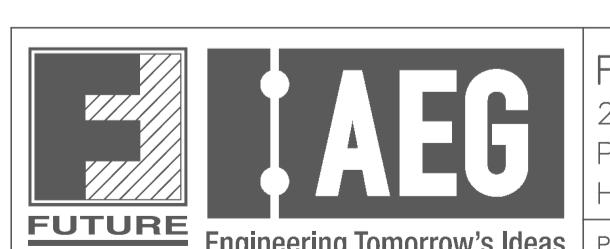
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- WHITE BLACK Other 8. IMPEDANCE CONTROL - NO YES SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

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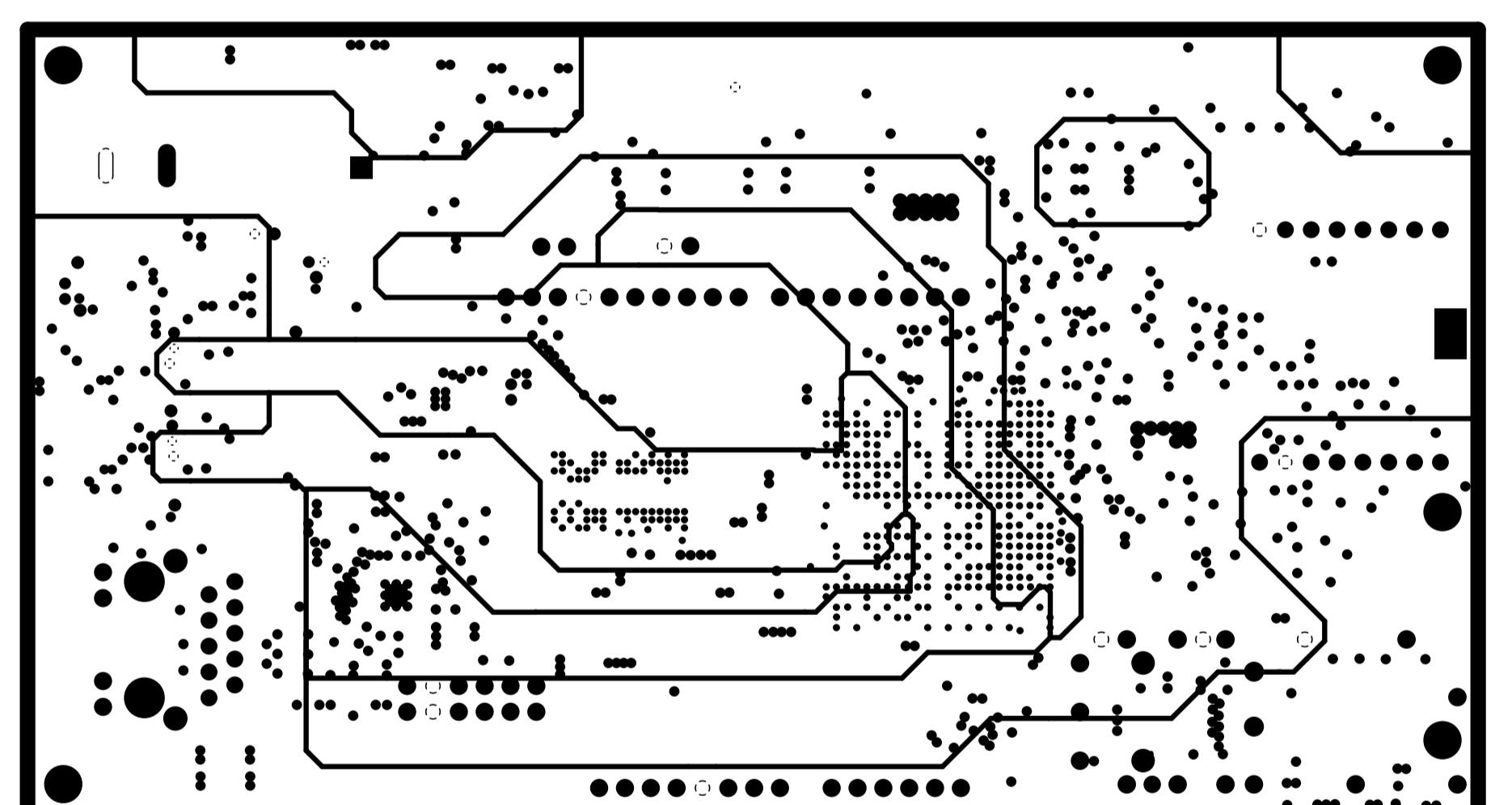
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Future Electronics – System Design Center NA
237 Hymus Blvd
Pointe-Claire, Quebec, Canada
H9R 5C7

Project #	Microsemi_Avalanche
Title:	Board Name
Size:	DWG NO: FEN-412728-PCB-R2
Date:	1/12/2018
Sheet	1 of 1

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Power_1

Impedance Requirements

Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)	
Top Layer	5mil	5mil	10mil	4mil	10mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Bottom Layer	5mil	5mil	10mil	4mil	10mil	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
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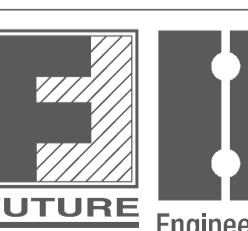
9. ELECTRICAL TEST - 100% IPC-D-356B

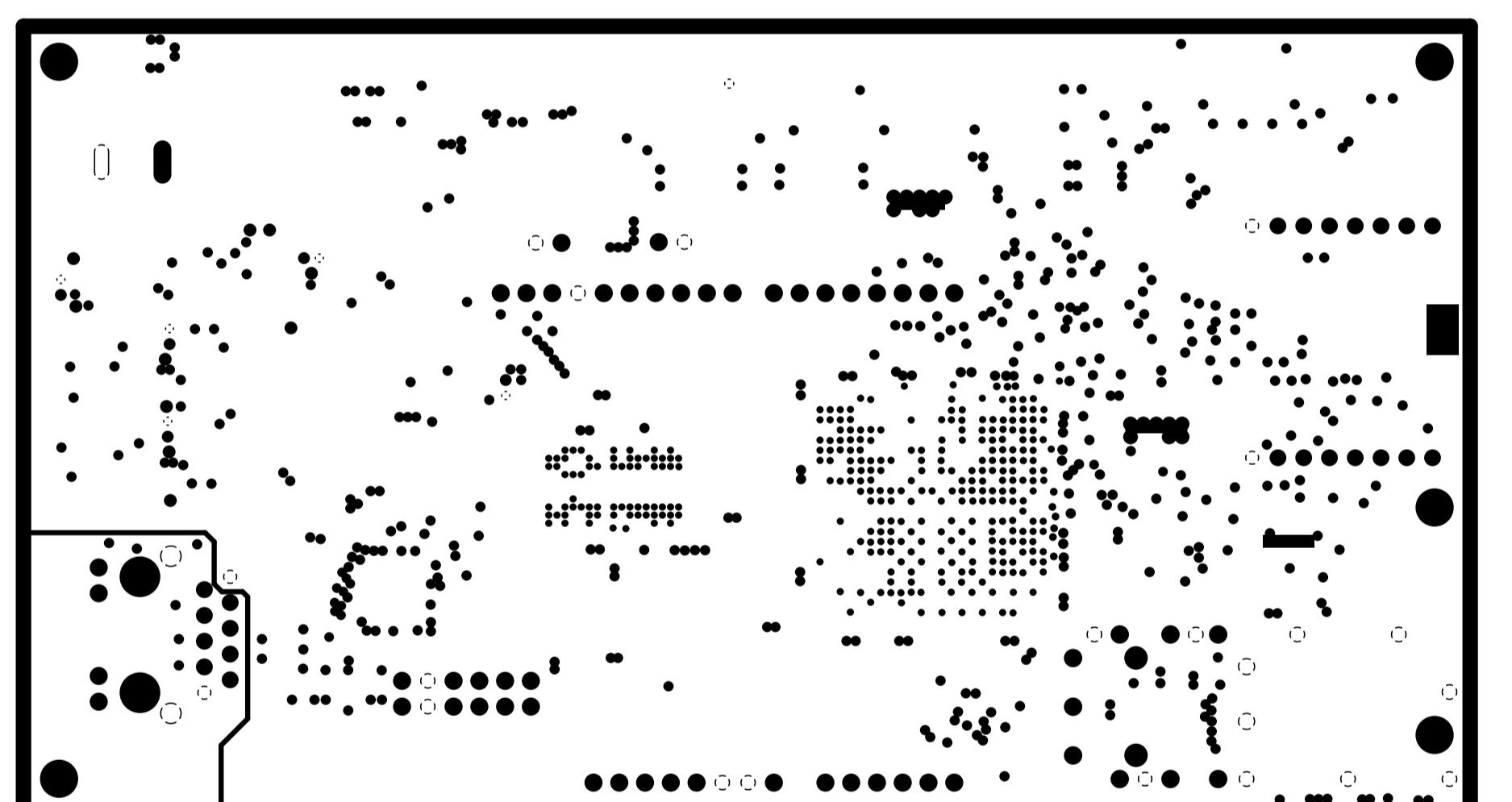
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  Future Electronics – System Design Center NA 237 Hymus Blvd Pointe-Claire, Quebec, Canada H9R 5C7	
Project # Microsemi_Avalanche	
Designed by: N. Gautam	Drawn by: A. Desbiens
Checked by: H. Letourneau	Approved by: M. Bernier
Date: 1/12/2018	
Sheet 1 of 1	



GND_2

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Impedance Requirements

Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
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Bottom Layer	5mil	5mil	10mil	4mil	10mil	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
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19	Bottom Overlay				

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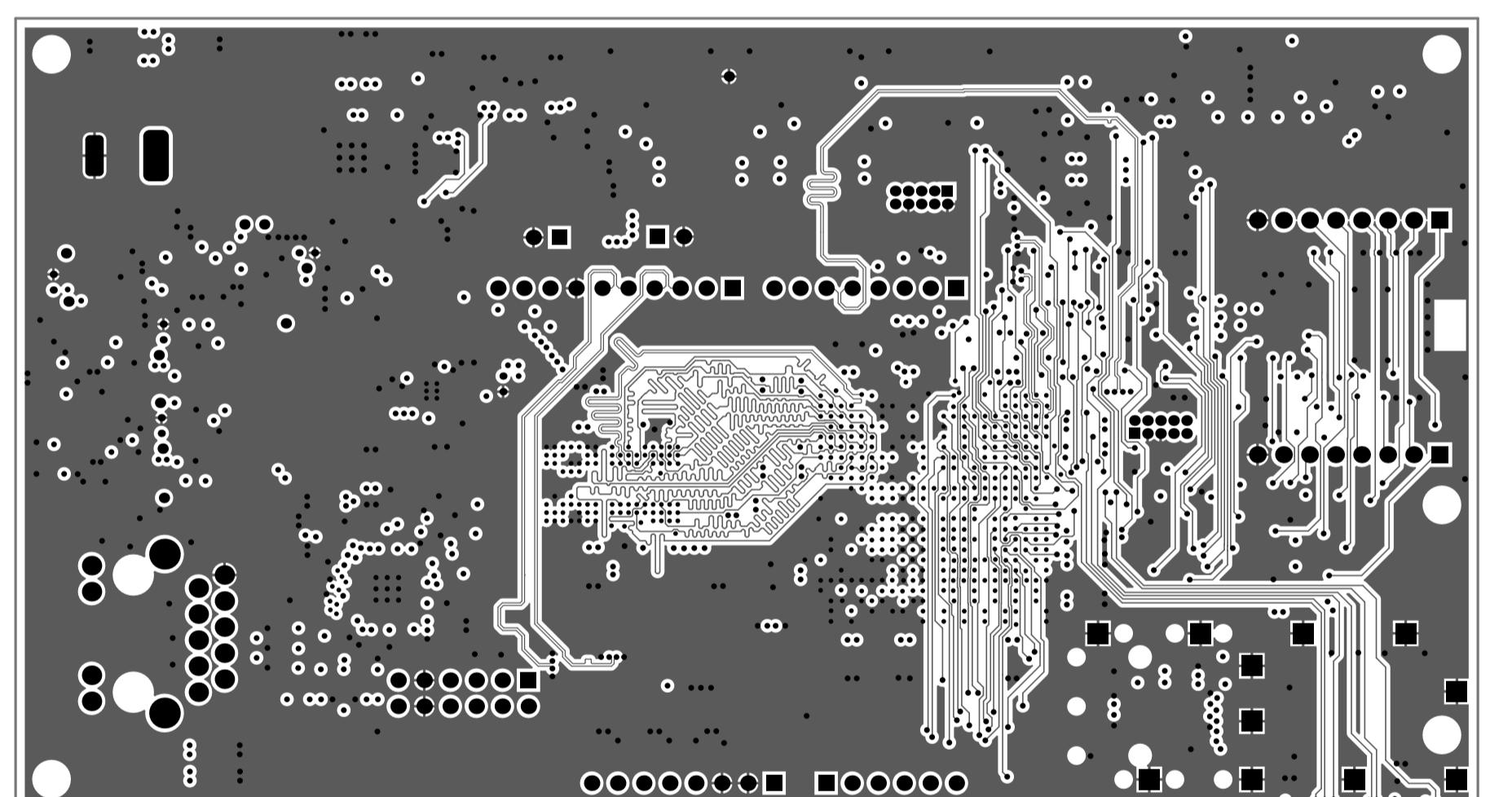
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Mid2-Sig_3



Future Electronics – System Design Center NA
237 Hymus Blvd
Pointe-Claire, Quebec, Canada
H9R 5C7

Project #	Microsemi_Avalanche
Title:	Board Name
Size:	DWG NO: FEN-412728-PCB-R2
Date:	1/12/2018
Sheet	1 of 1

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Layer	Name	Material	Thickness	Constant	Board Layer Stack
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18	Bottom Solder	Solder Resist	0,40mil	3,5	
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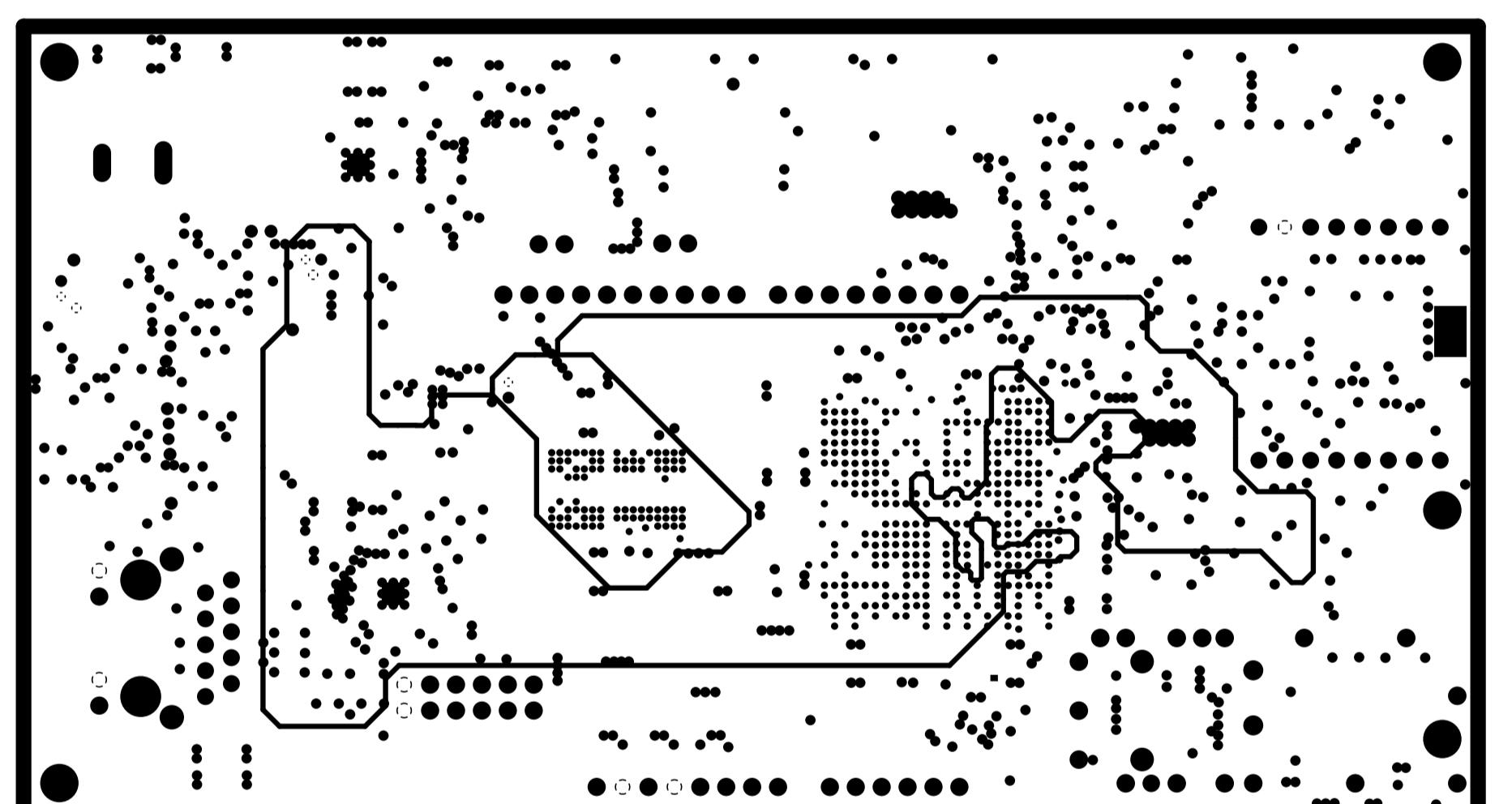
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Power_2



Future Electronics – System Design Center NA
237 Hymus Blvd
Pointe-Claire, Quebec, Canada
H9R 5C7

Project #	Microsemi_Avalanche
Title:	Board Name
Size:	DWG NO: FEN-412728-PCB-R2
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Sheet	1 of 1

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Impedance Requirements

Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)	
Top Layer	5mil	5mil	10mil	4mil	10mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Bottom Layer	5mil	5mil	10mil	4mil	10mil	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0,40mil	3,5	
3	Top_Sig_1	Copper	2,10mil		
4	Dielectric1	FR-4 HTg	3,80mil	4,6	
5	GND_1	Copper	0,70mil		
6	Dielectric 4		7,00mil	4,6	
7	Mid1_Sig_2	Copper	0,70mil		
8	Dielectric2	FR-4 HTg	12,00mil	4,6	
9	Power_1	Copper	1,40mil		
10	Dielectric 5		5,00mil	4,6	
11	Power_2	Copper	1,40mil		
12	Dielectric 7		12,00mil	4,6	
13	Mid2-Sig_3	Copper	0,70mil		
14	Dielectric 8		7,00mil	4,6	
15	GND_2	Copper	0,70mil		
16	Dielectric3	FR-4 HTg	3,80mil	4,6	
17	Bottom_Sig_4	Copper	2,10mil		
18	Bottom Solder	Solder Resist	0,40mil	3,5	
19	Bottom Overlay				

NOTES: < UNLESS OTHERWISE SPECIFIED >

1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET
ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)2. BASE MATERIAL - FR4 High Tg Metal Core Other
- Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL
TO 170°C

3. COPPER FOIL WEIGHT - SEE TABLE FOR STACK-UP DETAIL

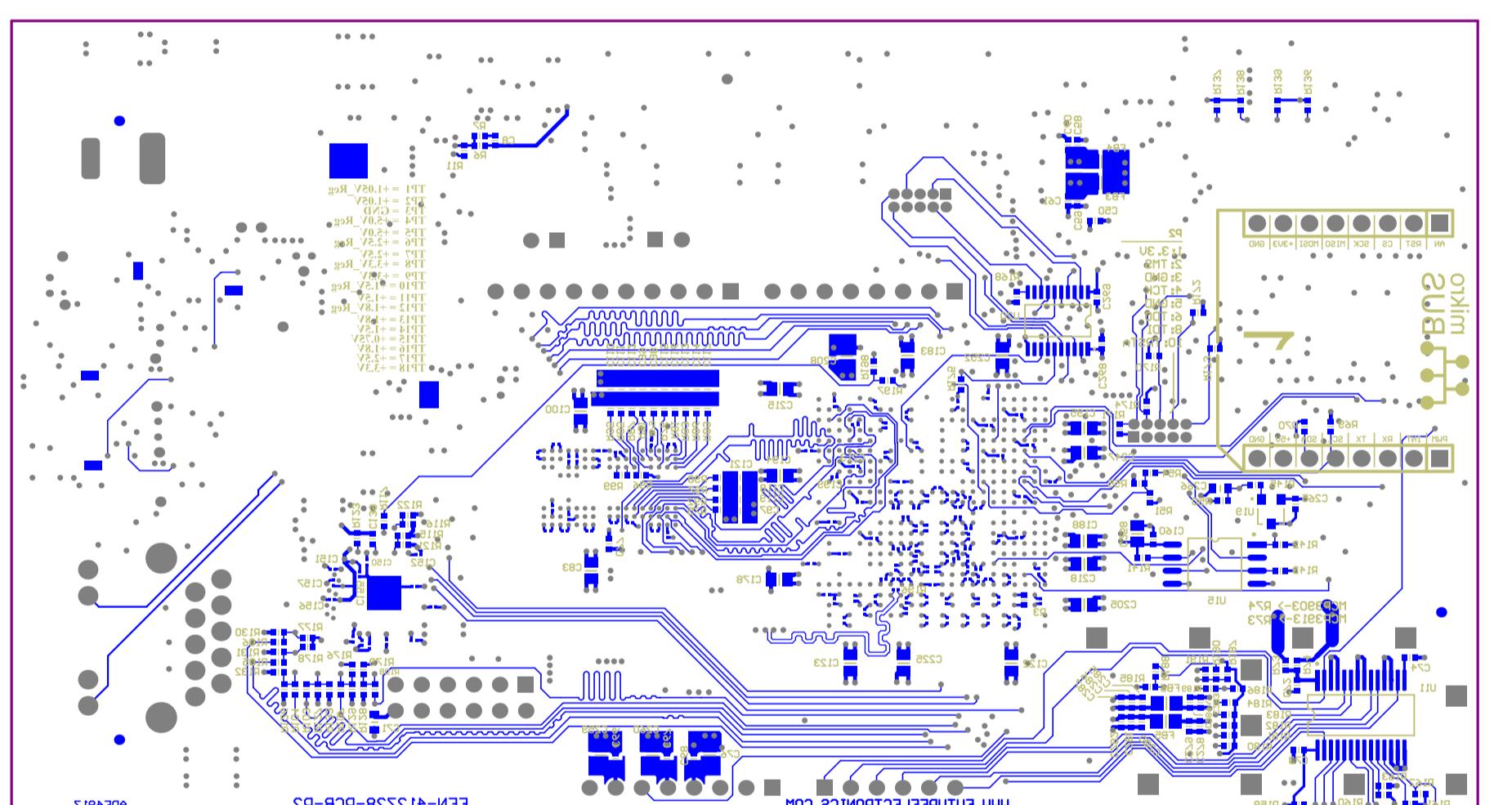
4. PLATING - 0.5oz 0.75oz 1oz Other 5. FINISH - HASL RoHS HASL Immersion Silver Immersion Tin ENIG
Other 6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-810 ON PCB OVER BARE COPPER
- GREEN WHITE BLUE Other 7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
- TOP/BOTTOM TOP ONLY BOTTOM ONLY NONE
- WHITE BLACK Other 8. IMPEDANCE CONTROL - NO YES SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

10. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP
- ALL HOLES LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM

11. GERBER FILES - SUPPLIED GERBER FILES MUST NOT BE MODIFIED WITHOUT PRIOR PERMISSION FROM THE CLIENT

12. LOGO - ONLY LOGOS SUPPLIED IN GERBER FILES WILL BE ACCEPTED ON PCB

13. TOOLING HOLES - NO HOLES SHALL BE PERMITTED WITHIN THE BOARD AREA, EXCEPT THOSE INDICATED
IN THE DRILL LEGEND14. REGISTRATION - REGISTRATION OF PATTERNS TO BE WITHIN +/- .005 LOCATION OF PATTERN ON BOARD
TO DIMENSION SHOWN

Bottom_Sig_4

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FROM THE FUTURE ELECTRONICS CORPORATION.



Future Electronics – System Design Center NA
237 Hymus Blvd
Pointe-Claire, Quebec, Canada
H9R 5C7
Project # Microsemi_Avalanche
Title: Board Name
Size: B DWG NO: FEN-412728-PCB-R2 REV: 2
Checked by: H. Letourneau Approved by: M. Bernier
Date: 1/12/2018 Sheet 1 of 1

Impedance Requirements

Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
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16	Dielectric3	FR-4 HTg	3,80mil	4,6	
17	Bottom_Sig_4	Copper	2,10mil		
18	Bottom Solder	Solder Resist	0,40mil	3,5	
19	Bottom Overlay				

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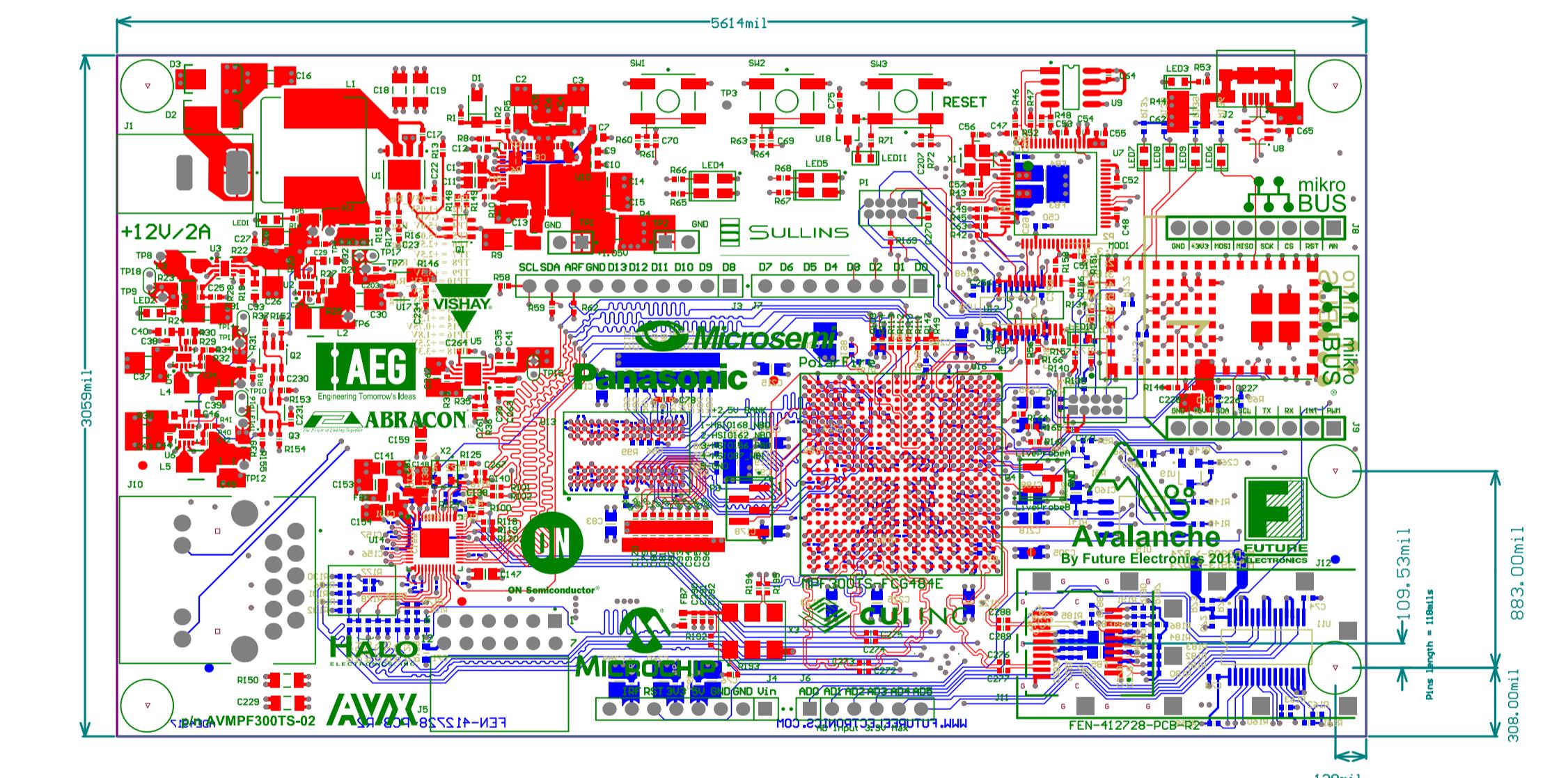
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TO DIMENSION SHOWN

  <p>Future Electronics – System Design Center NA 237 Hymus Blvd Pointe-Claire, Quebec, Canada H9R 5C7</p>	
Project # Microsemi_Avalanche	
Designed by: N. Gautam	Drawn by: A. Desbiens
Checked by: H. Letourneau	Approved by: M. Bernier
Title: Board Name	
Size: B	DWG NO: FEN-412728-PCB-R2
Date: 1/12/2018	REV: 2
Sheet 1 of 1	



Top_Sig_1

Bottom_Sig_4

Symbol	Count	Hole Size	Hole Length	Routed Path Length	Plated	Hole Type
E	1	37.00mil (0.94mm)	-	58.74mil (1.49mm)	PTH	Round
H	1	38.29mil (1.00mm)	116.11mil (3.00mm)	98.74mil (2.00mm)	PTH	Slot
O	1	39.37mil (1.00mm)	137.80mil (3.50mm)	98.43mil (2.50mm)	PTH	Slot
F	2	47.24mil (1.20mm)	-	-	PTH	Round
C	2	61.02mil (1.55mm)	-	-	PTH	Round
●	2	64.17mil (1.65mm)	-	-	PTH	Round
□	2	128.00mil (3.25mm)	-	-	PTH	Round
▽	2	188.11mil (4.80mm)	-	-	PTH	Round
○	5	40.40mil (1.00mm)	-	-	PTH	Round
×	9	41.34mil (1.05mm)	-	-	PTH	Round
▼	9	7.87mil (0.20mm)	-	-	PTH	Round
G	9	41.34mil (1.05mm)	-	-	PTH	Round
◊	10	16.00mil (0.40mm)	-	-	PTH	Round
■	10	35.43mil (0.90mm)	-	-	PTH	Round
△	11	20.00mil (0.50mm)	-	-	PTH	Round
D	14	26.00mil (0.65mm)	-	-	PTH	Round
□	20	27.55mil (0.70mm)	-	-	PTH	Round
×	44	40.16mil (1.02mm)	-	-	PTH	Round
○	498	8.00mil (0.20mm)	-	-	PTH	Round
	144 Total	10.00mil (0.25mm)	-	-	PTH	Round

Slot definitions: Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout.

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