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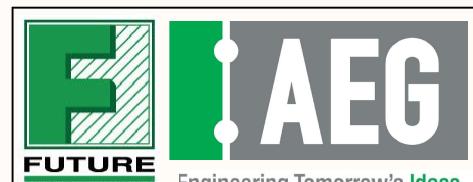
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Engineering Tomorrow's Ideas

Designed by N. Gautam Drawn by D. Ouellette

Checked by H. Letourneau Approved by M. Bernier

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H9R 5C7

Project Name
Microsemi_Avalanche Rev 3

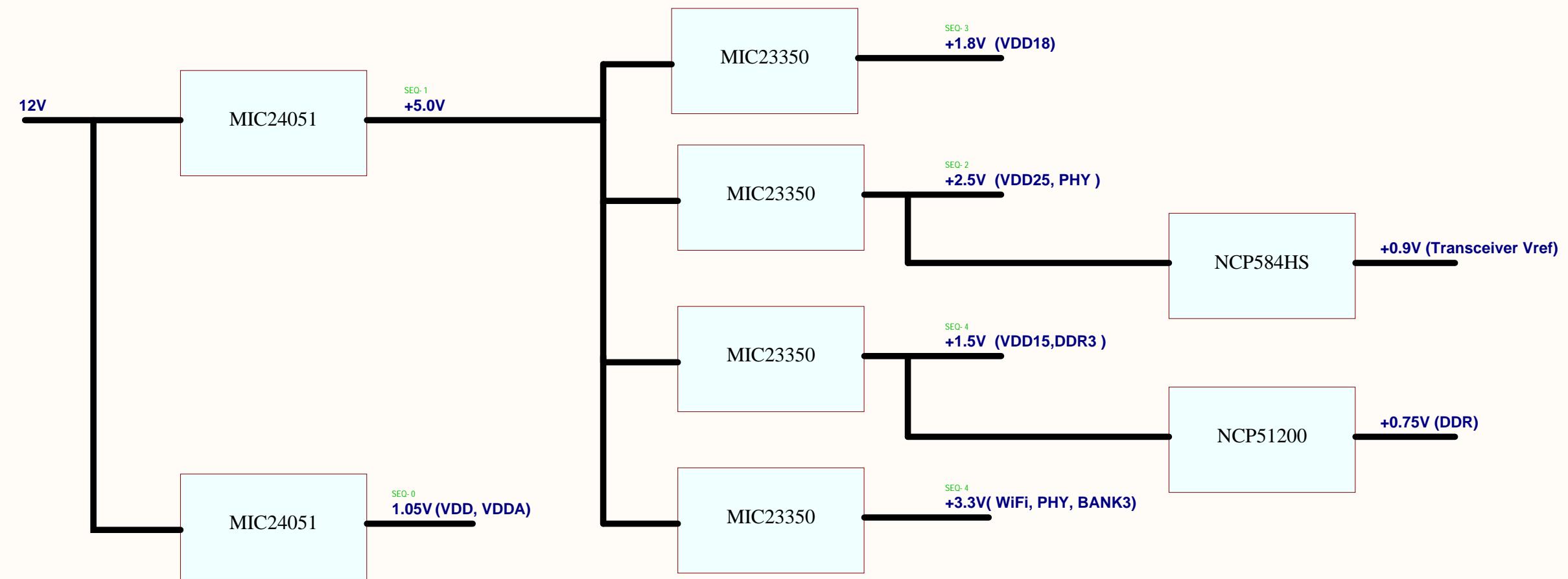
Title
Block Diagram

Size B Dwg No. FEN-412728-SCH-R3 Rev 3

Date 1/13/2020 Sheet 1 of 16 Variant: MCP3913



Power supply block diagram



Power supply sequencing requirement for FPGA
 1) VDD & VDDA (1.05V)
 2) VDD25
 3) VDD18
 4) Others (+1.5V, +3.3V)



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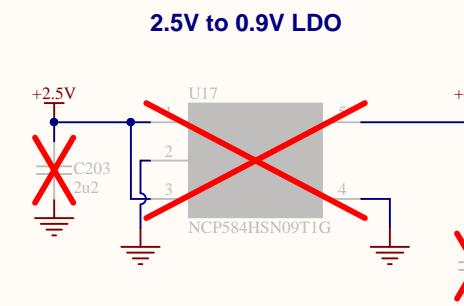
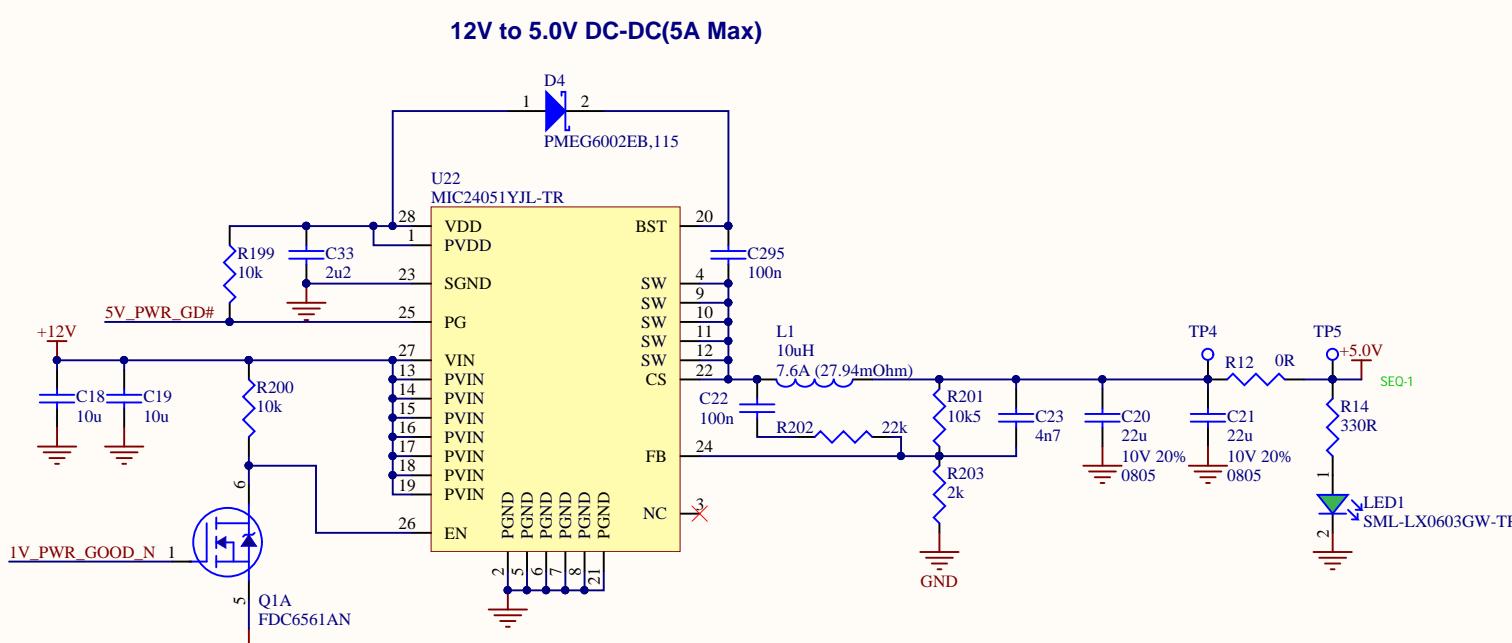
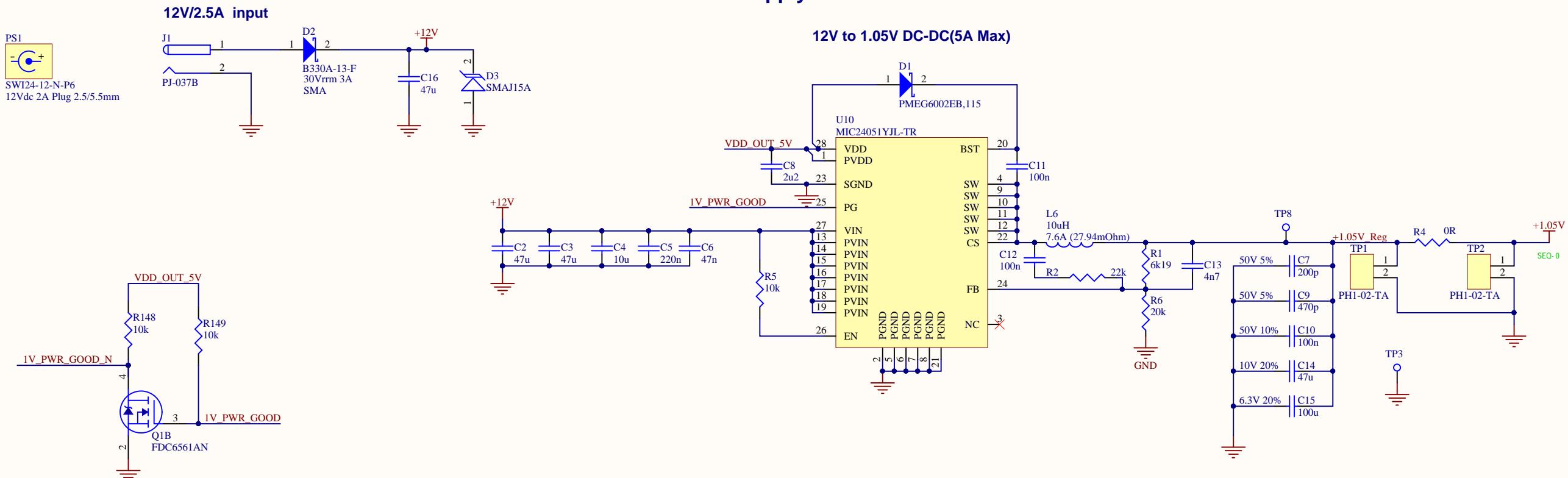
Project Name
Microsemi_Avalanche Rev 3

Title
Power supply Block diagram

Size **B** Dwg No. **FEN-412728-SCH-R3** Rev **3**

Date **1/22/2020** Sheet **2 of 16** Variant: **MCP3913**

Power supply



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Project Name
Microsemi Avalanche Rev 3

Title

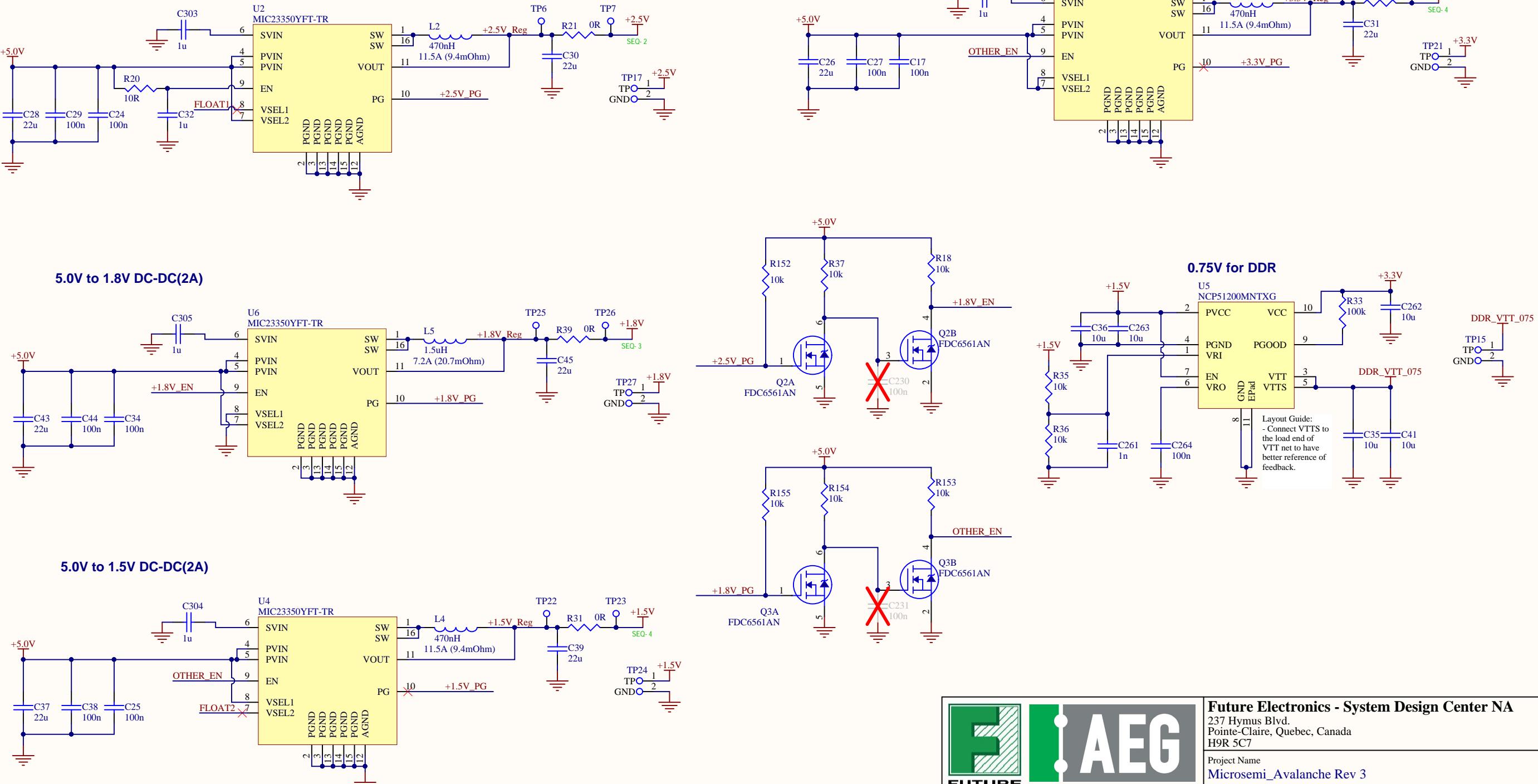
Size B Dwg No. EEN 412728 SCH B3 Rev. 5

1/22/2020 | Page 1 of 16 | MGR2013

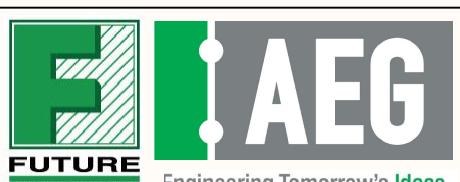
Date 1/22/2020 Sheet 5 of 10 Variant: MCP3913

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Power supply



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Project Name
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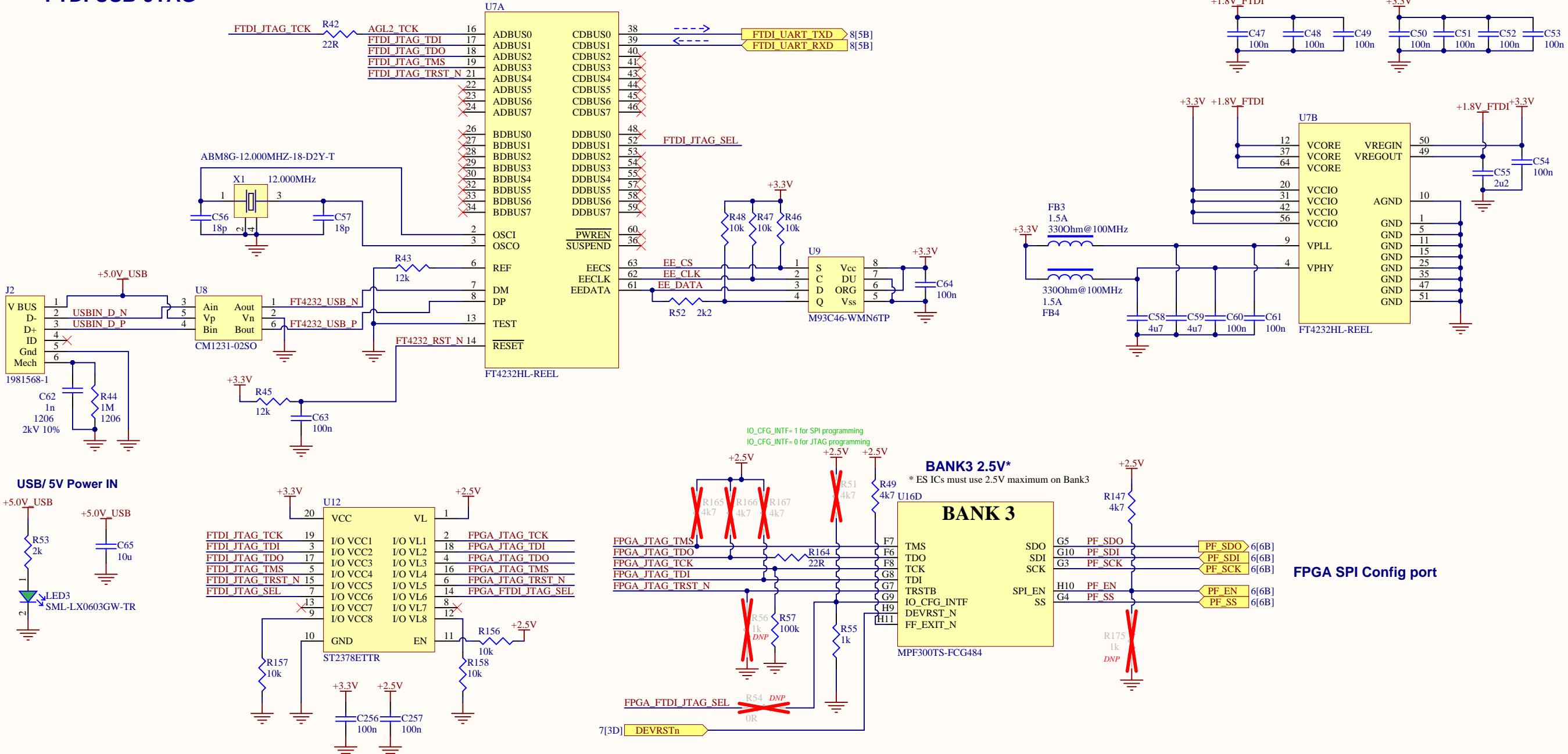
Title
Power Supply 2

Size **B** Dwg No. **FEN-412728-SCH-R3**

Rev **3**

Checked by **H. Letourneau** Approved by **M. Bernier**

Date **1/22/2020** Sheet **4 of 16** Variant: **MCP3913**

FTDI USB-JTAG

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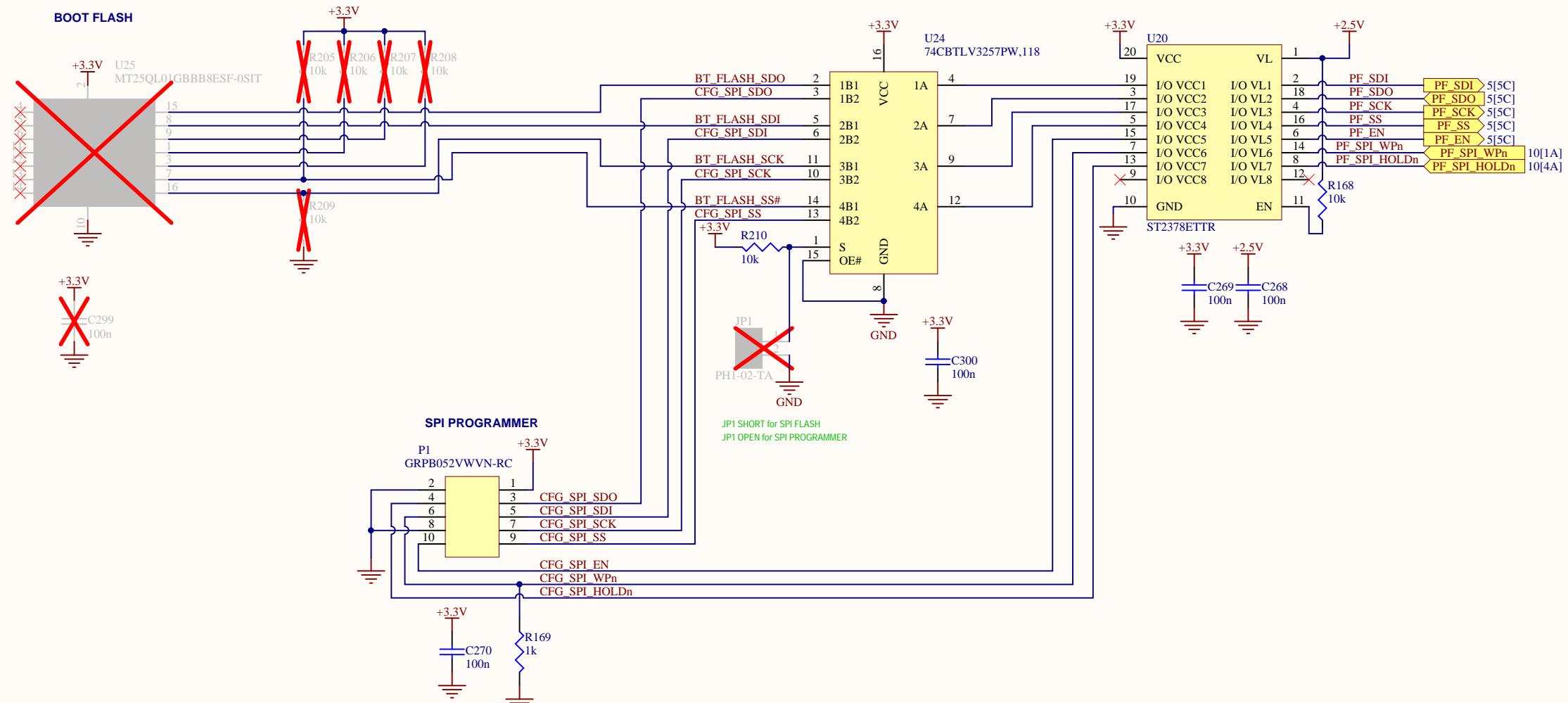
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Pointe-Claire, Quebec, Canada
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Project Name
Microsemi_Avalanche Rev 3

Title

USB - JTAGSize **B** Dwg No. **FEN-412728-SCH-R3**Rev **3**Checked by **H. Letourneau** Approved by **M. Bernier**Date **1/21/2020** Sheet **5** of **16** Variant: **MCP3913**

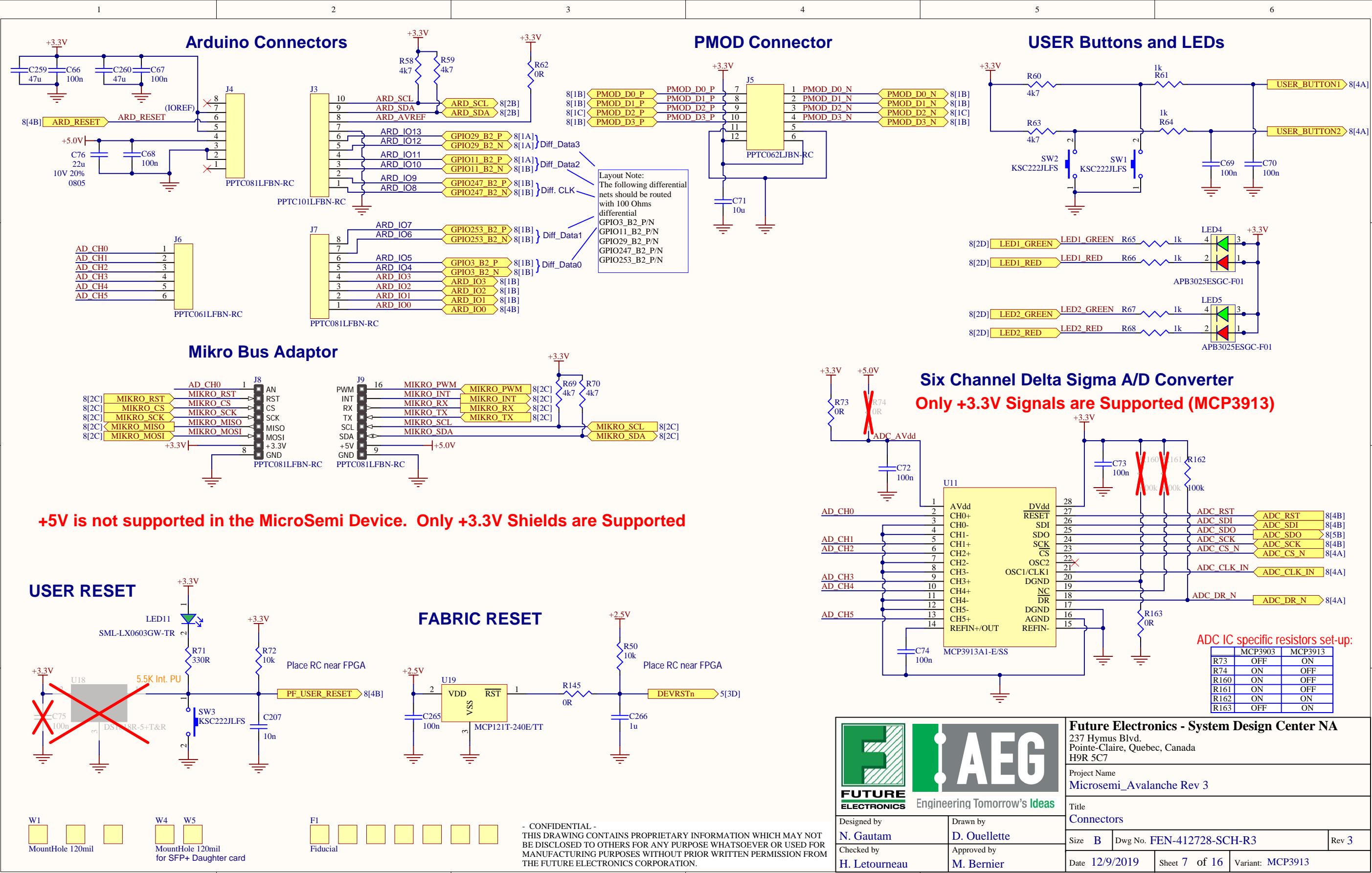
FPGA SPI Configuration

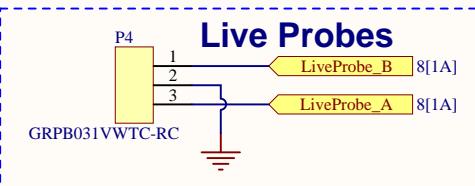


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Project Name Microsemi_Avalanche Rev 3	
Title USB - JTAG	
Size B Dwg No. FEN-412728-SCH-R3 Rev 3	
Designed by N. Gautam Drawn by D. Ouellette	
Checked by H. Letourneau Approved by M. Bernier	
Date 1/10/2020 Sheet 6 of 16 Variant: MCP3913	





Bank - 2 (3.3V)

A
Layout Note:
The Following differential nets
should be routed with 100 Ohms
differential.

Length matching:

Intra-Pair : 10mils

Inter-pairs : 50mils

GPIO3_B2_P/N

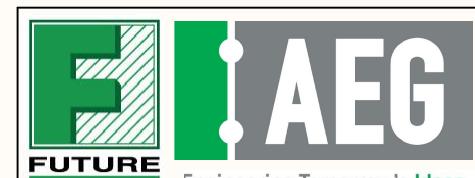
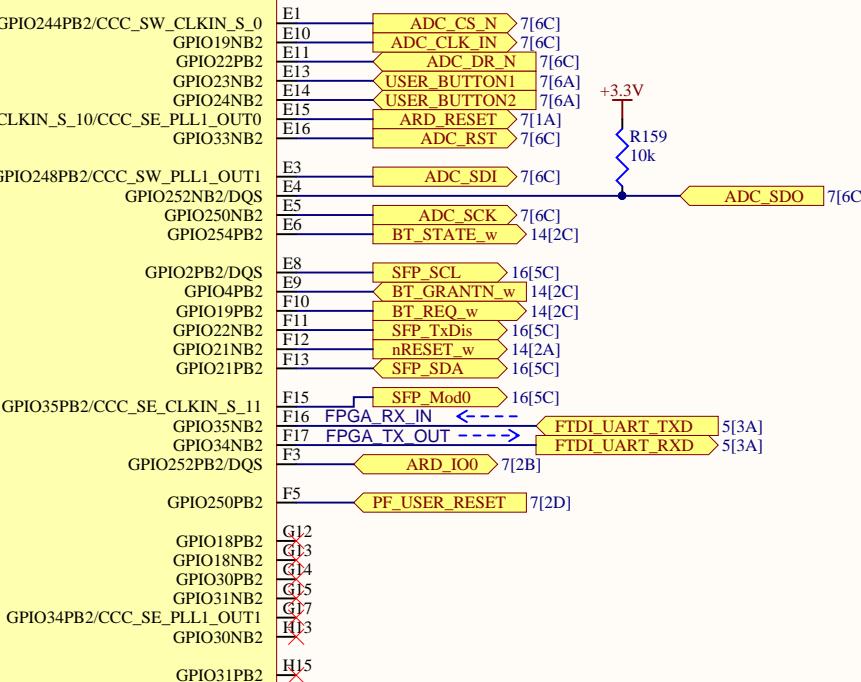
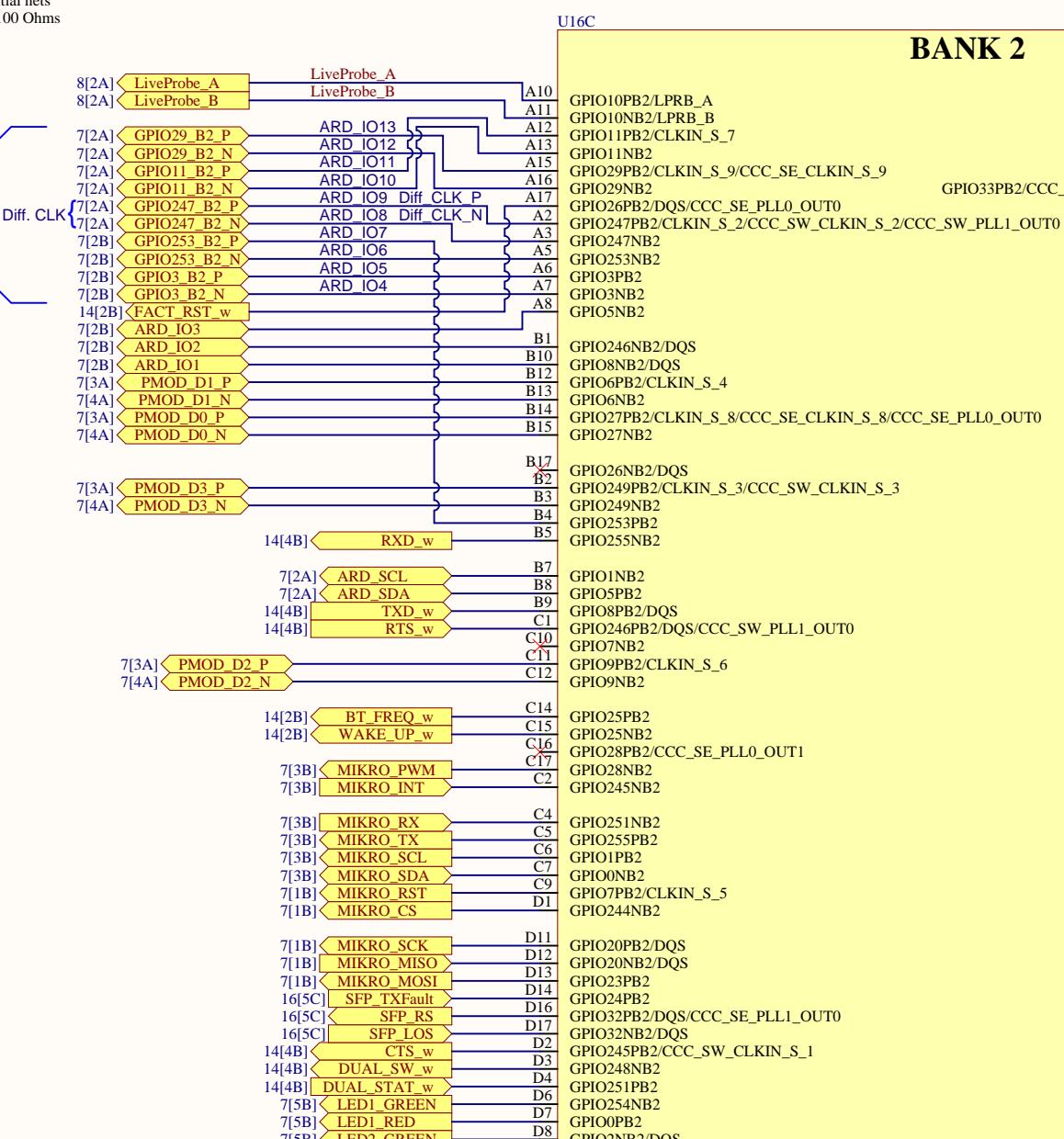
GPIO11_B2_P/N

GPIO29_B2_P/N

GPIO247_B2_P/N

GPIO253_B2_P/N

Diff. Pairs



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Project Name
Microsemi_Avalanche Rev 3

Title
FPGA Bank 2

Size **B** Dwg No. **FEN-412728-SCH-R3**

Rev **3**

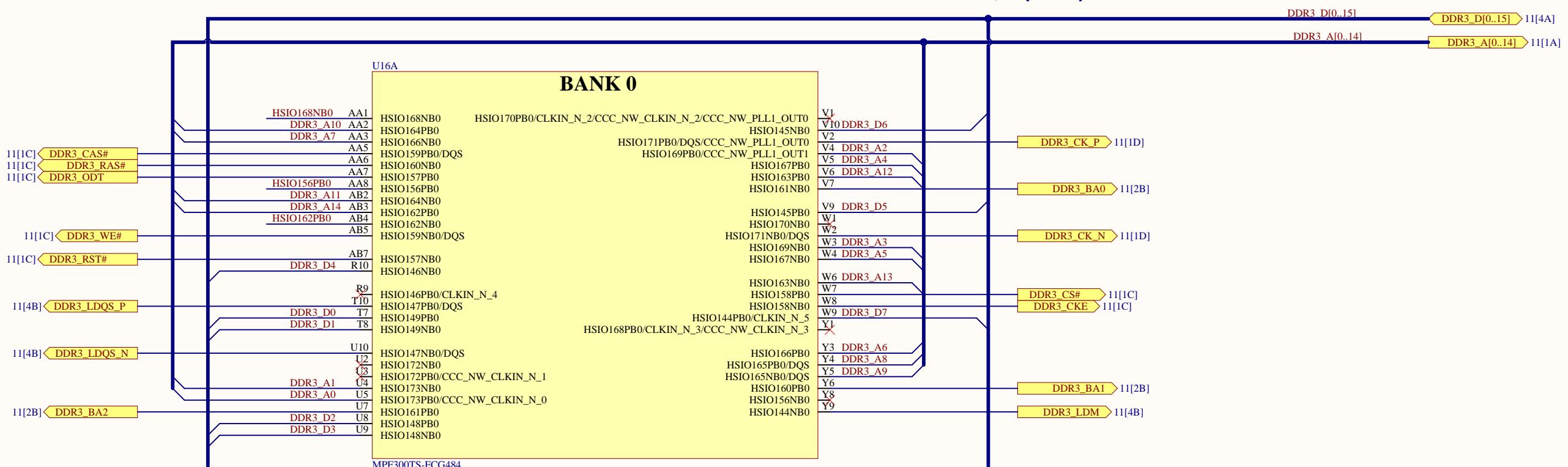
Checked by **H. Letourneau** Approved by **M. Bernier**

Date **1/21/2020** Sheet **8** of **16** Variant: **MCP3913**

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Bank - 0, 1 (1.5V)



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Project Name
Microsemi_Avalanche Rev 3

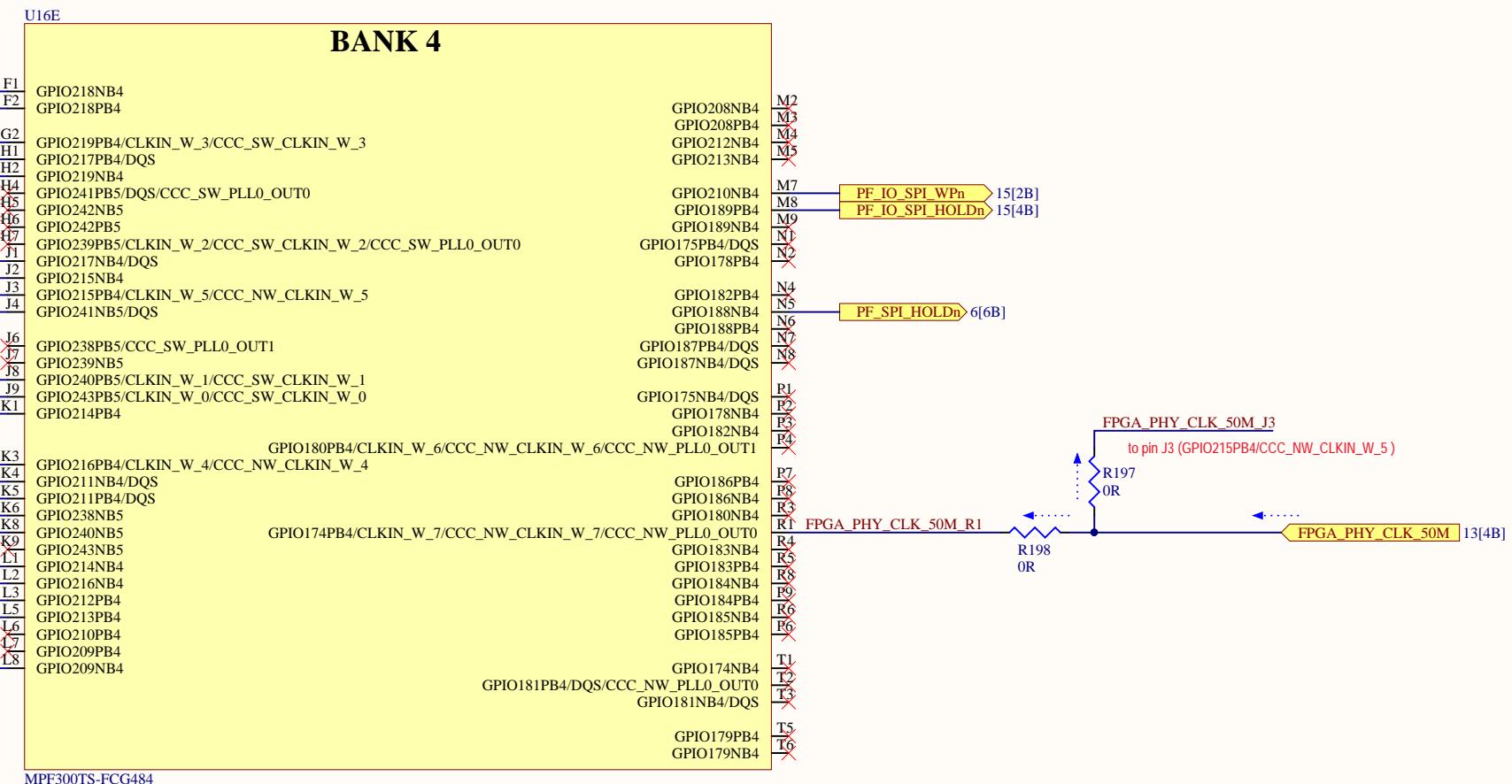
Title
FPGA Bank 0,1

Size **B** Dwg No. **FEN-412728-SCH-R3**

Rev **3**

Date **1/21/2020** Sheet **9 of 16** Variant: **MCP3913**

Bank - 4 (2.5V)



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Project Name
Microsemi_Avalanche Rev 3

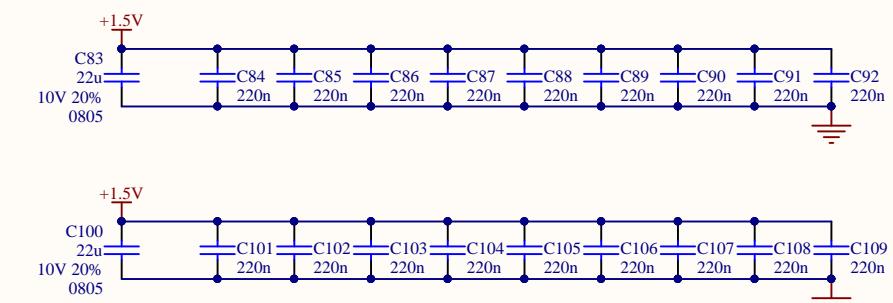
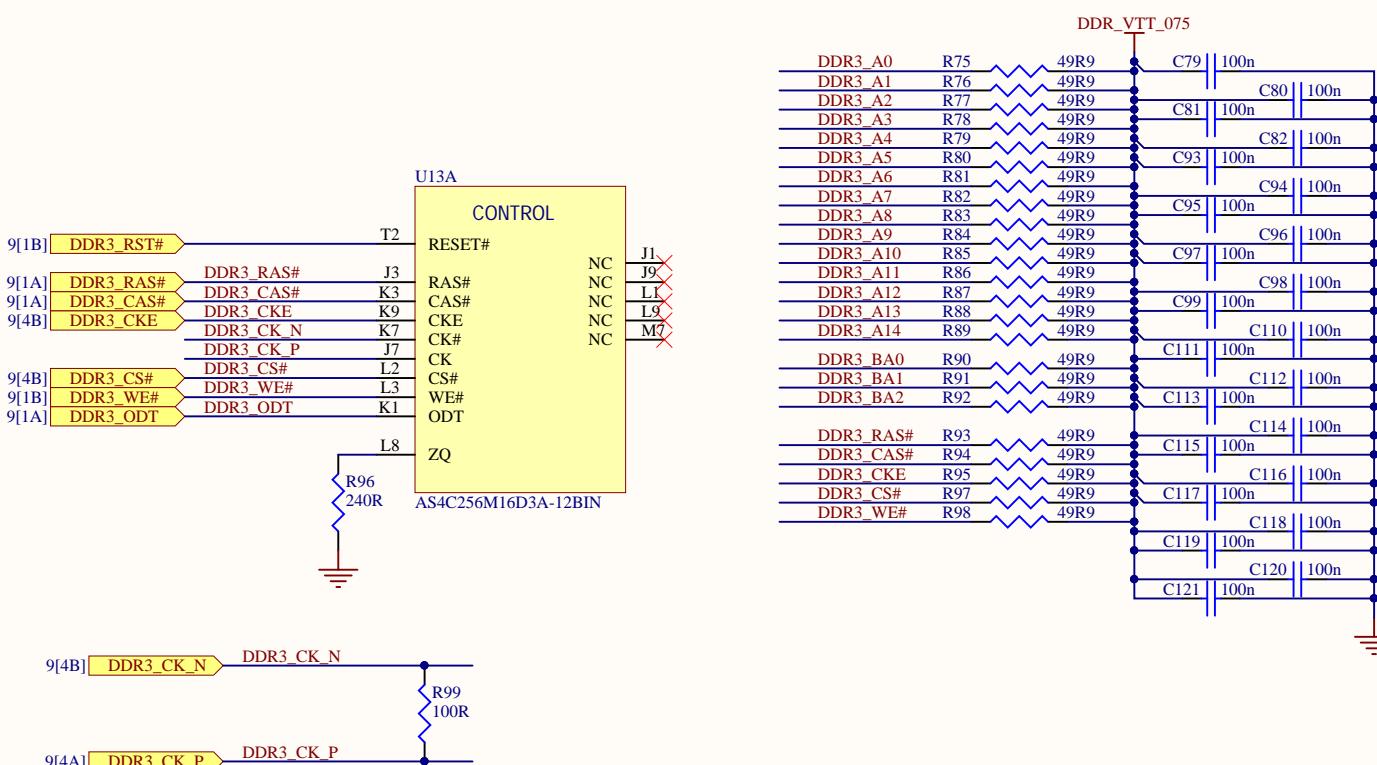
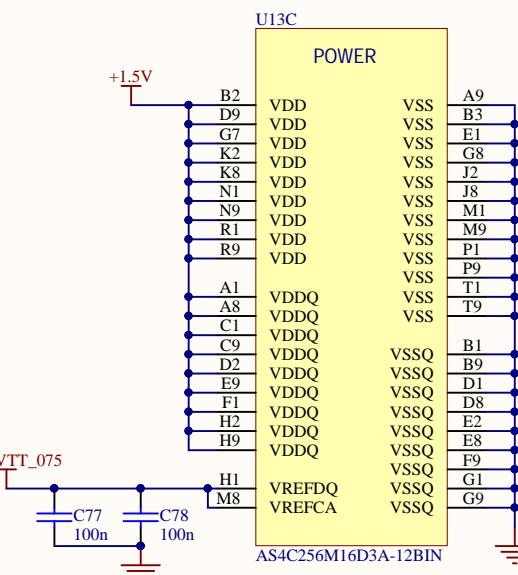
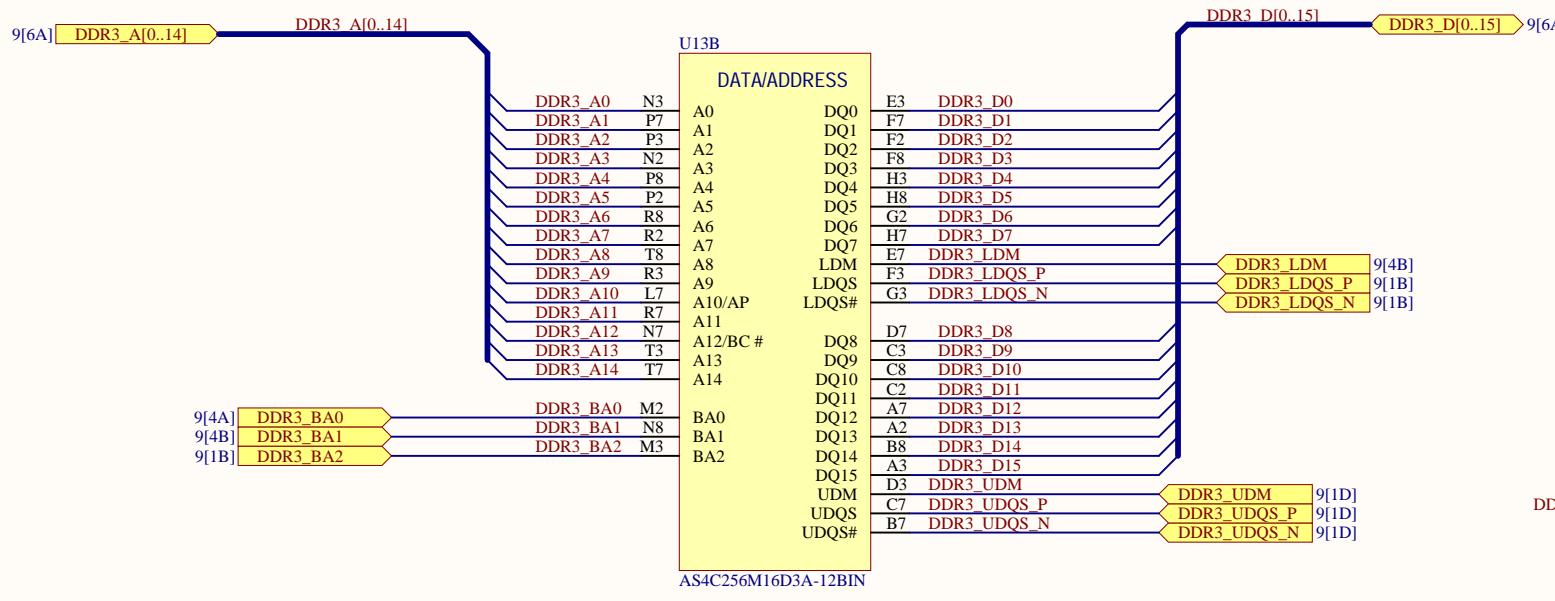
Title
FPGA Bank 4

Size **B** Dwg No. **FEN-412728-SCH-R3**

Rev **3**

Designed by **N. Gautam** Drawn by **D. Ouellette**
Checked by **H. Letourneau** Approved by **M. Bernier**

Date **1/21/2020** Sheet **10 of 16** Variant: **MCP3913**

DDR3

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Project Name
Microsemi_Avalanche Rev 3

Title

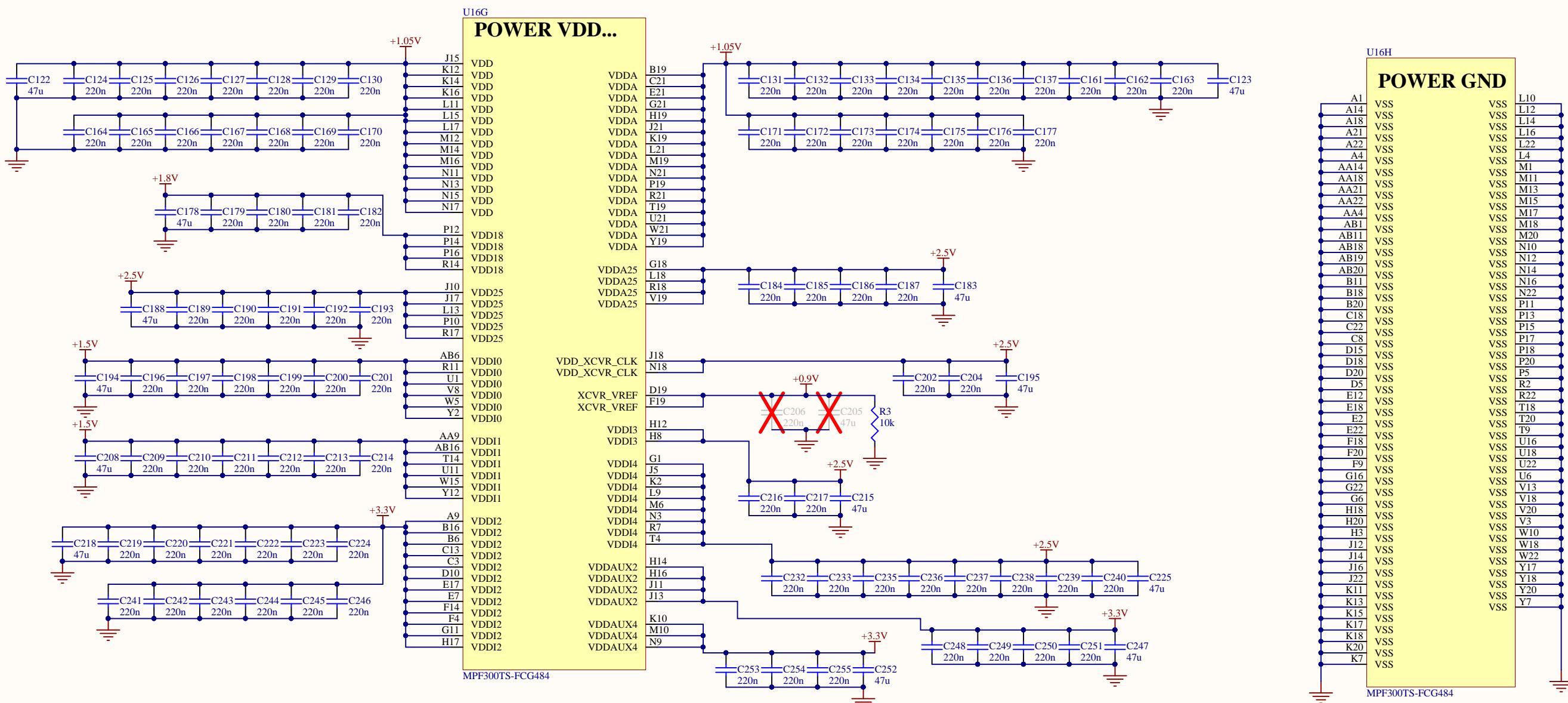
DDR3

Size **B** Dwg No. **FEN-412728-SCH-R3**

Rev **3**

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Date **11/7/2019** Sheet **11 of 16** Variant: **MCP3913**

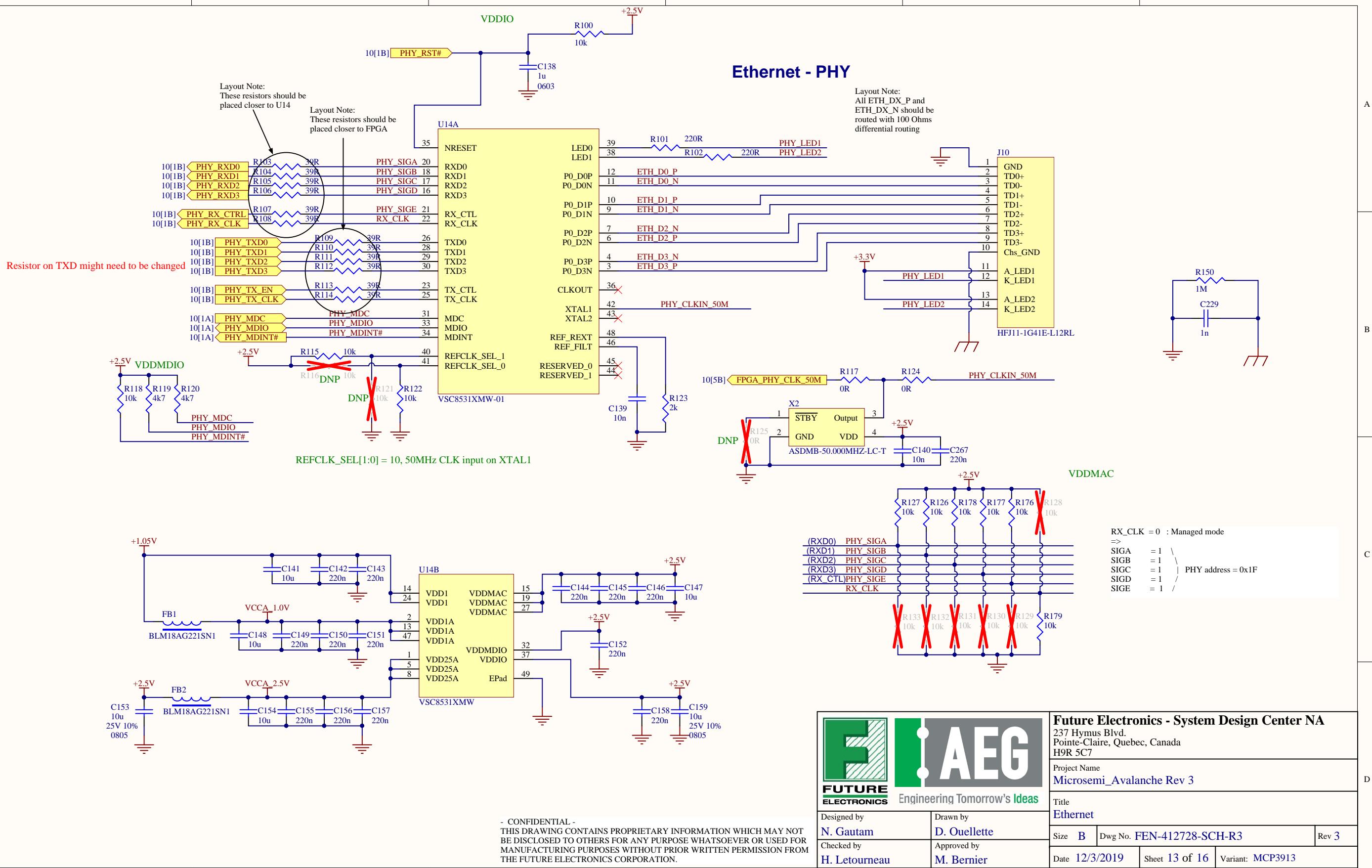


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237 Hymus Blvd. Pointe-Claire, Quebec, Canada H9R 5C7	
Project Name Microsemi_Avalanche Rev 3	
Title FPGA Power	
Size B Dwg No. FEN-412728-SCH-R3 Rev 3	
Designed by N. Gautam Drawn by D. Ouellette	
Checked by H. Letourneau Approved by M. Bernier	
Date 1/21/2020 Sheet 12 of 16 Variant: MCP3913	

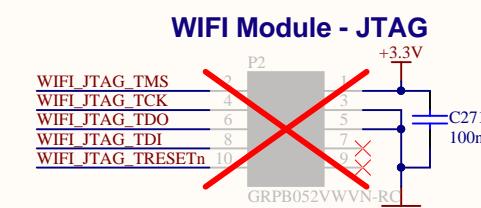
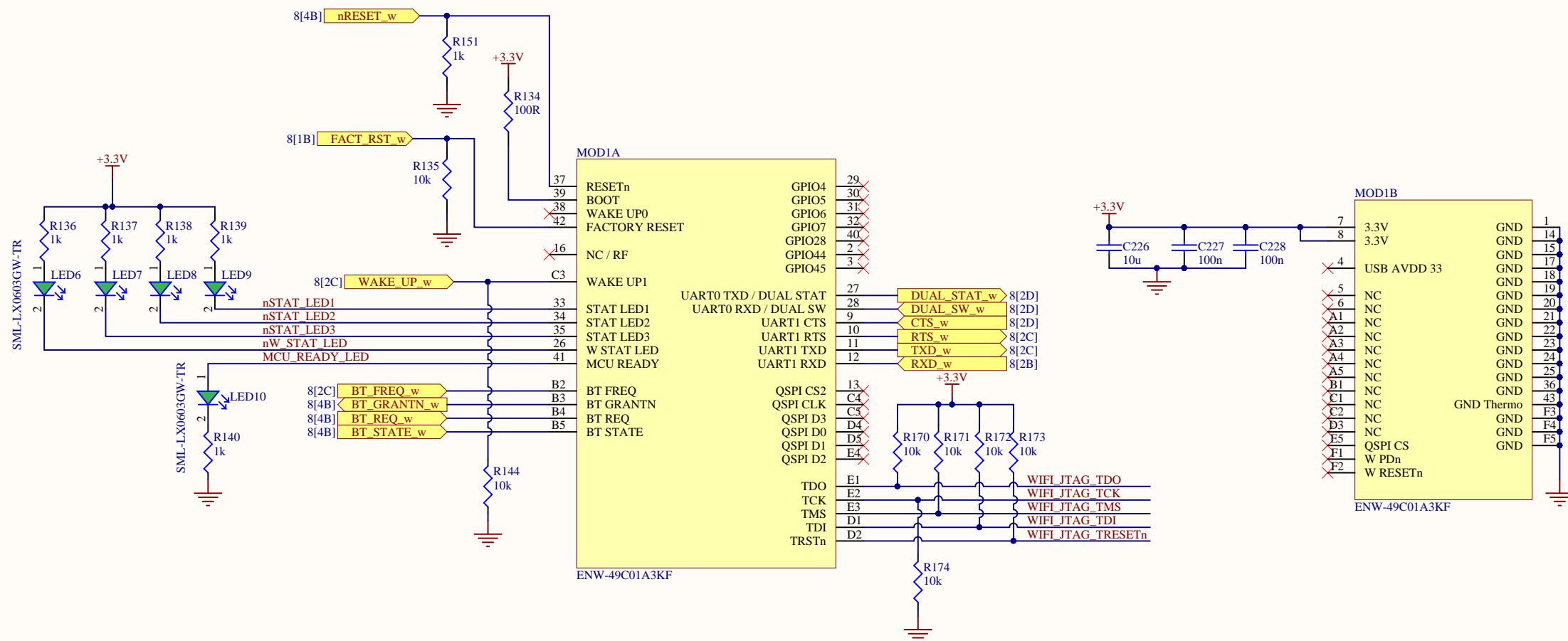
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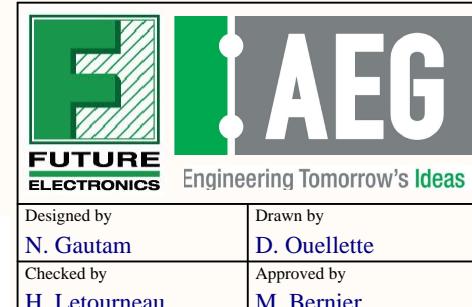


WiFi (PAN9420)



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Project Name
Microsemi_Avalanche Rev 3

Title
WiFi BLE Combo

Size **B** Dwg No. **FEN-412728-SCH-R3** Rev **3**

Date **1/13/2020** Sheet **14 of 16** Variant: **MCP3913**

A

A

B

B

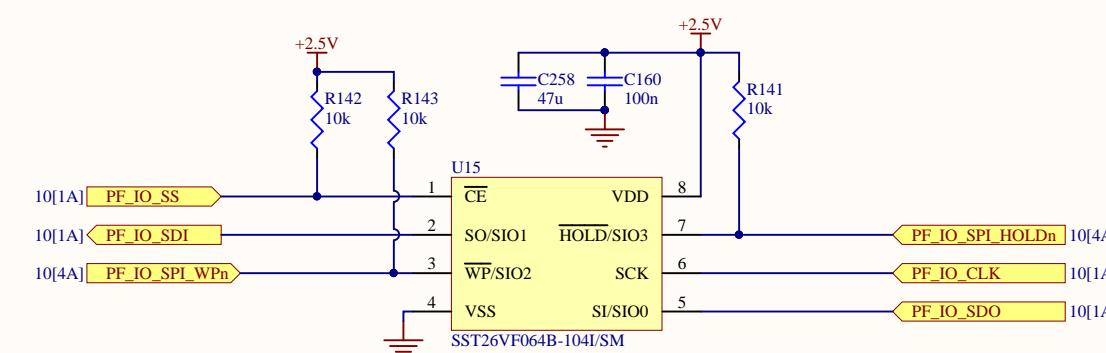
C

C

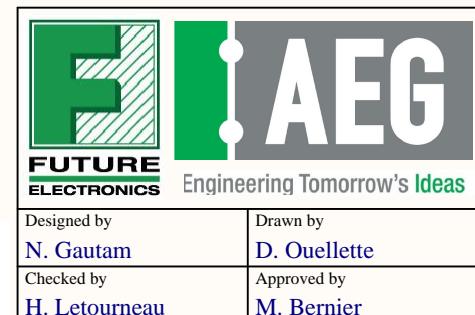
D

D

64 Mbit Serial Flash



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Project Name Microsemi_Avalanche Rev 3	
Title SPI Memory	
Size B Dwg No. FEN-412728-SCH-R3 Rev 3	
Designed by N. Gautam Drawn by D. Ouellette	
Checked by H. Letourneau Approved by M. Bernier	
Date 11/7/2019 Sheet 15 of 16 Variant: MCP3913	

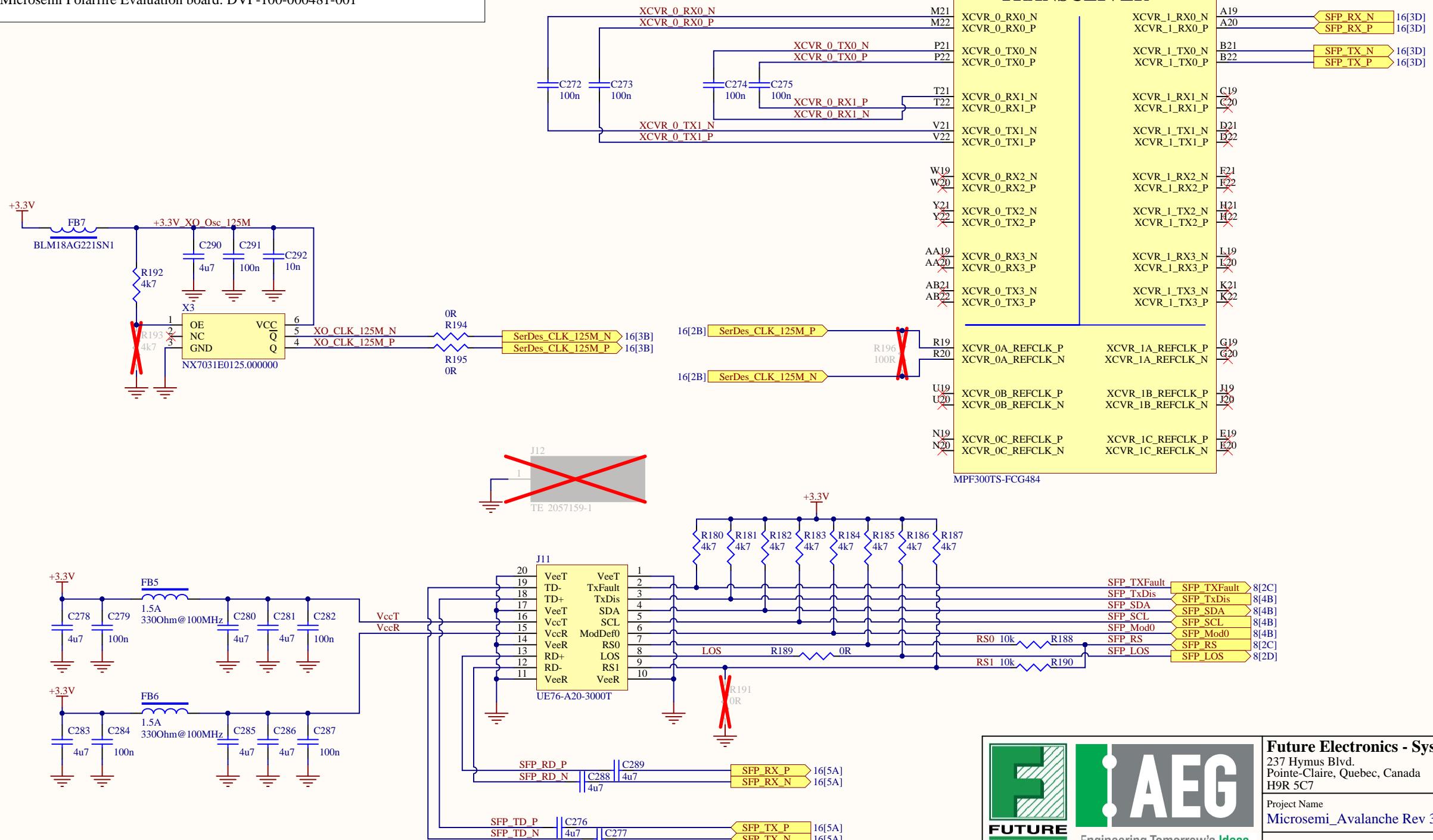
Note on Serdes:

The SerDes implementation provided is for basic evaluation purpose only.

For high performance evaluation, please call your Future Electronics Representative:

=> Microsemi Polarfire Evaluation board: DVP-100-000481-001

Transceiver - (3.3V)



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Project Name
Microsemi_Avalanche Rev 3

Title
Transceiver

Size **B** Dwg No. **FEN-412728-SCH-R3**

Rev **3**

Date **1/21/2020** Sheet **16 of 16** Variant: **MCP3913**

Impedance Requirements

Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)	
Top Layer	5mil	5mil	10mil	4mil	10mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Bottom Layer	5mil	5mil	10mil	4mil	10mil	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top_Sig_1	Copper	2.10mil		
4	Dielectric1	FR-4 HTg	3.80mil	4.6	
5	GND_1	Copper	0.70mil		
6	Dielectric 4		7.00mil	4.6	
7	Mid1_Sig_2	Copper	0.70mil		
8	Dielectric2	FR-4 HTg	12.00mil	4.6	
9	Power_1	Copper	1.40mil		
10	Dielectric 5		5.00mil	4.6	
11	Power_2	Copper	1.40mil		
12	Dielectric 7		12.00mil	4.6	
13	Mid2-Sig_3	Copper	0.70mil		
14	Dielectric 8		7.00mil	4.6	
15	GND_2	Copper	0.70mil		
16	Dielectric3	FR-4 HTg	3.80mil	4.6	
17	Bottom_Sig_4	Copper	2.10mil		
18	Bottom Solder	Solder Resist	0.40mil	3.5	
19	Bottom Overlay				

NOTES: < UNLESS OTHERWISE SPECIFIED >

1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET
ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)2. BASE MATERIAL - FR4 High Tg Metal Core Other
- Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL
TO 170°C

3. COPPER FOIL WEIGHT - SEE TABLE FOR STACK-UP DETAIL

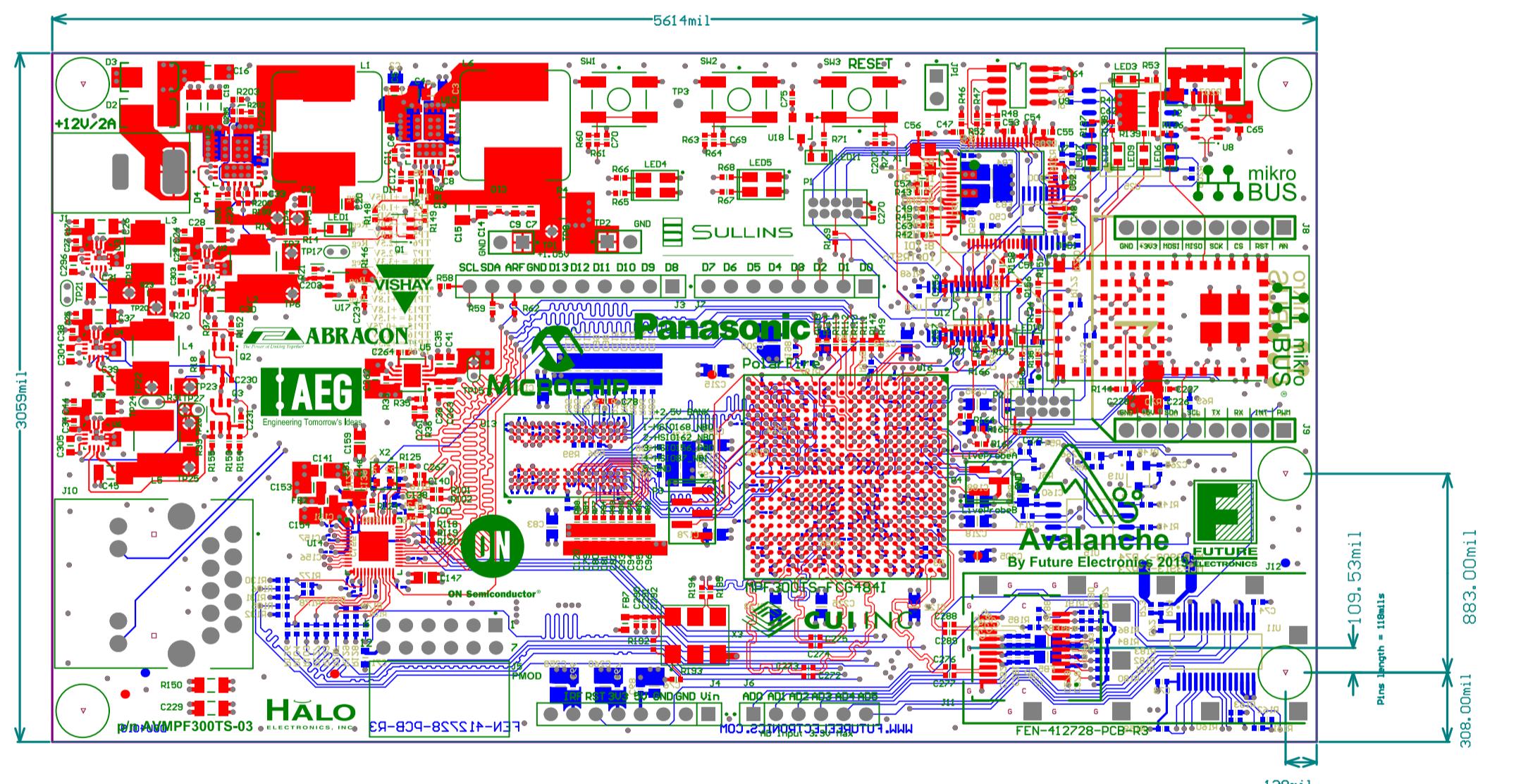
4. PLATING - 0.5oz 0.75oz 1oz Other 5. FINISH - HASL RoHS HASL Immersion Silver Immersion Tin ENIG
Other 6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-840 ON PCB OVER BARE COPPER
- GREEN WHITE BLUE Other 7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
- TOP/BOTTOM TOP ONLY BOTTOM ONLY NONE
- WHITE BLACK Other 8. IMPEDANCE CONTROL - NO YES SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

10. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP
- ALL HOLES LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM

11. GERBER FILES - SUPPLIED GERBER FILES MUST NOT BE MODIFIED WITHOUT PRIOR PERMISSION FROM THE CLIENT

12. LOGO - ONLY LOGOS SUPPLIED IN GERBER FILES WILL BE ACCEPTED ON PCB

13. TOOLING HOLES - NO HOLES SHALL BE PERMITTED WITHIN THE BOARD AREA, EXCEPT THOSE INDICATED
IN THE DRILL LEGEND14. REGISTRATION - REGISTRATION OF PATTERNS TO BE WITHIN +/- .005 LOCATION OF PATTERN ON BOARD
TO DIMENSION SHOWN

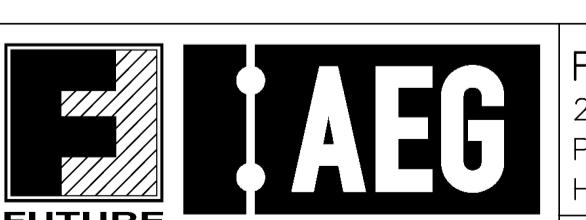
Top_Sig_1

Bottom_Sig_4

Symbol	Count	Hole Size	Hole Length	Routed Path Length	Plated	Hole Type
E	1	37.00mil (0.93mm)	-	-	PTH	Round
H	1	38.39mil (1.00mm)	118.11mil (3.00mm)	78.74mil (2.00mm)	PTH	Round
O	1	39.37mil (1.00mm)	137.80mil (3.50mm)	98.43mil (2.50mm)	PTH	Star
F	2	47.24mil (1.20mm)	-	-	PTH	Round
C	2	61.02mil (1.55mm)	-	-	PTH	Round
●	2	64.17mil (1.65mm)	-	-	PTH	Round
□	2	128.00mil (3.25mm)	-	-	PTH	Round
▽	2	118.11mil (3.00mm)	-	-	PTH	Round
×	5	14.14mil (0.35mm)	-	-	PTH	Round
×	9	7.87mil (0.20mm)	-	-	PTH	Round
G	9	21.34mil (0.55mm)	-	-	PTH	Round
◊	10	16.00mil (0.40mm)	-	-	PTH	Round
✖	10	35.43mil (0.90mm)	-	-	PTH	Round
○	10	40.00mil (1.01mm)	-	-	PTH	Round
◎	12	20.00mil (0.50mm)	-	-	PTH	Round
D	12	25.00mil (0.63mm)	-	-	PTH	Round
□	20	27.55mil (0.70mm)	-	-	PTH	Round
✖	44	40.16mil (1.02mm)	-	-	PTH	Round
○	509	8.00mil (0.20mm)	-	-	PTH	Round
O	509	10.00mil (0.25mm)	-	-	PTH	Round
1982 Total						

Slot definitions: Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout.

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Project # Microsemi_Avalanche
Title: Avalanche Polarfire board
Size: B DWG NO: FEN-412728-PCB-R3 REV: 3
Checked by: H. Letourneau Approved by: M. Bernier
Date: 1/23/2020 Sheet 1 of 1

Impedance Requirements

Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)	
Top Layer	5mil	5mil	10mil	4mil	10mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Bottom Layer	5mil	5mil	10mil	4mil	10mil	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top_Sig_1	Copper	2.10mil		
4	Dielectric1	FR-4 HTg	3.80mil	4.6	
5	GND_1	Copper	0.70mil		
6	Dielectric 4		7.00mil	4.6	
7	Mid1_Sig_2	Copper	0.70mil		
8	Dielectric2	FR-4 HTg	12.00mil	4.6	
9	Power_1	Copper	1.40mil		
10	Dielectric 5		5.00mil	4.6	
11	Power_2	Copper	1.40mil		
12	Dielectric 7		12.00mil	4.6	
13	Mid2-Sig_3	Copper	0.70mil		
14	Dielectric 8		7.00mil	4.6	
15	GND_2	Copper	0.70mil		
16	Dielectric3	FR-4 HTg	3.80mil	4.6	
17	Bottom_Sig_4	Copper	2.10mil		
18	Bottom Solder	Solder Resist	0.40mil	3.5	
19	Bottom Overlay				

NOTES: < UNLESS OTHERWISE SPECIFIED >

1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET
ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)2. BASE MATERIAL - FR4 High Tg Metal Core Other
- Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL
TO 170°C

3. COPPER FOIL WEIGHT - SEE TABLE FOR STACK-UP DETAIL

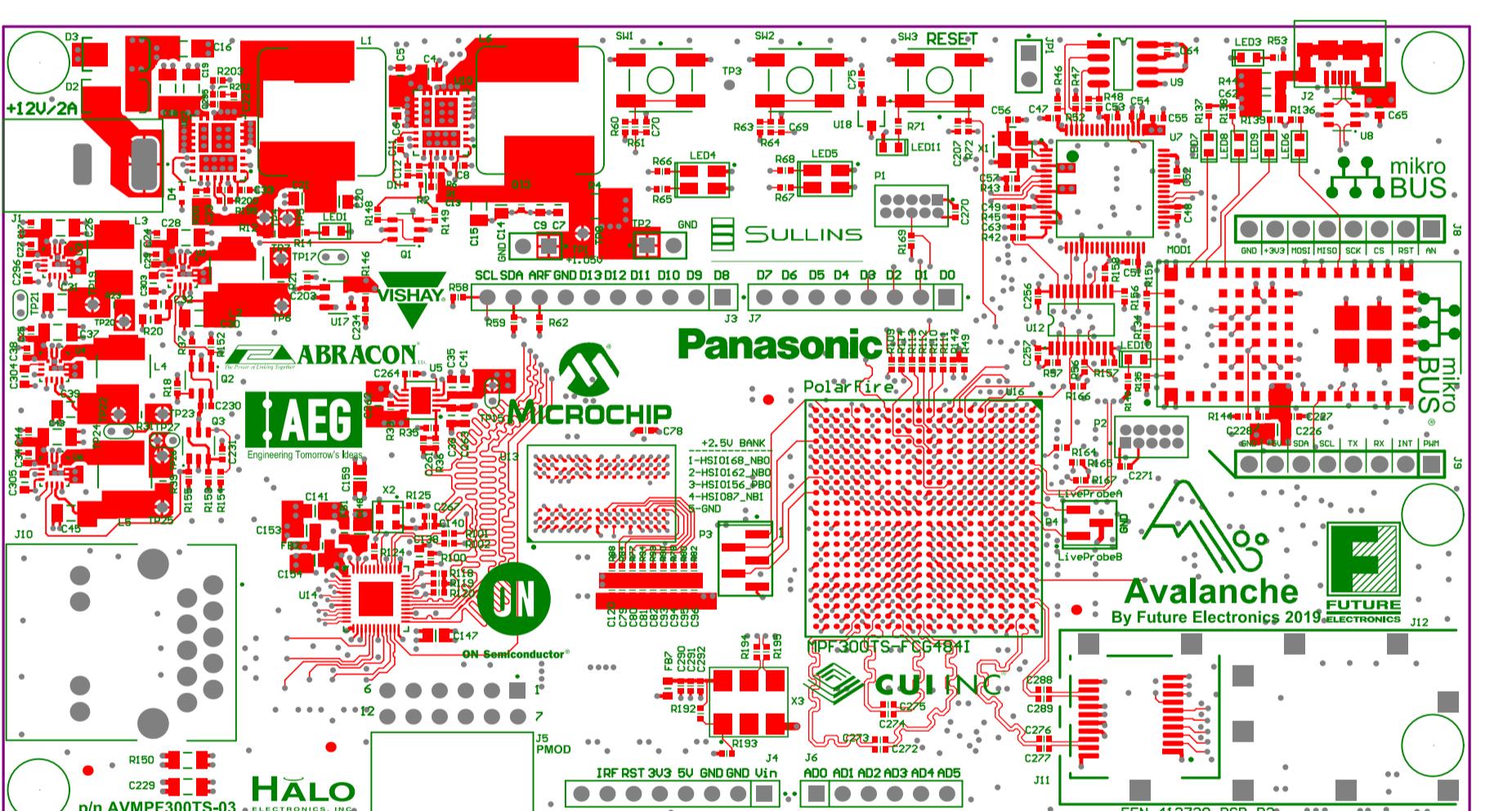
4. PLATING - 0.5oz 0.75oz 1oz Other 5. FINISH - HASL RoHS HASL Immersion Silver Immersion Tin ENIG
Other 6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-840 ON PCB OVER BARE COPPER
- GREEN WHITE BLUE Other 7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
- TOP/BOTTOM TOP ONLY BOTTOM ONLY NONE
- WHITE BLACK Other 8. IMPEDANCE CONTROL - NO YES SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

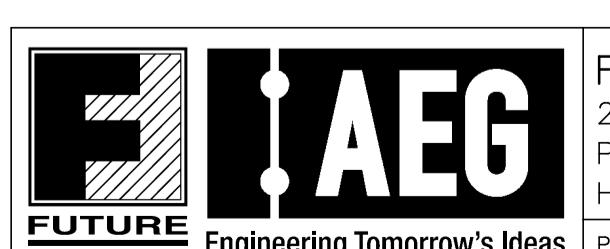
10. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP
- ALL HOLES LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM

11. GERBER FILES - SUPPLIED GERBER FILES MUST NOT BE MODIFIED WITHOUT PRIOR PERMISSION FROM THE CLIENT

12. LOGO - ONLY LOGOS SUPPLIED IN GERBER FILES WILL BE ACCEPTED ON PCB

13. TOOLING HOLES - NO HOLES SHALL BE PERMITTED WITHIN THE BOARD AREA, EXCEPT THOSE INDICATED
IN THE DRILL LEGEND14. REGISTRATION - REGISTRATION OF PATTERNS TO BE WITHIN +/- .005 LOCATION OF PATTERN ON BOARD
TO DIMENSION SHOWN

Top_Sig_1



Future Electronics – System Design Center NA
237 Hymus Blvd
Pointe-Claire, Quebec, Canada
H9R 5C7

Project #	Microsemi_Avalanche
Title:	Avalanche Polarfire board
Size:	B
DWG NO:	FEN-412728-PCB-R3
REV:	3
Date:	1/23/2020
Sheet	1 of 1

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FROM THE FUTURE ELECTRONICS CORPORATION.

Impedance Requirements

Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)	
Top Layer	5mil	5mil	10mil	4mil	10mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Bottom Layer	5mil	5mil	10mil	4mil	10mil	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top_Sig_1	Copper	2.10mil		
4	Dielectric1	FR-4 HTg	3.80mil	4.6	
5	GND_1	Copper	0.70mil		
6	Dielectric 4		7.00mil	4.6	
7	Mid1_Sig_2	Copper	0.70mil		
8	Dielectric2	FR-4 HTg	12.00mil	4.6	
9	Power_1	Copper	1.40mil		
10	Dielectric 5		5.00mil	4.6	
11	Power_2	Copper	1.40mil		
12	Dielectric 7		12.00mil	4.6	
13	Mid2-Sig_3	Copper	0.70mil		
14	Dielectric 8		7.00mil	4.6	
15	GND_2	Copper	0.70mil		
16	Dielectric3	FR-4 HTg	3.80mil	4.6	
17	Bottom_Sig_4	Copper	2.10mil		
18	Bottom Solder	Solder Resist	0.40mil	3.5	
19	Bottom Overlay				

NOTES: < UNLESS OTHERWISE SPECIFIED >

1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET
ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)2. BASE MATERIAL - FR4 High Tg Metal Core Other
- Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL
TO 170°C

3. COPPER FOIL WEIGHT - SEE TABLE FOR STACK-UP DETAIL

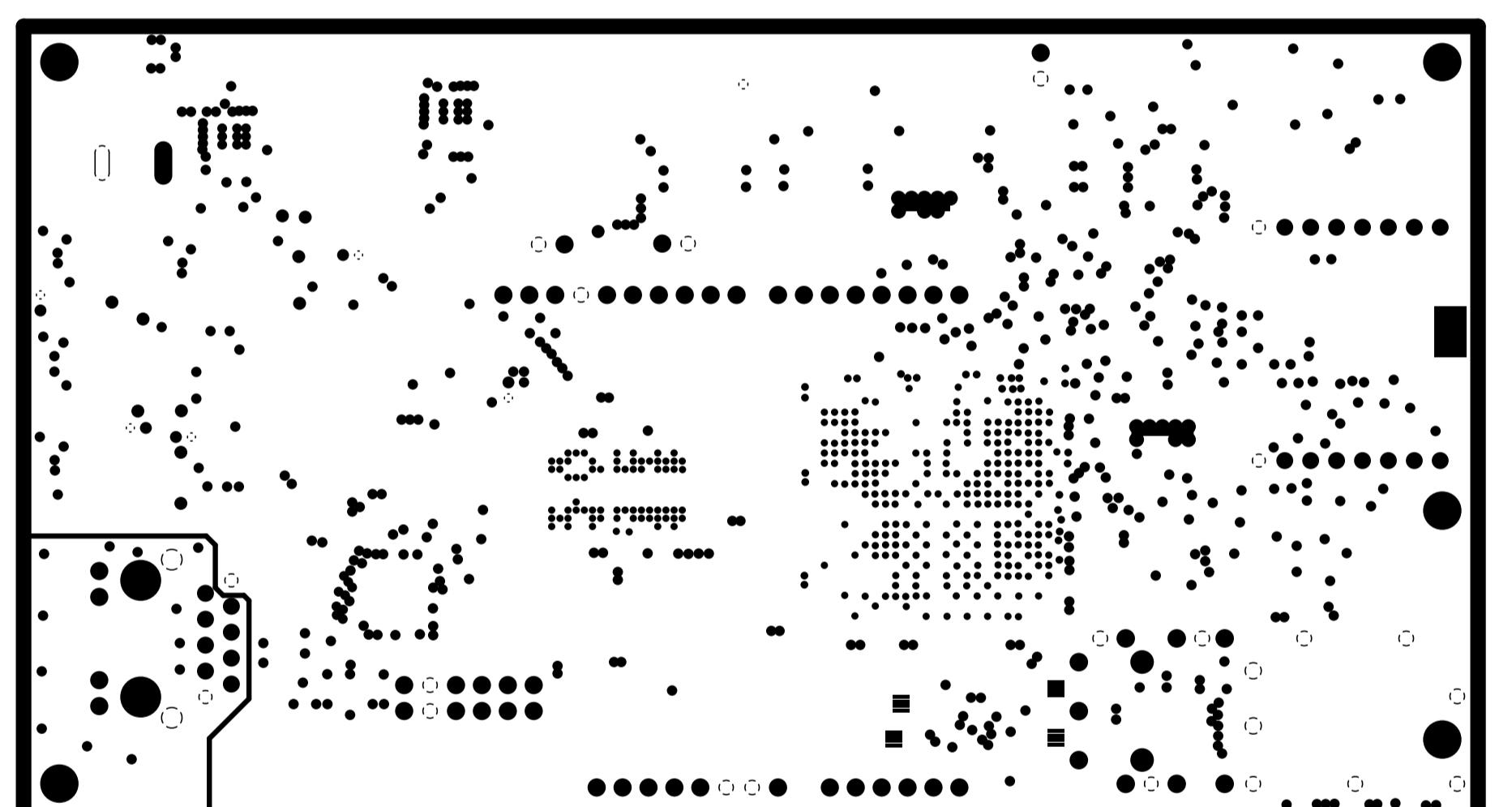
4. PLATING - 0.5oz 0.75oz 1oz Other 5. FINISH - HASL RoHS HASL Immersion Silver Immersion Tin ENIG
Other 6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-810 ON PCB OVER BARE COPPER
- GREEN WHITE BLUE Other 7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
- TOP/BOTTOM TOP ONLY BOTTOM ONLY NONE
- WHITE BLACK Other 8. IMPEDANCE CONTROL - NO YES SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

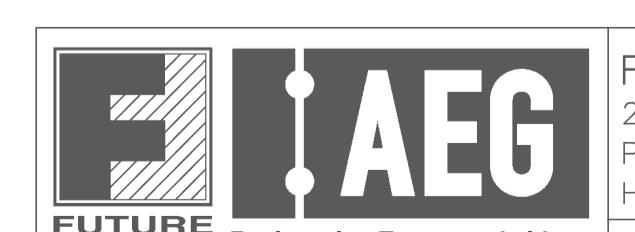
10. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP
- ALL HOLES LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM

11. GERBER FILES - SUPPLIED GERBER FILES MUST NOT BE MODIFIED WITHOUT PRIOR PERMISSION FROM THE CLIENT

12. LOGO - ONLY LOGOS SUPPLIED IN GERBER FILES WILL BE ACCEPTED ON PCB

13. TOOLING HOLES - NO HOLES SHALL BE PERMITTED WITHIN THE BOARD AREA, EXCEPT THOSE INDICATED
IN THE DRILL LEGEND14. REGISTRATION - REGISTRATION OF PATTERNS TO BE WITHIN +/- .005 LOCATION OF PATTERN ON BOARD
TO DIMENSION SHOWN

GND_1



Future Electronics – System Design Center NA
237 Hymus Blvd
Pointe-Claire, Quebec, Canada
H9R 5C7

Project #	Microsemi_Avalanche
Title:	Avalanche Polarfire board
Size: B	DWG NO: FEN-412728-PCB-R3
Date:	1/23/2020
Sheet	1 of 1

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FROM THE FUTURE ELECTRONICS CORPORATION.

Impedance Requirements

Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)	
Top Layer	5mil	5mil	10mil	4mil	10mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Bottom Layer	5mil	5mil	10mil	4mil	10mil	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top_Sig_1	Copper	2.10mil		
4	Dielectric1	FR-4 HTg	3.80mil	4.6	
5	GND_1	Copper	0.70mil		
6	Dielectric 4		7.00mil	4.6	
7	Mid1_Sig_2	Copper	0.70mil		
8	Dielectric2	FR-4 HTg	12.00mil	4.6	
9	Power_1	Copper	1.40mil		
10	Dielectric 5		5.00mil	4.6	
11	Power_2	Copper	1.40mil		
12	Dielectric 7		12.00mil	4.6	
13	Mid2-Sig_3	Copper	0.70mil		
14	Dielectric 8		7.00mil	4.6	
15	GND_2	Copper	0.70mil		
16	Dielectric3	FR-4 HTg	3.80mil	4.6	
17	Bottom_Sig_4	Copper	2.10mil		
18	Bottom Solder	Solder Resist	0.40mil	3.5	
19	Bottom Overlay				

NOTES: < UNLESS OTHERWISE SPECIFIED >

1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET
ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)2. BASE MATERIAL - FR4 High Tg Metal Core Other
- Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL
TO 170°C

3. COPPER FOIL WEIGHT - SEE TABLE FOR STACK-UP DETAIL

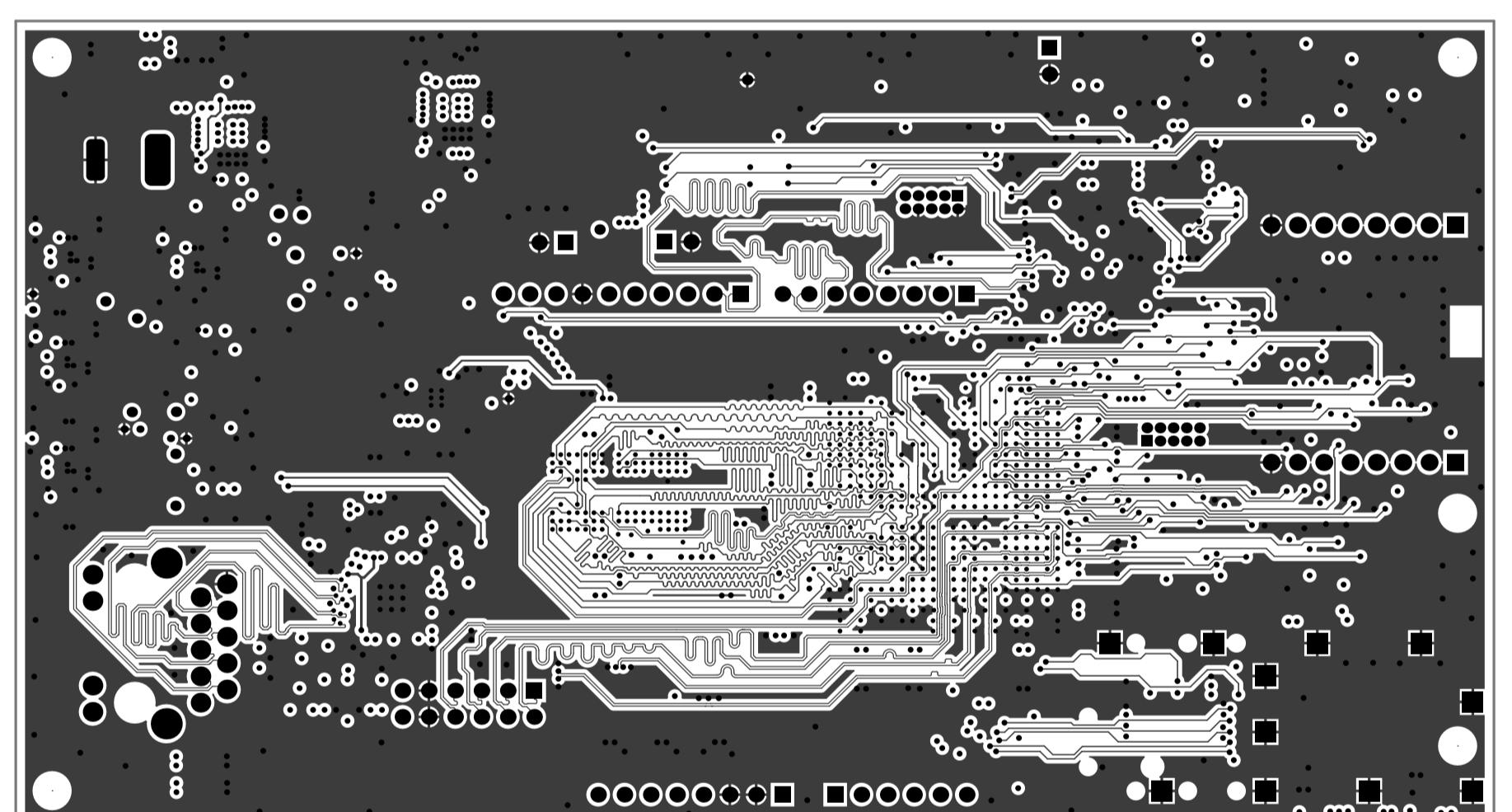
4. PLATING - 0.5oz 0.75oz 1oz Other 5. FINISH - HASL RoHS HASL Immersion Silver Immersion Tin ENIG
Other 6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-810 ON PCB OVER BARE COPPER
- GREEN WHITE BLUE Other 7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
- TOP/BOTTOM TOP ONLY BOTTOM ONLY NONE
- WHITE BLACK Other 8. IMPEDANCE CONTROL - NO YES SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

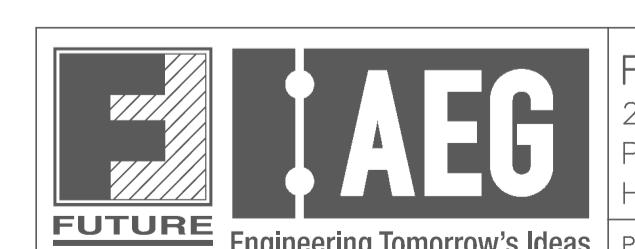
10. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP
- ALL HOLES LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM

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TO DIMENSION SHOWN

Mid1_Sig_2



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Future Electronics – System Design Center NA
237 Hymus Blvd
Pointe-Claire, Quebec, Canada
H9R 5C7
Project # Microsemi_Avalanche
Title: Avalanche Polarfire board
Size: B DWG NO: FEN-412728-PCB-R3 REV: 3
Checked by: H. Letourneau Approved by: M. Bernier
Date: 1/23/2020 Sheet 1 of 1

Impedance Requirements

Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)	
Top Layer	5mil	5mil	10mil	4mil	10mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Bottom Layer	5mil	5mil	10mil	4mil	10mil	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top_Sig_1	Copper	2.10mil		
4	Dielectric1	FR-4 HTg	3.80mil	4.6	
5	GND_1	Copper	0.70mil		
6	Dielectric 4		7.00mil	4.6	
7	Mid1_Sig_2	Copper	0.70mil		
8	Dielectric2	FR-4 HTg	12.00mil	4.6	
9	Power_1	Copper	1.40mil		
10	Dielectric 5		5.00mil	4.6	
11	Power_2	Copper	1.40mil		
12	Dielectric 7		12.00mil	4.6	
13	Mid2-Sig_3	Copper	0.70mil		
14	Dielectric 8		7.00mil	4.6	
15	GND_2	Copper	0.70mil		
16	Dielectric3	FR-4 HTg	3.80mil	4.6	
17	Bottom_Sig_4	Copper	2.10mil		
18	Bottom Solder	Solder Resist	0.40mil	3.5	
19	Bottom Overlay				

NOTES: < UNLESS OTHERWISE SPECIFIED >

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- Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL
TO 170°C

3. COPPER FOIL WEIGHT - SEE TABLE FOR STACK-UP DETAIL

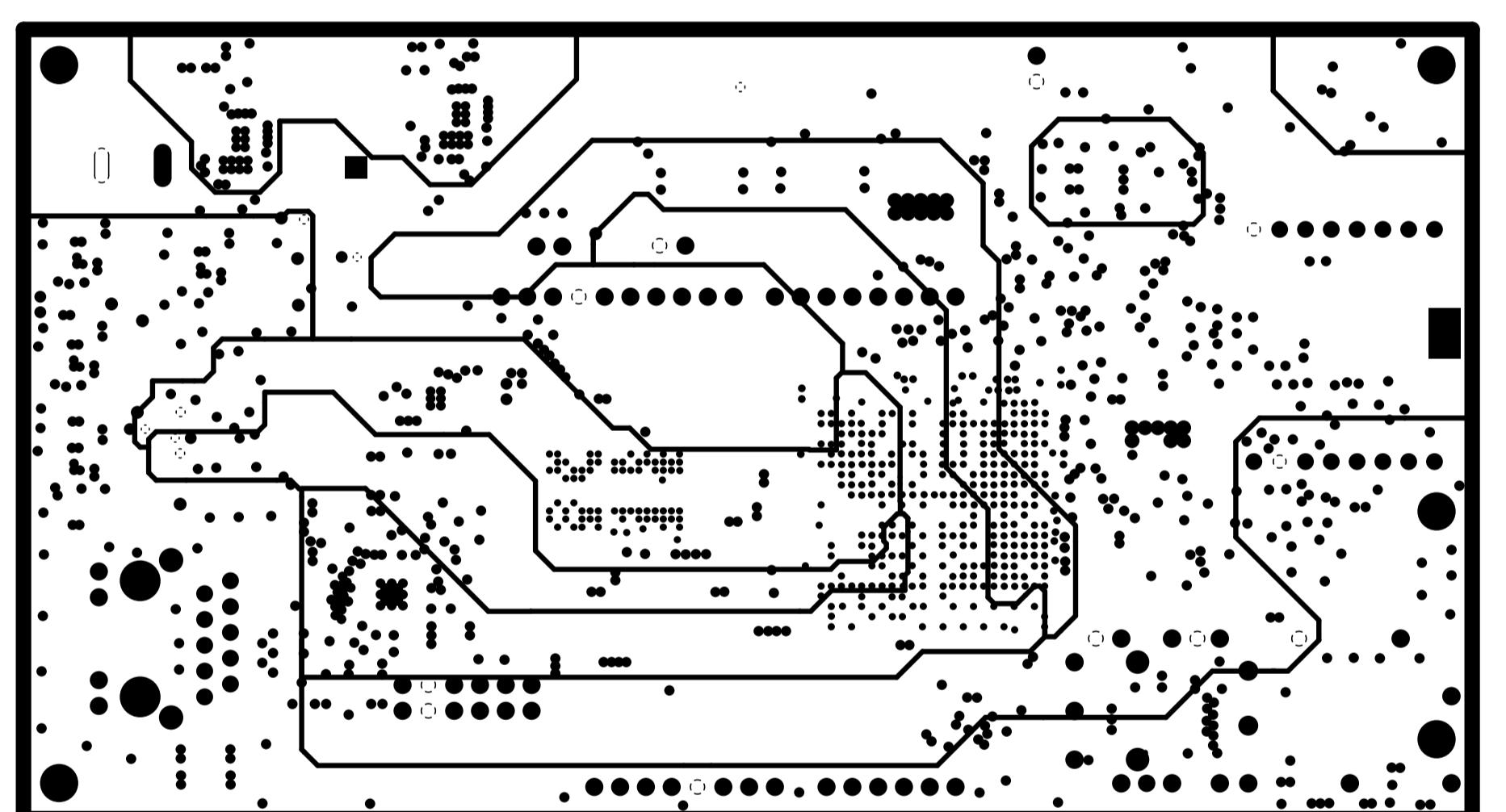
4. PLATING - 0.5oz 0.75oz 1oz Other 5. FINISH - HASL RoHS HASL Immersion Silver Immersion Tin ENIG
Other 6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-810 ON PCB OVER BARE COPPER
- GREEN WHITE BLUE Other 7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
- TOP/BOTTOM TOP ONLY BOTTOM ONLY NONE
- WHITE BLACK Other 8. IMPEDANCE CONTROL - NO YES SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

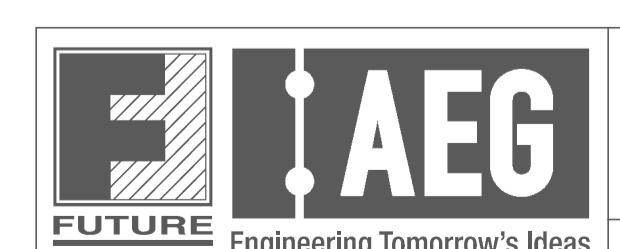
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13. TOOLING HOLES - NO HOLES SHALL BE PERMITTED WITHIN THE BOARD AREA, EXCEPT THOSE INDICATED
IN THE DRILL LEGEND14. REGISTRATION - REGISTRATION OF PATTERNS TO BE WITHIN +/- .005 LOCATION OF PATTERN ON BOARD
TO DIMENSION SHOWN

Power_1



Future Electronics – System Design Center NA
237 Hymus Blvd
Pointe-Claire, Quebec, Canada
H9R 5C7

Project #	Microsemi_Avalanche
Title:	Avalanche Polarfire board
Size: B	DWG NO: FEN-412728-PCB-R3
Date:	1/23/2020
Sheet	1 of 1

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Impedance Requirements

Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)	
Top Layer	5mil	5mil	10mil	4mil	10mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Bottom Layer	5mil	5mil	10mil	4mil	10mil	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top_Sig_1	Copper	2.10mil		
4	Dielectric1	FR-4 HTg	3.80mil	4.6	
5	GND_1	Copper	0.70mil		
6	Dielectric 4		7.00mil	4.6	
7	Mid1_Sig_2	Copper	0.70mil		
8	Dielectric2	FR-4 HTg	12.00mil	4.6	
9	Power_1	Copper	1.40mil		
10	Dielectric 5		5.00mil	4.6	
11	Power_2	Copper	1.40mil		
12	Dielectric 7		12.00mil	4.6	
13	Mid2-Sig_3	Copper	0.70mil		
14	Dielectric 8		7.00mil	4.6	
15	GND_2	Copper	0.70mil		
16	Dielectric3	FR-4 HTg	3.80mil	4.6	
17	Bottom_Sig_4	Copper	2.10mil		
18	Bottom Solder	Solder Resist	0.40mil	3.5	
19	Bottom Overlay				

NOTES: < UNLESS OTHERWISE SPECIFIED >

1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET
ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)2. BASE MATERIAL - FR4 High Tg Metal Core Other
- Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL
TO 170°C

3. COPPER FOIL WEIGHT - SEE TABLE FOR STACK-UP DETAIL

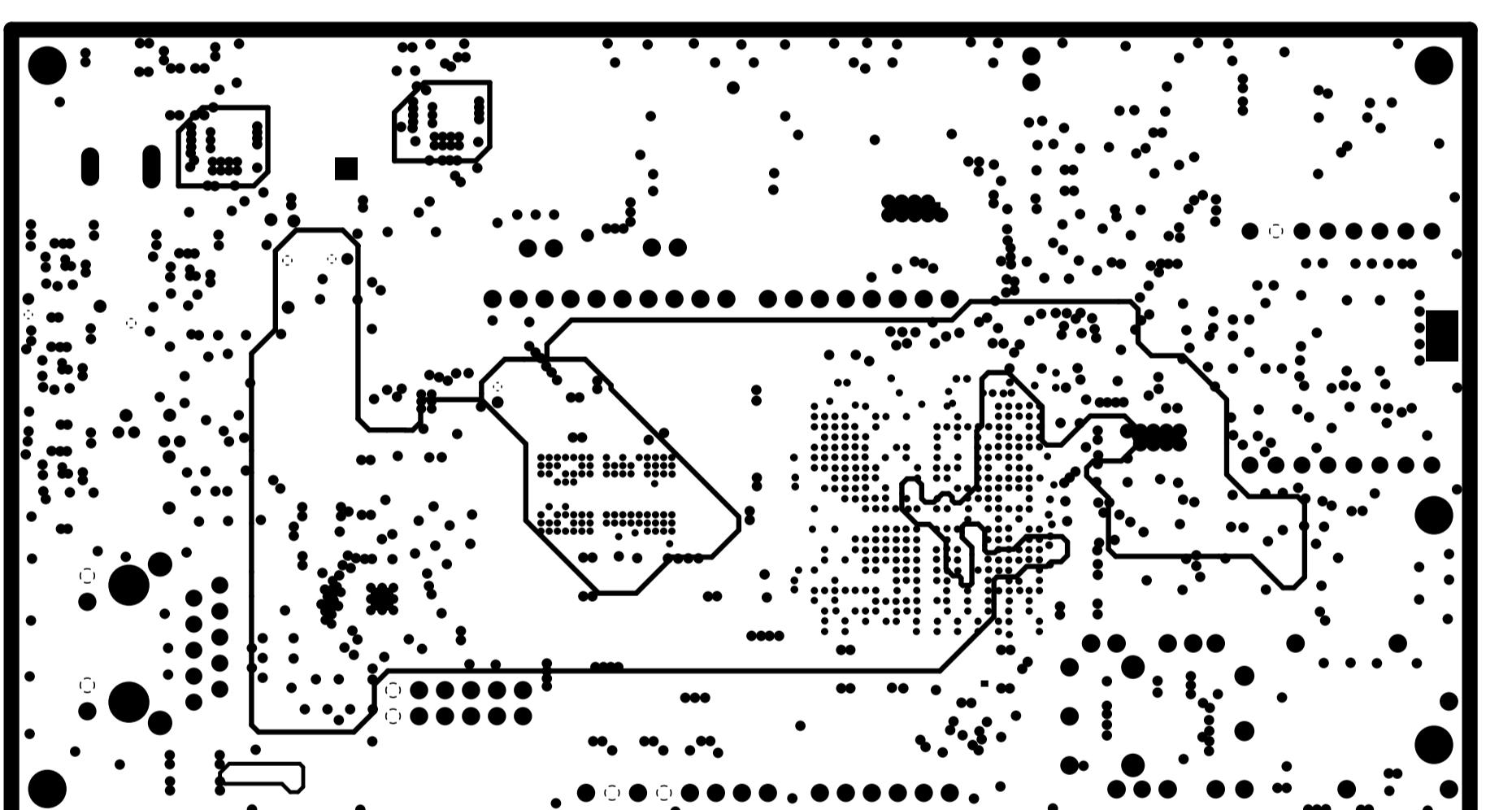
4. PLATING - 0.5oz 0.75oz 1oz Other 5. FINISH - HASL RoHS HASL Immersion Silver Immersion Tin ENIG
Other 6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-810 ON PCB OVER BARE COPPER
- GREEN WHITE BLUE Other 7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
- TOP/BOTTOM TOP ONLY BOTTOM ONLY NONE
- WHITE BLACK Other 8. IMPEDANCE CONTROL - NO YES SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

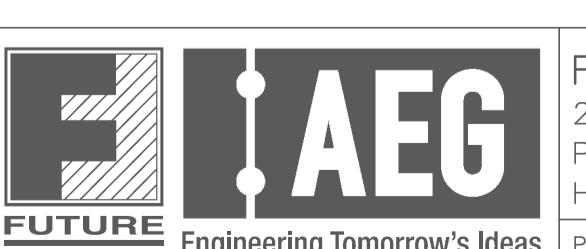
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TO DIMENSION SHOWN

Power_2



Future Electronics – System Design Center NA
237 Hymus Blvd
Pointe-Claire, Quebec, Canada
H9R 5C7

Project #	Microsemi_Avalanche
Title:	Avalanche Polarfire board
Size: B	DWG NO: FEN-412728-PCB-R3
Date:	1/23/2020
Sheet	1 of 1

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Impedance Requirements

Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)	
Top Layer	5mil	5mil	10mil	4mil	10mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Bottom Layer	5mil	5mil	10mil	4mil	10mil	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top_Sig_1	Copper	2.10mil		
4	Dielectric1	FR-4 HTg	3.80mil	4.6	
5	GND_1	Copper	0.70mil		
6	Dielectric 4		7.00mil	4.6	
7	Mid1_Sig_2	Copper	0.70mil		
8	Dielectric2	FR-4 HTg	12.00mil	4.6	
9	Power_1	Copper	1.40mil		
10	Dielectric 5		5.00mil	4.6	
11	Power_2	Copper	1.40mil		
12	Dielectric 7		12.00mil	4.6	
13	Mid2-Sig_3	Copper	0.70mil		
14	Dielectric 8		7.00mil	4.6	
15	GND_2	Copper	0.70mil		
16	Dielectric3	FR-4 HTg	3.80mil	4.6	
17	Bottom_Sig_4	Copper	2.10mil		
18	Bottom Solder	Solder Resist	0.40mil	3.5	
19	Bottom Overlay				

NOTES: < UNLESS OTHERWISE SPECIFIED >

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3. COPPER FOIL WEIGHT - SEE TABLE FOR STACK-UP DETAIL

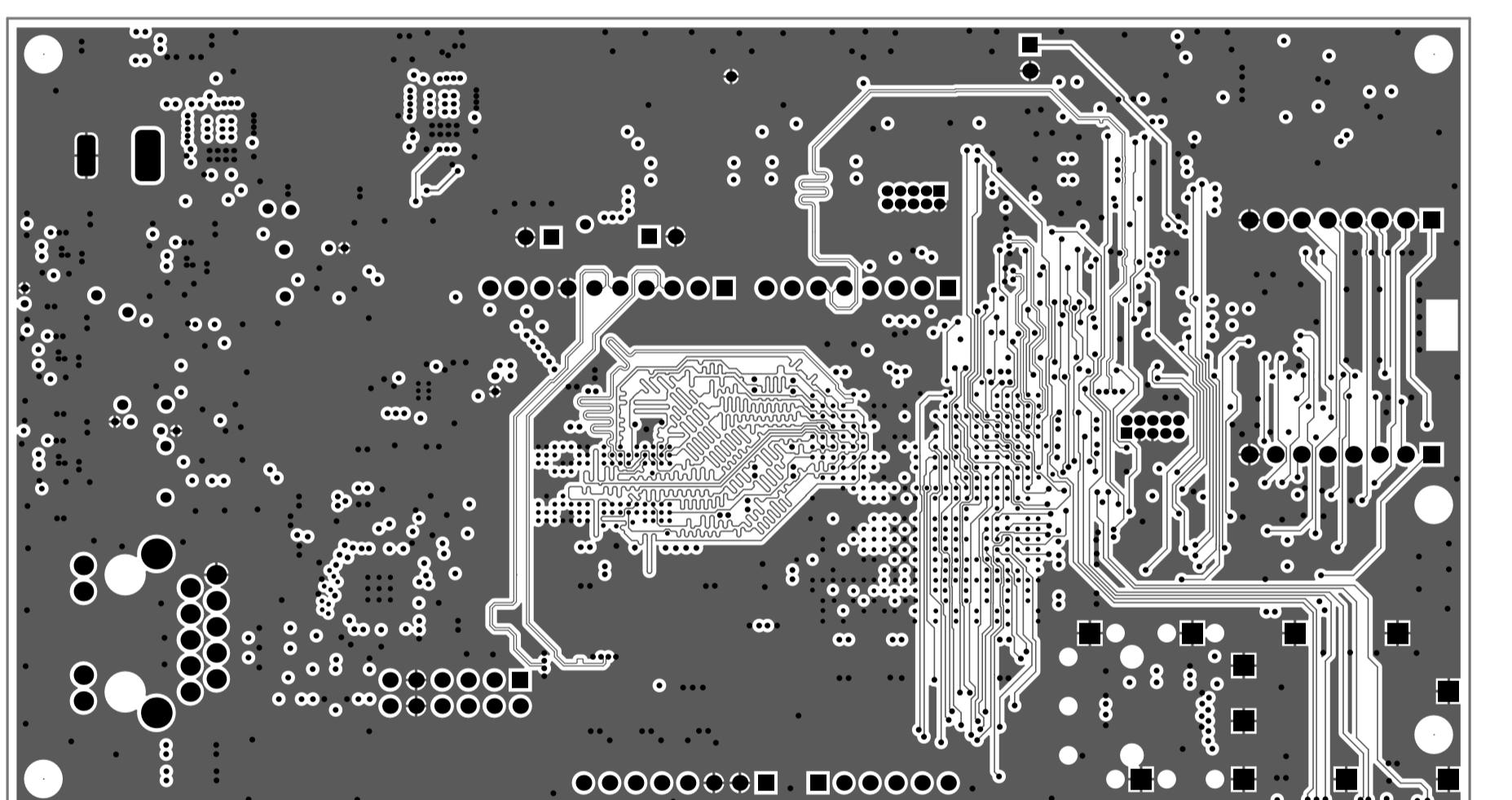
4. PLATING - 0.5oz 0.75oz 1oz Other 5. FINISH - HASL RoHS HASL Immersion Silver Immersion Tin ENIG
Other 6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-810 ON PCB OVER BARE COPPER
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- WHITE BLACK Other 8. IMPEDANCE CONTROL - NO YES SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

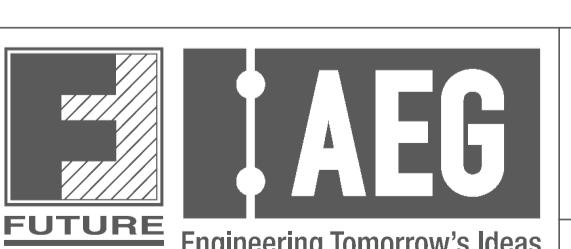
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IN THE DRILL LEGEND14. REGISTRATION - REGISTRATION OF PATTERNS TO BE WITHIN +/- .005 LOCATION OF PATTERN ON BOARD
TO DIMENSION SHOWN

Mid2-Sig_3



Future Electronics – System Design Center NA
237 Hymus Blvd
Pointe-Claire, Quebec, Canada
H9R 5C7

Project #	Microsemi_Avalanche
Title:	Avalanche Polarfire board
Size: B	DWG NO: FEN-412728-PCB-R3
Date:	1/23/2020
Sheet	1 of 1

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Impedance Requirements

Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)	
Top Layer	5mil	5mil	10mil	4mil	10mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Inner Layer	5mil	5.5mil	6mil	4mil	6mil	
Bottom Layer	5mil	5mil	10mil	4mil	10mil	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top_Sig_1	Copper	2.10mil		
4	Dielectric1	FR-4 HTg	3.80mil	4.6	
5	GND_1	Copper	0.70mil		
6	Dielectric 4		7.00mil	4.6	
7	Mid1_Sig_2	Copper	0.70mil		
8	Dielectric2	FR-4 HTg	12.00mil	4.6	
9	Power_1	Copper	1.40mil		
10	Dielectric 5		5.00mil	4.6	
11	Power_2	Copper	1.40mil		
12	Dielectric 7		12.00mil	4.6	
13	Mid2-Sig_3	Copper	0.70mil		
14	Dielectric 8		7.00mil	4.6	
15	GND_2	Copper	0.70mil		
16	Dielectric3	FR-4 HTg	3.80mil	4.6	
17	Bottom_Sig_4	Copper	2.10mil		
18	Bottom Solder	Solder Resist	0.40mil	3.5	
19	Bottom Overlay				

NOTES: < UNLESS OTHERWISE SPECIFIED >

1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET
ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)2. BASE MATERIAL - FR4 High Tg Metal Core Other
- Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL
TO 170°C

3. COPPER FOIL WEIGHT - SEE TABLE FOR STACK-UP DETAIL

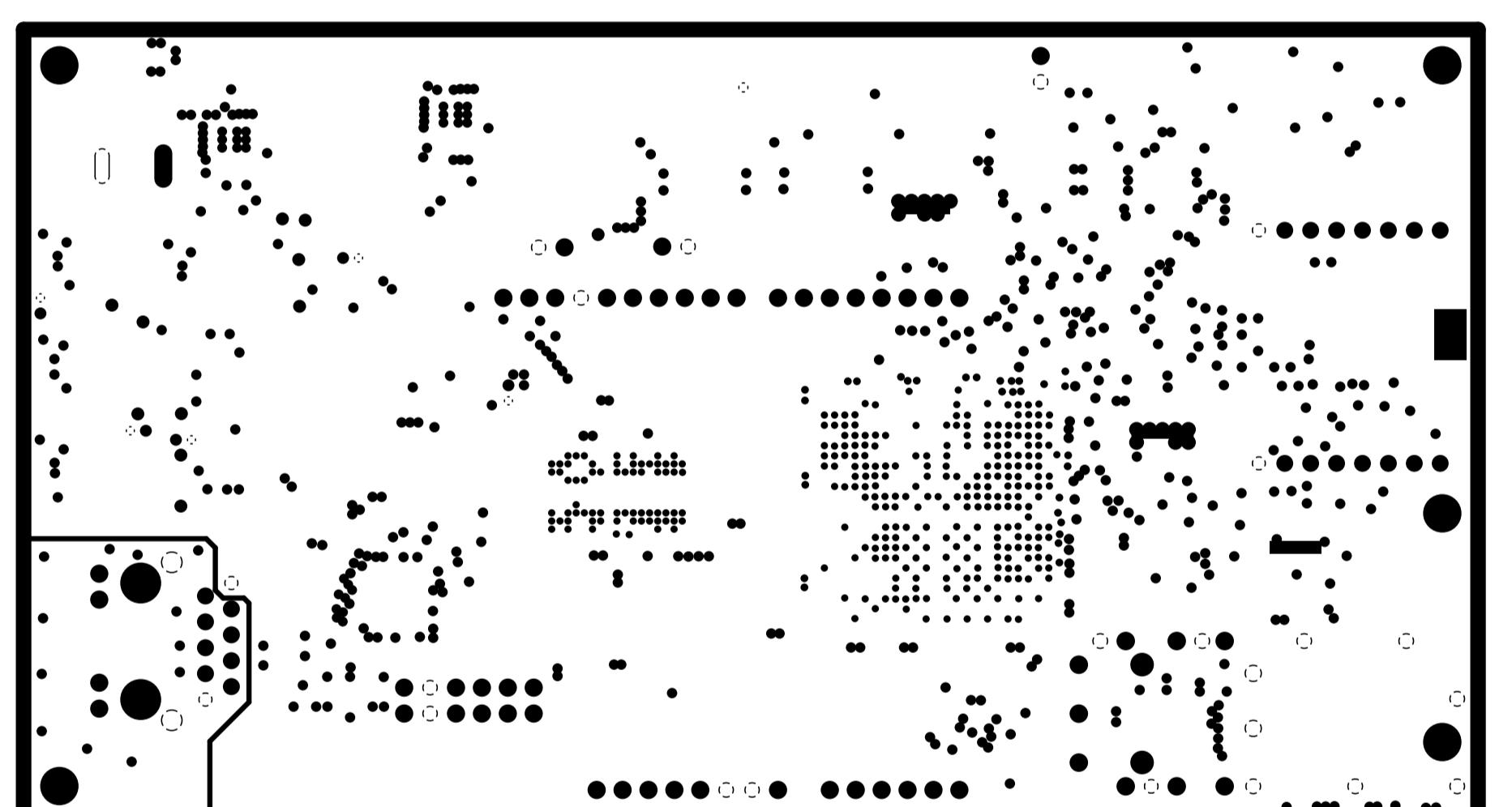
4. PLATING - 0.5oz 0.75oz 1oz Other 5. FINISH - HASL RoHS HASL Immersion Silver Immersion Tin ENIG
Other 6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-810 ON PCB OVER BARE COPPER
- GREEN WHITE BLUE Other 7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
- TOP/BOTTOM TOP ONLY BOTTOM ONLY NONE
- WHITE BLACK Other 8. IMPEDANCE CONTROL - NO YES SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

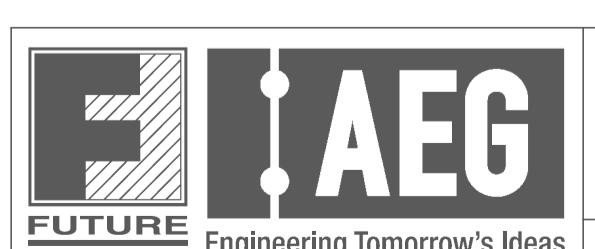
10. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP
- ALL HOLES LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM

11. GERBER FILES - SUPPLIED GERBER FILES MUST NOT BE MODIFIED WITHOUT PRIOR PERMISSION FROM THE CLIENT

12. LOGO - ONLY LOGOS SUPPLIED IN GERBER FILES WILL BE ACCEPTED ON PCB

13. TOOLING HOLES - NO HOLES SHALL BE PERMITTED WITHIN THE BOARD AREA, EXCEPT THOSE INDICATED
IN THE DRILL LEGEND14. REGISTRATION - REGISTRATION OF PATTERNS TO BE WITHIN +/- .005 LOCATION OF PATTERN ON BOARD
TO DIMENSION SHOWN

GND_2



Future Electronics – System Design Center NA
237 Hymus Blvd
Pointe-Claire, Quebec, Canada
H9R 5C7

Project #	Microsemi_Avalanche
Title:	Avalanche Polarfire board
Size: B	DWG NO: FEN-412728-PCB-R3
Date:	1/23/2020
Sheet	1 of 1

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PURPOSE WHATSOEVER OR USED FOR MANUFACTURING
PURPOSES WITHOUT PRIOR WRITTEN PERMISSION
FROM THE FUTURE ELECTRONICS CORPORATION.

Impedance Requirements

Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)	
Top Layer	5mil	5mil	10mil	4mil	10mil	
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14	Dielectric 8		7.00mil	4.6	
15	GND_2	Copper	0.70mil		
16	Dielectric3	FR-4 HTg	3.80mil	4.6	
17	Bottom_Sig_4	Copper	2.10mil		
18	Bottom Solder	Solder Resist	0.40mil	3.5	
19	Bottom Overlay				

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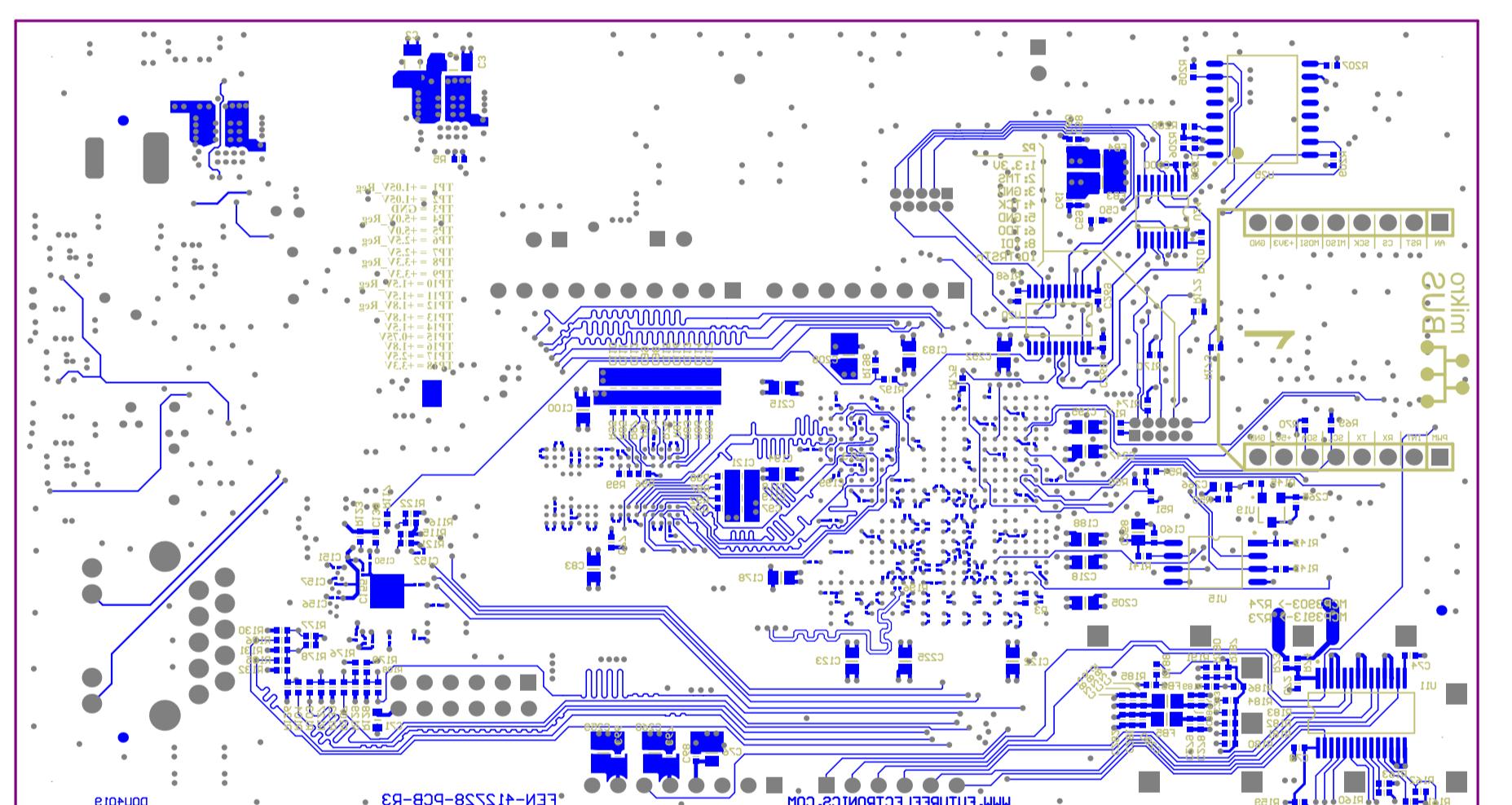
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TO DIMENSION SHOWN

Bottom_Sig_4



Future Electronics – System Design Center NA
237 Hymus Blvd
Pointe-Claire, Quebec, Canada
H9R 5C7

Project #	Microsemi_Avalanche
Title:	Avalanche Polarfire board
Size:	B
DWG NO:	FEN-412728-PCB-R3
REV:	3
Date:	1/23/2020
Sheet	1 of 1

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