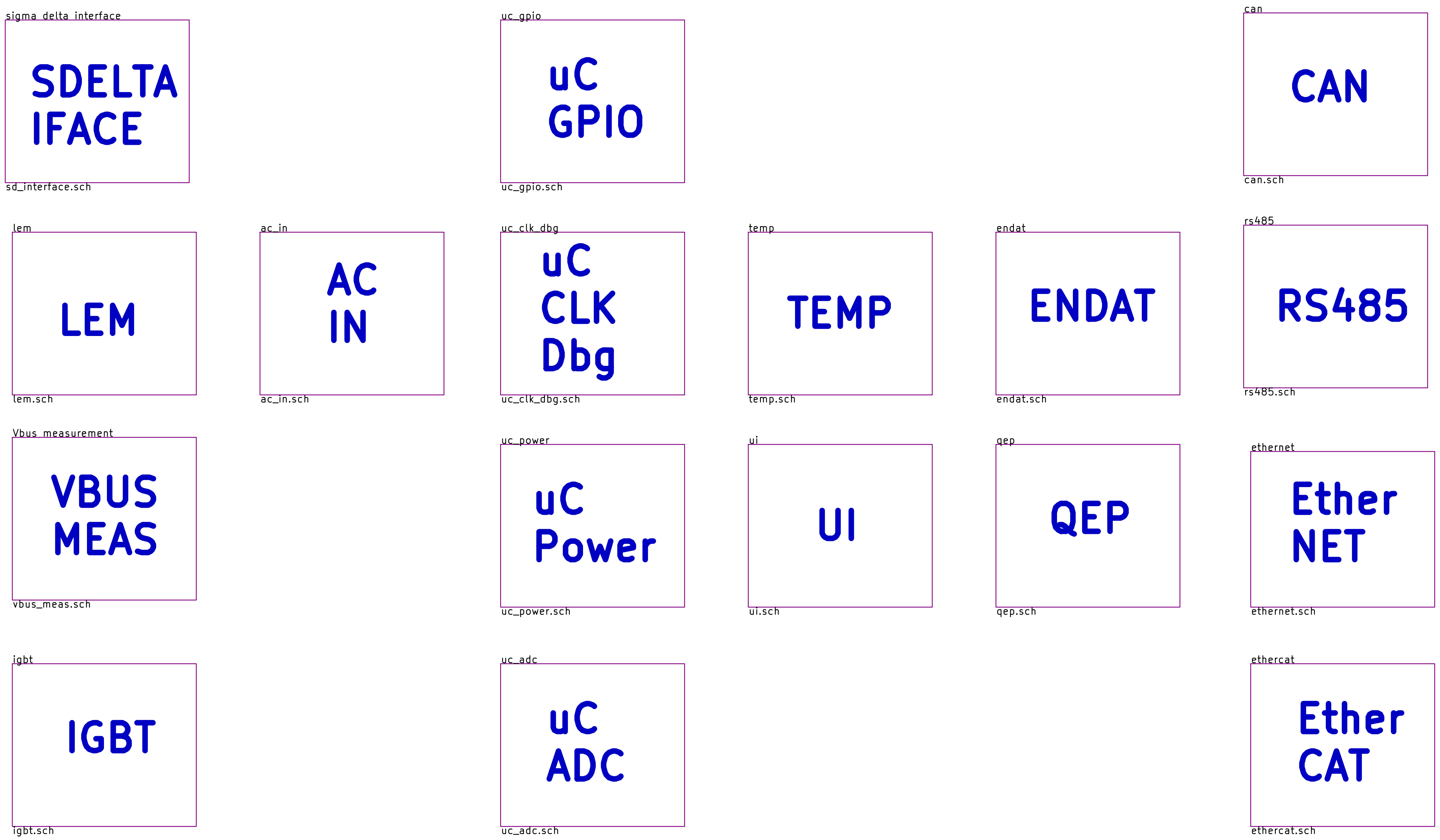
SERVO DRIVER BLOCKS

The project is divided in blocks. Each block join a group os signals and circuits depending on his function. The project is intended to have reinforced insulation using double simple isolation. For that reason, the uC circuitery is on a cold supply and the output logic is at hot supply. BUT take in account that HOT is not 220, is just a name indicating the first isolation stage



Pablo Slavkin
dci

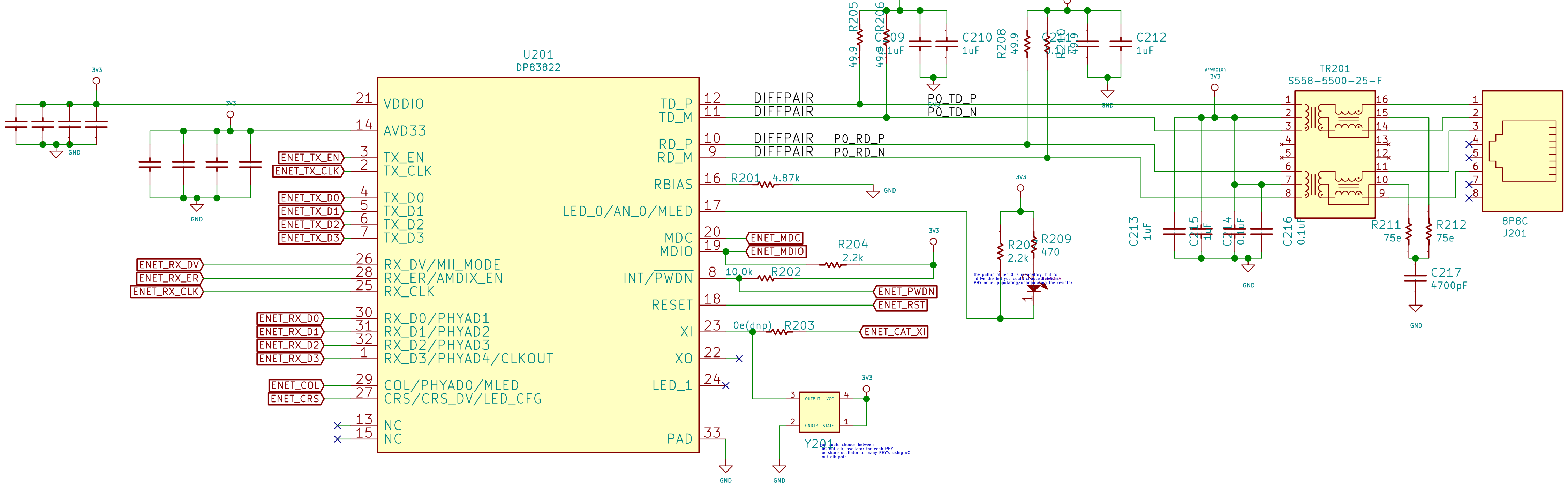
Sheet: /
File: servo.sch

Title: servo drive

Size: A3 | Date: 2020-01-09 | **Rev: 1.0**
KiCad E.D.A. kicad 5.0.2+dfsg1-1 | Id: 1/18

EtherNET

I choose transfeormer spare part instead of the embedded shielded RJ45
plus leds, cause noy I can choose any format connector RJ45 and
maybe add PoE then. And are halt the price



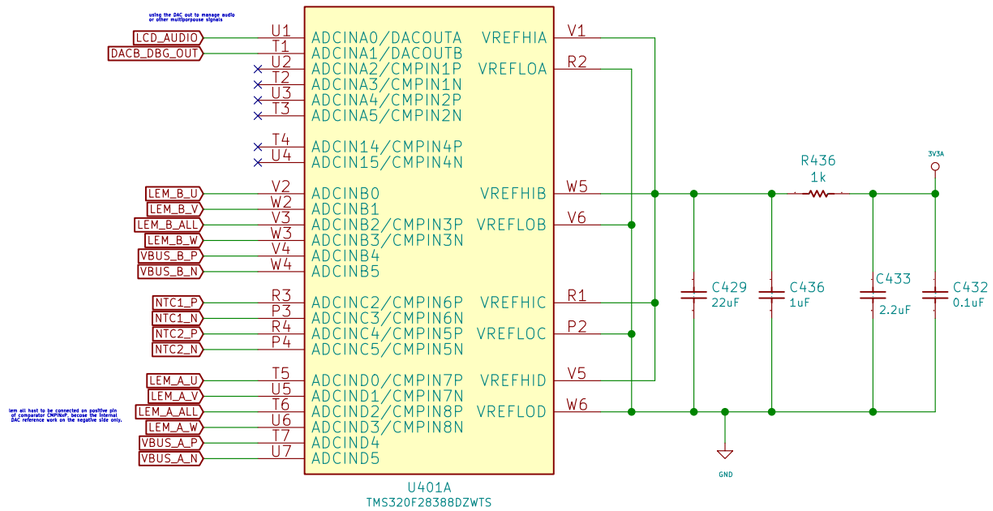
Pablo Slavkin
dci
Sheet: /ethernet/
File: ethernet.sch
Title: ethernet

Size: A3	Date: 2020-01-09	**Rev: 1.0**
KiCad E.D.A. kicad 5.0.2+dfsg1-1		Id: 2/18

uC ADC PINS

Every interface to the ADC has the responsability to filter it's output before enter ADC pin, for that reason these page just connect to the uC without audible to the middle

using the DAC out to manage audio or other multipurpose signals



lem all have to be connected on positive pin of comparator CMPINxP, because the internal DAC reference work on the negative side only.

U401A
TMS320F28388DZWTS

Pablo Slavkin
dci

Sheet: /uc_adc/
File: uc_adc.sch

Title: ADC

Size: A3	Date: 2020-01-09	**Rev: 1.0**
KiCad E.D.A. kicad 5.0.2+dfsg1-1		Id: 3/18

EtherCAT

I choose transformer spare part instead of the embedded stlyded RJ45 plus 1ms, cause say I can choose any format connector RJ45 and maybe add Pol Stek. And we hold the price

The eeprom is mandatory in order to ESC read save some internal configuration.

Leds are optional, but the PHY's has som pins used as a bootstrap, so you have to respect that

EtherCAT P0

U402
DP83822

VDDIO
AVD33
TX_EN
TX_CLK
TX_D0
TX_D1
TX_D2
TX_D3
RX_DV/MII_MODE
RX_ER/AMDIX_EN
RX_CLK
RX_D0/PHYAD1
RX_D1/PHYAD2
RX_D2/PHYAD3
RX_D3/PHYAD4/CLKOUT
COL/PHYAD0/MLED
CRS/CRS_DV/LED_CFG
NC
NC
TD_P
TD_M
RD_P
RD_M
RBIAS
LED_0/AN_0/MLED
MDC
MDIO
INT/PWDN
RESET
XI
XO
LED_1
PAD

ECAT0_TX_EN
ECAT0_TX_CLK
ECAT0_TX_D0
ECAT0_TX_D1
ECAT0_TX_D2
ECAT0_TX_D3
ECAT0_RX_DV
ECAT0_RX_ER
ECAT0_RX_CLK
ECAT0_RX_D0
ECAT0_RX_D1
ECAT0_RX_D2
ECAT0_RX_D3

R619 2.2k
R620 2.2k
R624 4.87k
R625 10.0k
R629 2.2k
R409 0e(dnp)
ECAT_MDC
ECAT_MDIO
ECAT_RST
ENET_CAT_XI

Address select. Be shure you select two distinct

Y401
You should choose between 50M o.s. oscilator for work PHY or share oscilator to many PHY's using uC out clk path

P0_TD_P
P0_TD_N
P0_RD_P
P0_RD_N

R631 49.9
R632 49.9
R635 49.9
R636 49.9
C619 0.1uF
C621 1uF
C624 0.1uF
C625 1uF

TR401
S558-5500-25-F
J401
8P8C

R639 2.2k
R421 470
R422 470
R417 2.2k
ECAT0_RJ_LED0
ECAT0_RJ_LED1

The pullup of led_0 is mandatory, but to shure the phy you could choose between PHY or uC pooltating/unpooltating the resistor

C629 1uF
C628 0.1uF
C630 0.1uF
R425 75e
R426 75e
C417 4700pF

EtherCAT P1

U403
DP83822

VDDIO
AVD33
TX_EN
TX_CLK
TX_D0
TX_D1
TX_D2
TX_D3
RX_DV/MII_MODE
RX_ER/AMDIX_EN
RX_CLK
RX_D0/PHYAD1
RX_D1/PHYAD2
RX_D2/PHYAD3
RX_D3/PHYAD4/CLKOUT
COL/PHYAD0/MLED
CRS/CRS_DV/LED_CFG
NC
NC
TD_P
TD_M
RD_P
RD_M
RBIAS
LED_0/AN_0/MLED
MDC
MDIO
INT/PWDN
RESET
XI
XO
LED_1
PAD

ECAT1_TX_EN
ECAT1_TX_CLK
ECAT1_TX_D0
ECAT1_TX_D1
ECAT1_TX_D2
ECAT1_TX_D3
ECAT1_RX_DV
ECAT1_RX_ER
ECAT1_RX_CLK
ECAT1_RX_D0
ECAT1_RX_D1
ECAT1_RX_D2
ECAT1_RX_D3

R407 2.2k
R408 2.2k
R410 4.87k
R411 10.0k
R413 2.2k
R412 0e(dnp)
ECAT_MDC
ECAT_MDIO
ECAT_RST
ENET_CAT_XI

Address select. Be shure you select two distinct

Y402
You should choose between 50M o.s. oscilator for work PHY or share oscilator to many PHY's using uC out clk path

P1_TD_P
P1_TD_N
P1_RD_P
P1_RD_N

R414 49.9
R415 49.9
R418 49.9
R419 49.9
C409 0.1uF
C410 1uF
C411 0.1uF
C412 1uF

TR402
S558-5500-25-F
J402
8P8C

R416 2.2k
R422 470
R423 470
R419 2.2k
ECAT1_RJ_LED1
ECAT1_RJ_LED0

C415 1uF
C414 0.1uF
C416 0.1uF
R427 75e
R428 75e
C418 4700pF

EtherCAT EEPROM

these IC is a must, Especified on the ethercat slave

U601
EEPROM_8P_1-3NC

NC
NC
NC
VSS
VCC
WP
SCL
SDA

R603 4.7k
R604 4.7k
C602 0.1uF
ECAT_EEPROM_SCL
ECAT_EEPROM_SDA

Run and Error LEDs

There are totaly optional

D601
Red@2mA
R605 330
ECAT_LED0

D602
green@2mA
R606 330
ECAT_LED1

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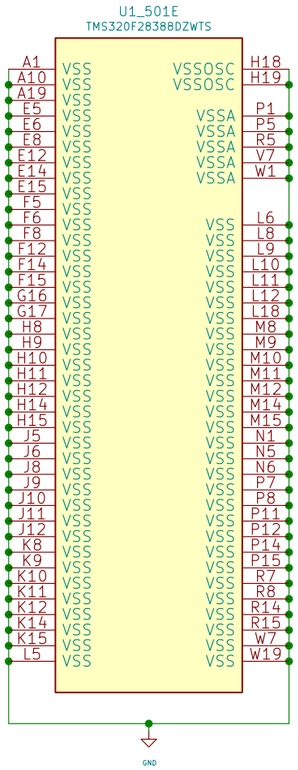
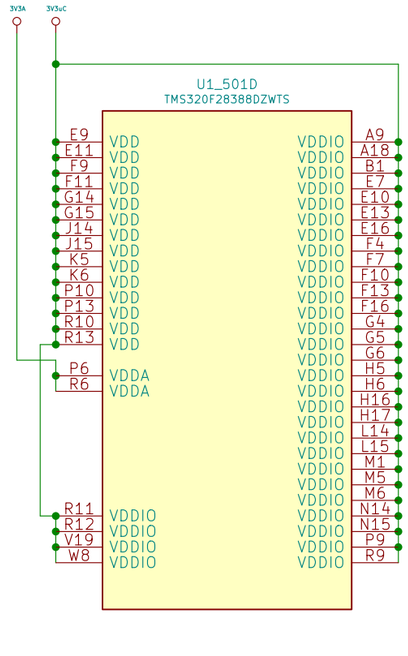
Sheet: /ethercat/
File: ethercat.sch

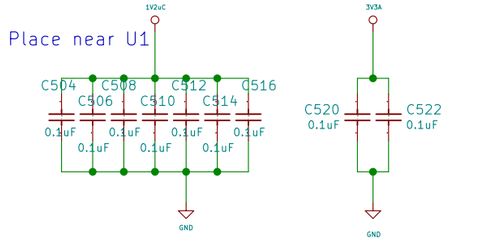
Title: ethercat

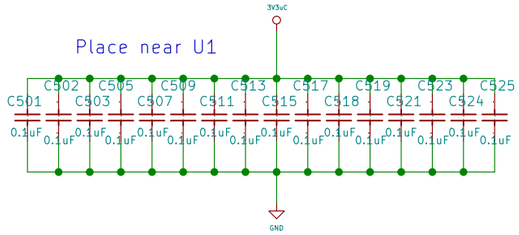
Size: A3	Date: 2020-01-09	**Rev: 1.0**
KiCad E.D.A. kicad 5.0.2+dfsg1-1		Id: 4/18

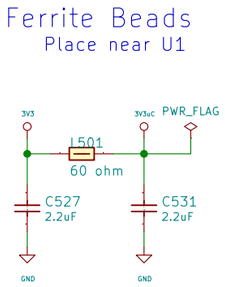
DECOUPLING FILTERS











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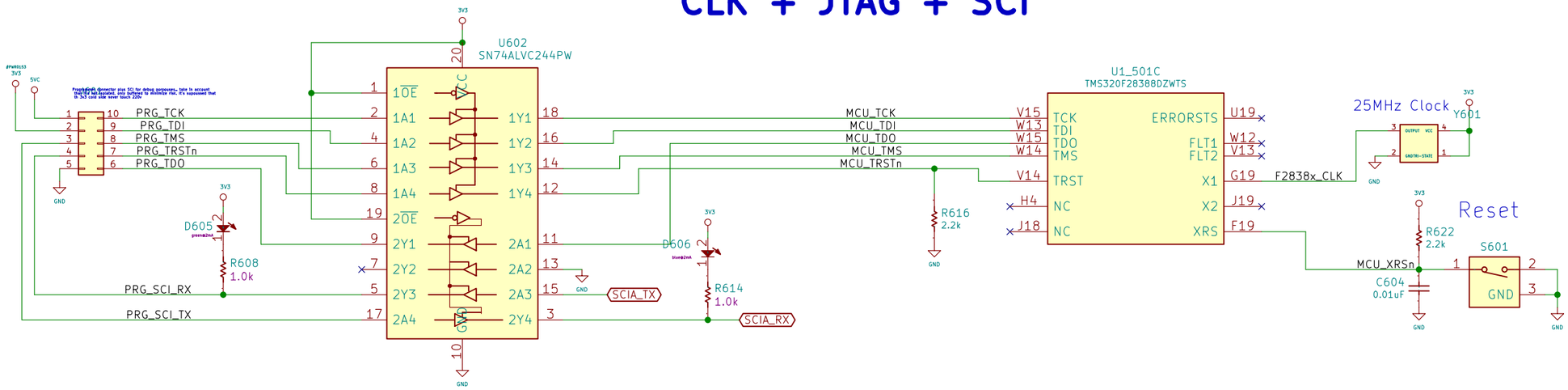
Sheet: /uc_power/
File: uc_power.sch

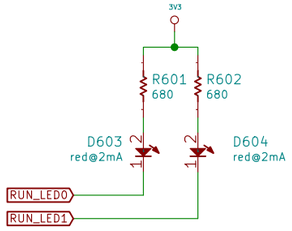
Title: uC Power

Size: A3	Date: 2020-01-09	**Rev: 1.0**
KiCad E.D.A. kicad 5.0.2+dfsg1-1		Id: 5/18

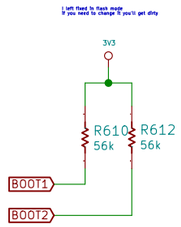
CLK + JTAG + SCI



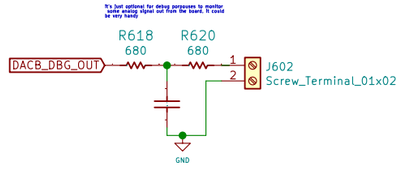
MULTI PORPOUSE LEDS



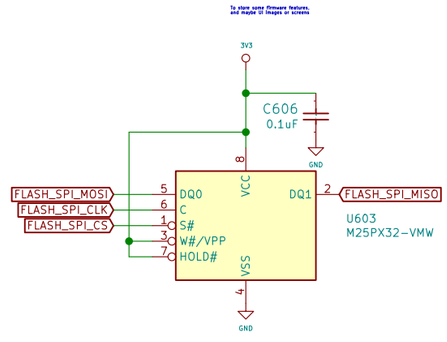
BOOTSRAP R's



DAC DBG OUT



SPI FLASH



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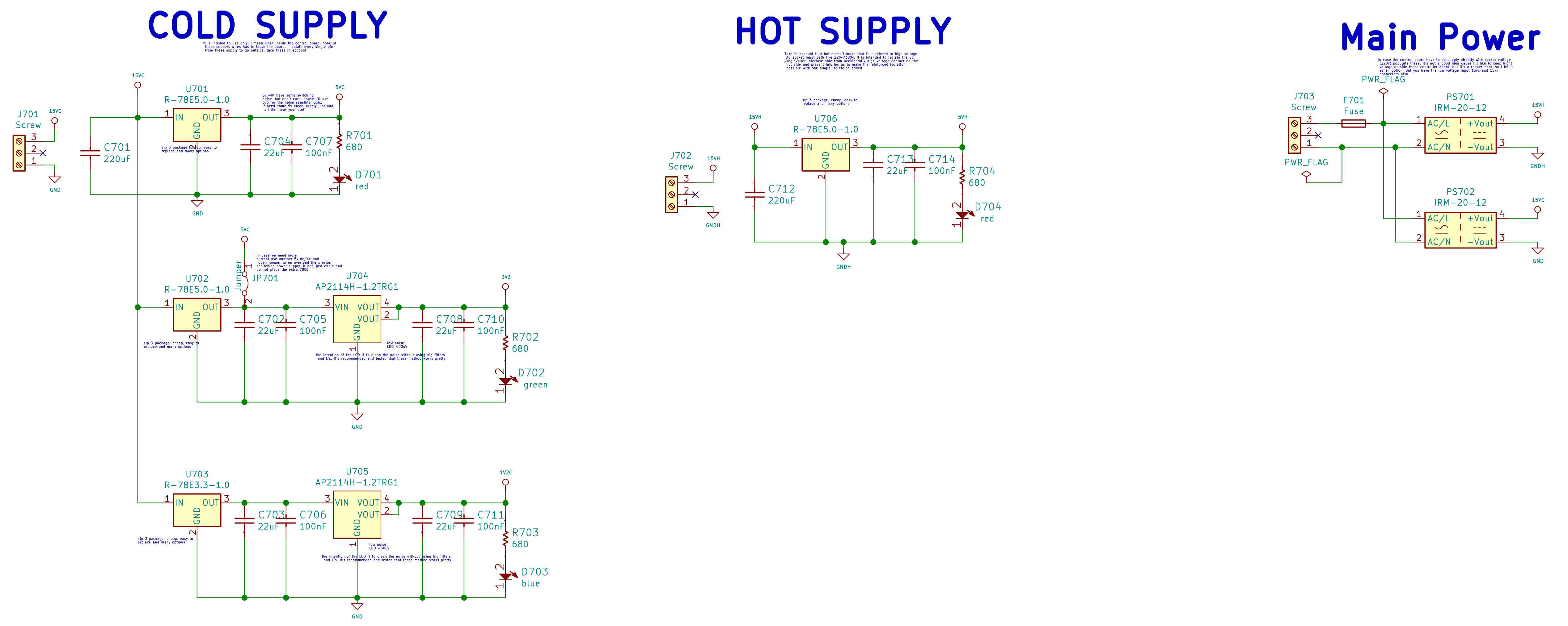
dci

Sheet: /uc_clk_dbg/		
File: uc_clk_dbg.sch		
Title: clk		
Size: A3	Date: 2020-01-09	**Rev: 1.0**
KiCad E.D.A. kicad 5.0.2+dfsg1-1		Id: 6/18



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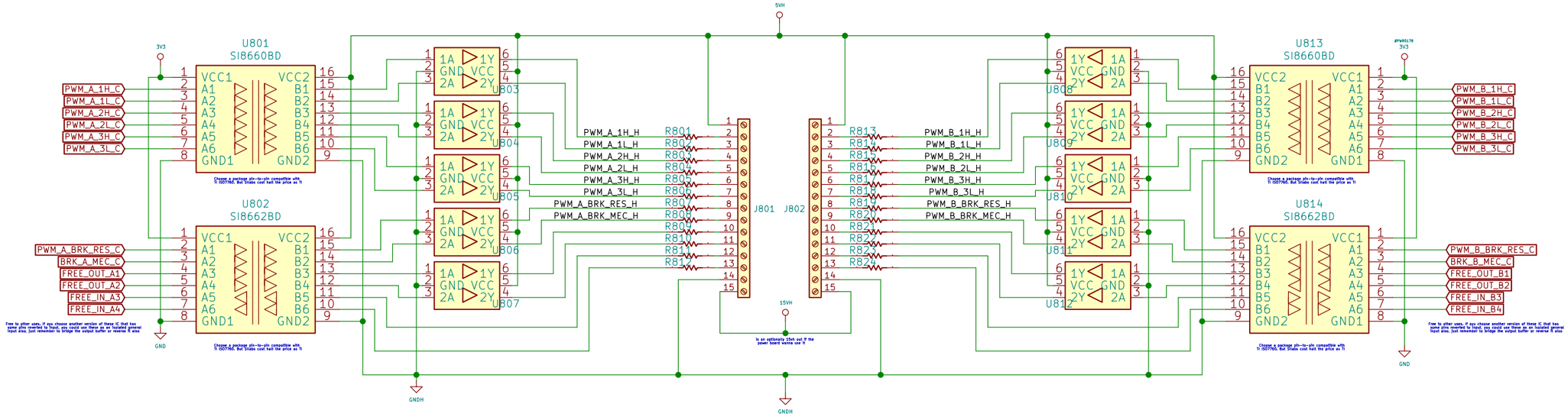
Sheet: /ac_in/
File: ac_in.sch

Title: AC input

Size: A3	Date: 2020-01-09	Rev: 1.0
KiCad E.D.A. kicad 5.0.2+dfsg1-1		Id: 7/18

PWM OUT -> ISOLATOR -> BUFFER -> LED

these pins has isolation and a buffer. They could be directly connected to a IGBT module for test porpouses or to a power board and another isolation stage for production porpouses to have a reinforced isolation. In next stages of the development of the board, the buffers could be eliminated, but not the isolation Scmith trigger stage



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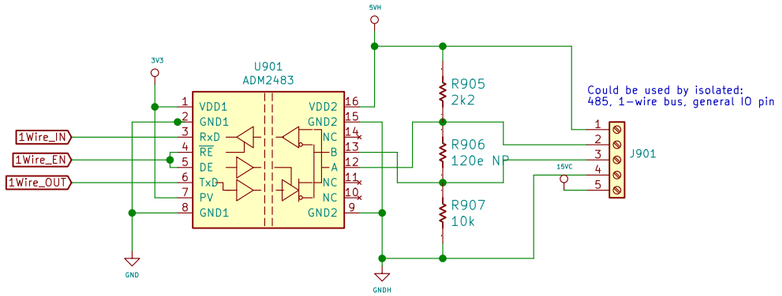
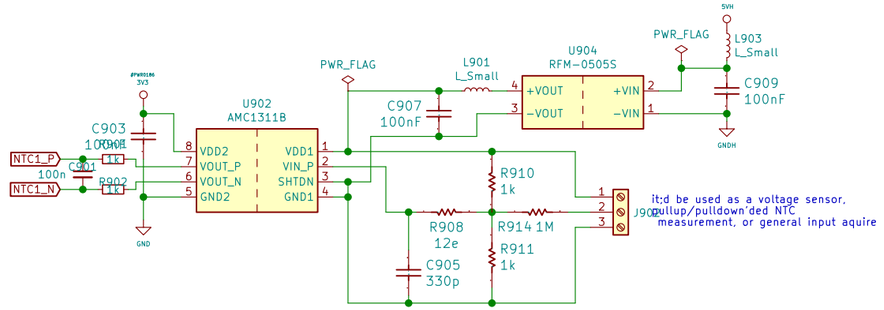
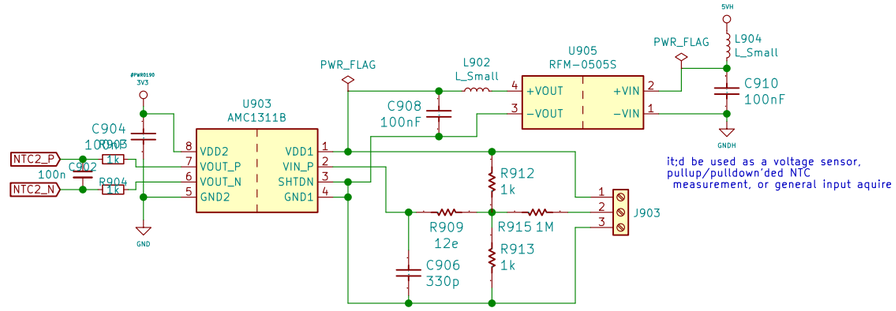
dci

Sheet: /igbt/		
File: igbt.sch		
Title: Igbt interface		
Size: A3	Date: 2020-01-09	**Rev: 1.0**
KiCad E.D.A. kicad 5.0.2+dfsg1-1		Id: 8/18

2 isolated NTC interfase +
1 isolated 1-wire/485

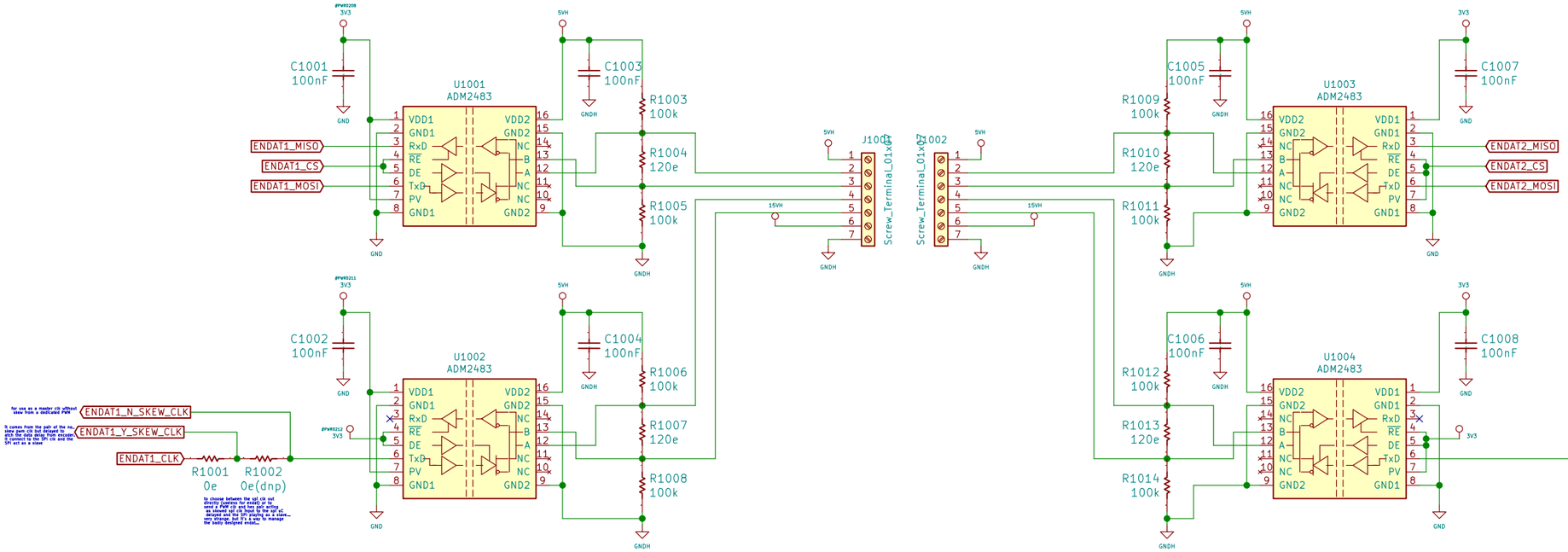






Pablo Slavkin		
dci		
Sheet: /temp/		
File: temp.sch		
Title: gpio		
Size: B	Date: 2020-01-09	**Rev: 1.0**
KiCad E.D.A. kicad 5.0.2+dfsg1-1		Id: 9/18

2X Isolated ENDAT interface



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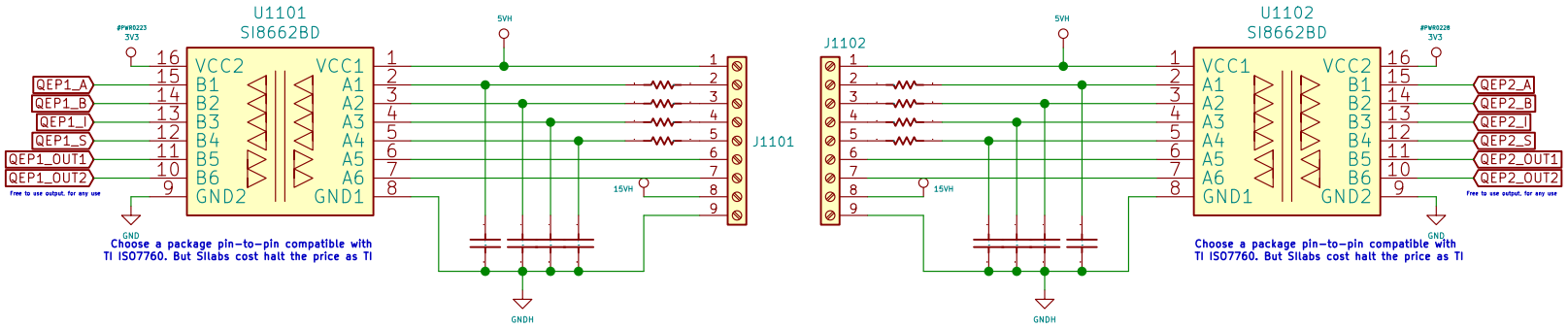
dci

Sheet: /endat/
File: endat.sch

Title: ENDAT/BISS Interface

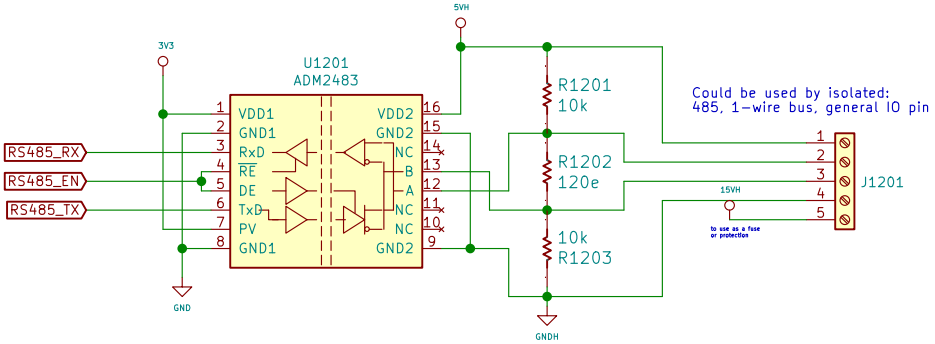
Size: A3	Date: 2020-01-09	**Rev: 1.0**
KiCad E.D.A. kicad 5.0.2+dfsg1-1		Id: 10/18

2x Isolated Incremental encoder
5v input A-B-I-S



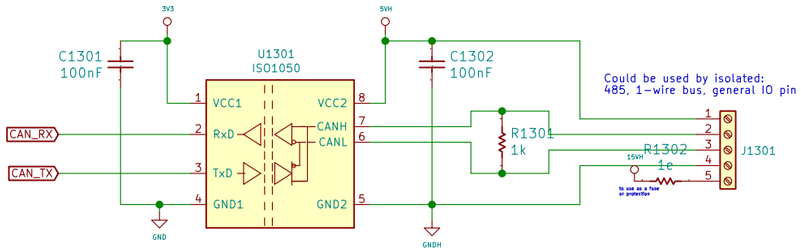
Pablo Slavkin		
dci		
Sheet: /qep/		
File: qep.sch		
Title: QEP encoder Interfase		
Size: A4	Date: 2020-01-09	**Rev: 1.0**
KiCad E.D.A. kicad 5.0.2+dfsg1-1		Id: 11/18

Isolated RS485



Pablo Slavkin **dci**		
Sheet: /rs485/ File: rs485.sch		
Title: RS485		
Size: A4	Date: 2020-01-09	**Rev: 1.0**
KiCad E.D.A. kicad 5.0.2+dfsg1-1		Id: 12/18

Isolated CAN interfase



Pablo Slavkin
dci

Sheet: /can/		
File: can.sch		
Title:		
Size: A3	Date: 2020-01-09	**Rev: 1.0**
KiCad E.D.A. kicad 5.0.2+dfsg1-1		Id: 13/18

uC GPIO's pins

I've spend hours to choose the GPIO's for each interface trying to not clash one to the other, just pay attention if you wanna move some pheres.
I've used global labels connector to go from one page to another because the off-page connector because it's more prone to errors. I know that's not too orthodox, but it's better and fastly for now

U1_501B
TMS320F28388DZWTS

PWM_A_1H_C	C8	GPIO0/EPWM1A	
PWM_A_1L_C	D8	GPIO1/EPWM1A	
PWM_A_2H_C	A7	GPIO2/EPWM2A	
PWM_A_2L_C	B7	GPIO3/EPWM2B	
PWM_A_3H_C	C7	GPIO4/EPWM3A	
PWM_A_3L_C	D7	GPIO5/EPWM3B	
PWM_B_1H_C	A6	GPIO6/EPWM4A	
PWM_B_1L_C	B6	GPIO7/EPWM4B	
PWM_B_2H_C	G2	GPIO8/EPWM5A	
PWM_B_2L_C	G3	GPIO9/EPWM5B	
PWM_B_3H_C	B2	GPIO10/EPWM6A	
PWM_B_3L_C	C1	GPIO11/EPWM6B	
PWM_A_BRK_RES_C	C2	GPIO12/EPWM7A	
PWM_B_BRK_RES_C	D1	GPIO13/EPWM7B	
ENDAT1_N_SKEW_CLK	D2	GPIO14/EPWM8A	
ENDAT1_Y_SKEW_CLK	D3	GPIO15/EPWM8B	
use PWM channel for sh if SD	E1	GPIO16/EPWM9A	
SD_A_CLK1	E2	GPIO17/SD1_C1	
ENDAT2_N_SKEW_CLK	E3	GPIO18/EPWM10A	
ENDAT2_Y_SKEW_CLK	E4	GPIO19/EPWM10B	
QEP1_A	F2	GPIO20/EQEP1_A	
QEP1_B	F3	GPIO21/EQEP1_B	
QEP1_S	J4	GPIO22/EQEP1_STROBE	
QEP1_I	K4	GPIO23/EQEP1_INDEX	
QEP2_A	K3	GPIO24/EQEP2_A	
QEP2_B	K2	GPIO25/EQEP2_B	
QEP2_I	K1	GPIO26/EQEP2_INDEX	
QEP2_S	L1	GPIO27/EQEP2_STROBE	
SCIA_RX	V11	GPIO28/SCIA_RX	
SCIA_TX	W11	GPIO29/SCIA_TX	
CAN_RX	T11	GPIO30/CANA_RX	
CAN_TX	U11	GPIO31/CANA_TX	
BRK_A_MEC_C	U13	GPIO32	
BRK_B_MEC_C	T13	GPIO33	
RUN_LED0	U14	GPIO34	
RUN_LED1	T14	GPIO35	
SD_A1_D	V16	GPIO36/SD1_D1	
SD_A2_D	U16	GPIO37/SD1_D2	
SD_A3_D	T16	GPIO38/SD1_D3	
SD_A4_D	W17	GPIO39/SD1_D4	
FREE_OUT_A1	V17	GPIO40	
FREE_OUT_A2	U17	GPIO41	
FREE_IN_A3	D19	GPIO42	
FREE_IN_A4	C19	GPIO43	
FREE_OUT_B1	K18	GPIO44	
FREE_OUT_B2	K19	GPIO45	
FREE_IN_B3	E19	GPIO46	
FREE_IN_B4	E18	GPIO47	
	R16	GPIO48	
SD_B1_D	R17	GPIO49/SD2_D1	
SD_B2_D	R18	GPIO50/SD2_D2	
SD_B3_D	R19	GPIO51/SD2_D3	
SD_B4_D	P16	GPIO52/SD2_D4	
RS485_EN	P17	GPIO53	
RS485_TX	P18	GPIO54/SCIB_TX	
RS485_RX	P19	GPIO55/SCIB_RX	
	N16	GPIO56	
SD_B_CLK1	N18	GPIO57/SD2_C1	
ENDAT1_MOSI	N17	GPIO58/SPIA_SIMO	
ENDAT1_MISO	M16	GPIO59/SPIA_SOMI	
ENDAT1_CLK	M17	GPIO60/SPIA_CLK	
ENDAT1_CS	L16	GPIO61/SPIA_STEn	
	J17	GPIO62	
ENDAT2_MOSI	J16	GPIO63/SPIB_SIMO	
ENDAT2_MISO	L17	GPIO64/SPIB_SOMI	
ENDAT2_CLK	K16	GPIO65/SPIB_CLK	
ENDAT2_CS	K17	GPIO66/SPIB_STEn	
	B19	GPIO67	
	C18	GPIO68	
	B18	GPIO69	
	A17	GPIO70	
	B17	GPIO71	
BOOT1	B16	GPIO72	
	A16	GPIO73	
	C17	GPIO74	
	D16	GPIO75	
	C16	GPIO76	
QEP2_OUT1	A15	GPIO77	
QEP2_OUT2	B15	GPIO78	
QEP1_OUT1	C15	GPIO79	
QEP1_OUT2	D15	GPIO80	
1Wire_IN	A14	GPIO81	
1Wire_EN	B14	GPIO82	
1Wire_OUT	C14	GPIO83	
	A11	GPIO84	BOOT2
	B11	GPIO85	LCD_GPIO3
	C11	GPIO86	LCD_GPIO2
	D11	GPIO87	LCD_GPIO1
	C6	GPIO88	LCD_GPIO0
	D6	GPIO89	LCD_SPI_PDW
	A5	GPIO90	LCD_INT
	B5	GPIO91/SPID_SIMO	LCD_SPI_MOSI
	A4	GPIO92/SPID_SOMI	LCD_SPI_MISO
	B4	GPIO93/SPID_CLK	LCD_SPI_CLK
	A3	GPIO94/SPID_STEn	LCD_SPI_CS
	B3	GPIO95	
	C3	GPIO96	
	A2	GPIO97	
	F1	GPIO98	
	G1	GPIO99	
	H1	GPIO100/SPIC_SIMO	FLASH_SPI_MOSI
	H2	GPIO101/SPIC_SOMI	FLASH_SPI_MISO
	H3	GPIO102/SPIC_CLK	FLASH_SPI_CLK
	J1	GPIO103/SPIC_STEn	FLASH_SPI_CS
	J2	GPIO104	
	J3	GPIO105	ENET_MDC
	L2	GPIO106	ENET_MDIO
	L3	GPIO107	
	L4	GPIO108	
	N2	GPIO109	ENET_PWDN
	M2	GPIO110	ENET_CRS
	M4	GPIO111	ENET_COL
	M3	GPIO112	ENET_RX_CLK
	N4	GPIO113	ENET_RX_DV
	N3	GPIO114	ENET_RX_ER
	V12	GPIO115	ENET_RX_D0
	W10	GPIO116	ENET_RX_D1
	U12	GPIO117	ENET_RX_D2
	T12	GPIO118	ENET_RX_D3
	T15	GPIO119	ENET_TX_EN
	U15	GPIO120	ENET_RST
	W16	GPIO121	ENET_TX_CLK
	T8	GPIO122	ENET_TX_D0
	U8	GPIO123	ENET_TX_D1
	V8	GPIO124	ENET_TX_D2
	T9	GPIO125	ENET_TX_D3
	U9	GPIO126	
	V9	GPIO127	
	W9	GPIO128	
	T10	GPIO129	ECAT1_TX_EN
	U10	GPIO130	ECAT1_TX_CLK
	V10	GPIO131	ECAT1_TX_D0
	W18	GPIO132	ECAT1_TX_D1
	G18	GPIO133	
	V18	GPIO134	ECAT1_TX_D2
	U18	GPIO135	ECAT1_TX_D3
	T17	GPIO136	ECAT1_RX_DV
	T18	GPIO137	ECAT1_RX_CLK
	T19	GPIO138	ECAT1_RX_ER
	N19	GPIO139	ECAT1_RX_D0
	M19	GPIO140	ECAT1_RX_D1
	M18	GPIO141	ECAT1_RX_D2
	L19	GPIO142	ECAT1_RX_D3
	F18	GPIO143	ECAT0_RJ_LED0
	F17	GPIO144	ECAT1_RJ_LED0
	E17	GPIO145	ECAT_LED0
	D18	GPIO146	ECAT_LED1
	D17	GPIO147	
	D14	GPIO148	ECAT0_RJ_LED1
	A13	GPIO149	ECAT1_RJ_LED1
	B13	GPIO150/ESC_I2C_SDA	ECAT_EEPROM_SDA
	C13	GPIO151/ESC_I2C_SCL	ECAT_EEPROM_SCL
	D13	GPIO152/ESC_MDIO_CLK	ECAT_MDC
	A12	GPIO153/ESC_MDIO_DATA	ECAT_MDIO
	B12	GPIO154/ESC_PHY_CLK	ENET_CAT_XI
	C12	GPIO155/ESC_PHY_RESETn	ECAT_RST
	D12	GPIO156/ESC_TX0_ENA	ECAT0_TX_EN
	B10	GPIO157/ESC_TX0_CLK	ECAT0_TX_CLK
	C10	GPIO158/ESC_TX0_DATA0	ECAT0_TX_D0
	D10	GPIO159/ESC_TX0_DATA1	ECAT0_TX_D1
	B9	GPIO160/ESC_TX0_DATA2	ECAT0_TX_D2
	C9	GPIO161/ESC_TX0_DATA3	ECAT0_TX_D3
	D9	GPIO162/ESC_RX0_DV	ECAT0_RX_DV
	A8	GPIO163/ESC_RX0_CLK	ECAT0_RX_CLK
	B8	GPIO164/ESC_RX0_ERR	ECAT0_RX_ER
	C5	GPIO165/ESC_RX0_DATA0	ECAT0_RX_D0
	D5	GPIO166/ESC_RX0_DATA1	ECAT0_RX_D1
	C4	GPIO167/ESC_RX0_DATA2	ECAT0_RX_D2
	D4	GPIO168/ESC_RX0_DATA3	ECAT0_RX_D3

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Sheet: /uc_gpio/
File: uc_gpio.sch

Title: gpio

Size: A3	Date: 2020-01-09	**Rev: 1.0**
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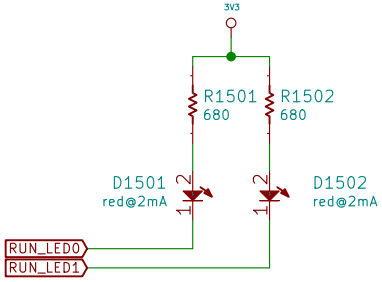
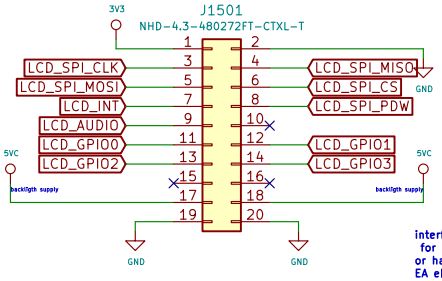
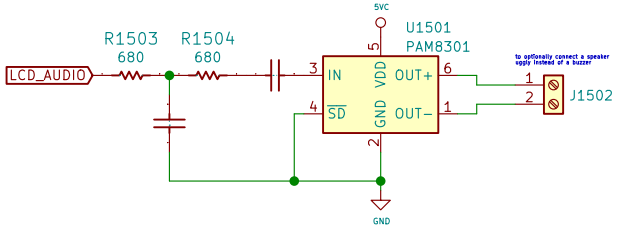
Multipropouse LEDs



LCD UI interfase





interfase directly using f20 wires flat cable
for NHD-4.3-480272FT-CTXL-T newheaven LCD
or hand wiring
EA eDIP128B-6LWTP

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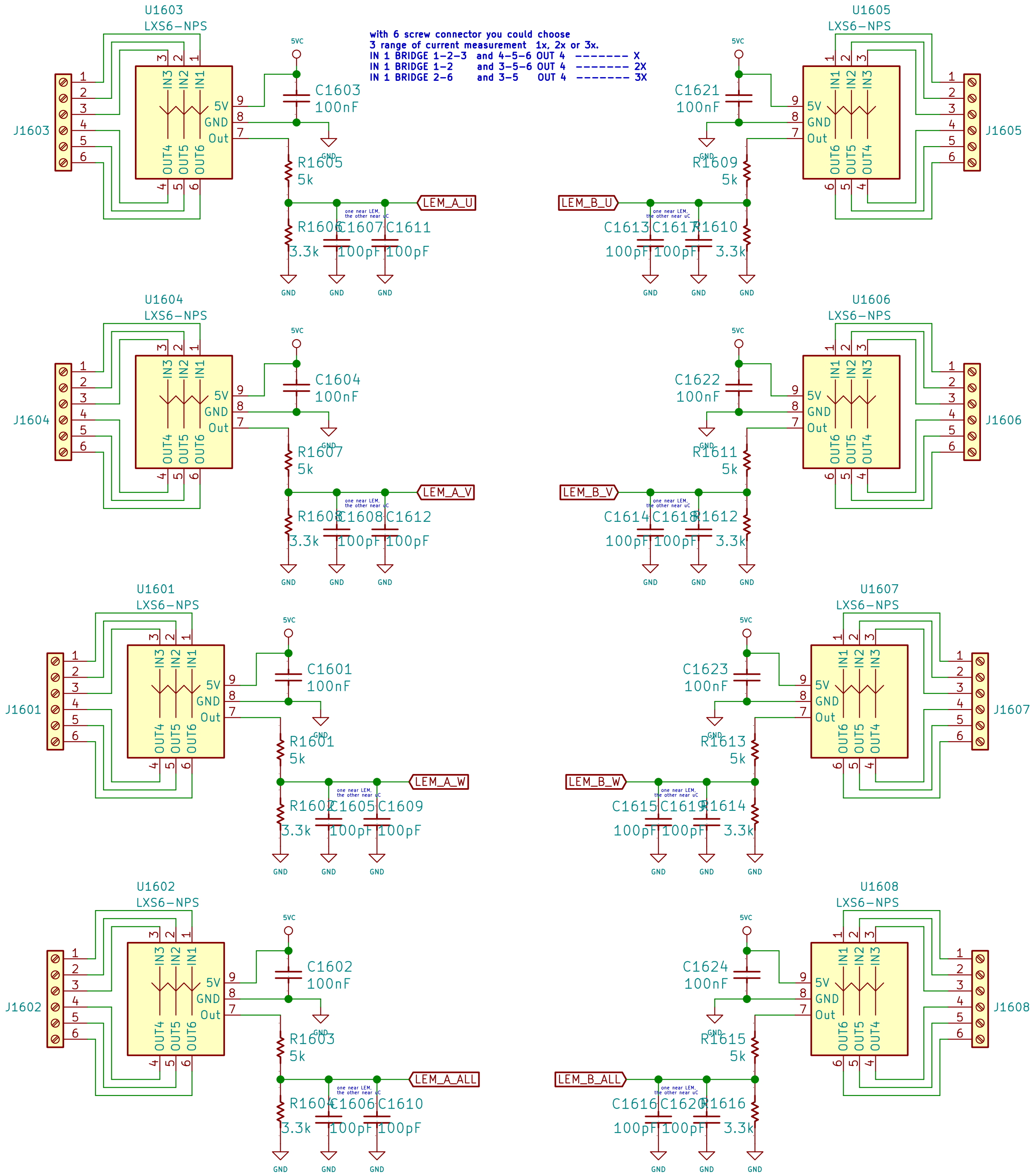
Sheet: /ui/ File: ui.sch		
Title: clk		
Size: A4	Date: 2020-01-09	**Rev: 1.0**
KiCad E.D.A. kicad 5.0.2+dfsg1-1		Id: 15/18

8 LEM's current measurement
U+V+W+ALL x 2

The intention of these lems is to have the capacity on the control board to measure all the current, without the need of the sigma delta chips on power board side. Why?? becouse I've study the two options carrefullty and I've conclude that there are very similar, and more or less buck per byck (a little expensive is SD) but the new generation LEM's I'm includin here has <0.5uSeg response time, and the SD has all the SD filter delay, so LEM is faster. The other advantage is that for same LEM I've choosen you could rearange the connection to multiply the preccision 1x,2x or 3x without touching nothing, and is pretty linear. In the case of SD you have to change the precission shunt. or puts more than one, that is costly and take some board space.
The disadvantage of LEM is that the output is single ended, so it could not travel across boards, for that reason I've put them on control board, but is completely isolated becouse of these phisics effect. and also becouse of that single ended I just use one ADC channel per current. I't not the only option, becous if you insist and wanna use SD, I'eft all the SD channels available as an inputs on SD schematic page.

these LEM's version doesn't need a buffer,
it's one already included inside LEM

LXS6 is LTS and CAS pin to pin compatible, but LXS is a little better.
I don't usa an opamp becous with the external conection I have x,2x and 3x amplifier option without any component



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Sheet: /lem/
File: lem.sch

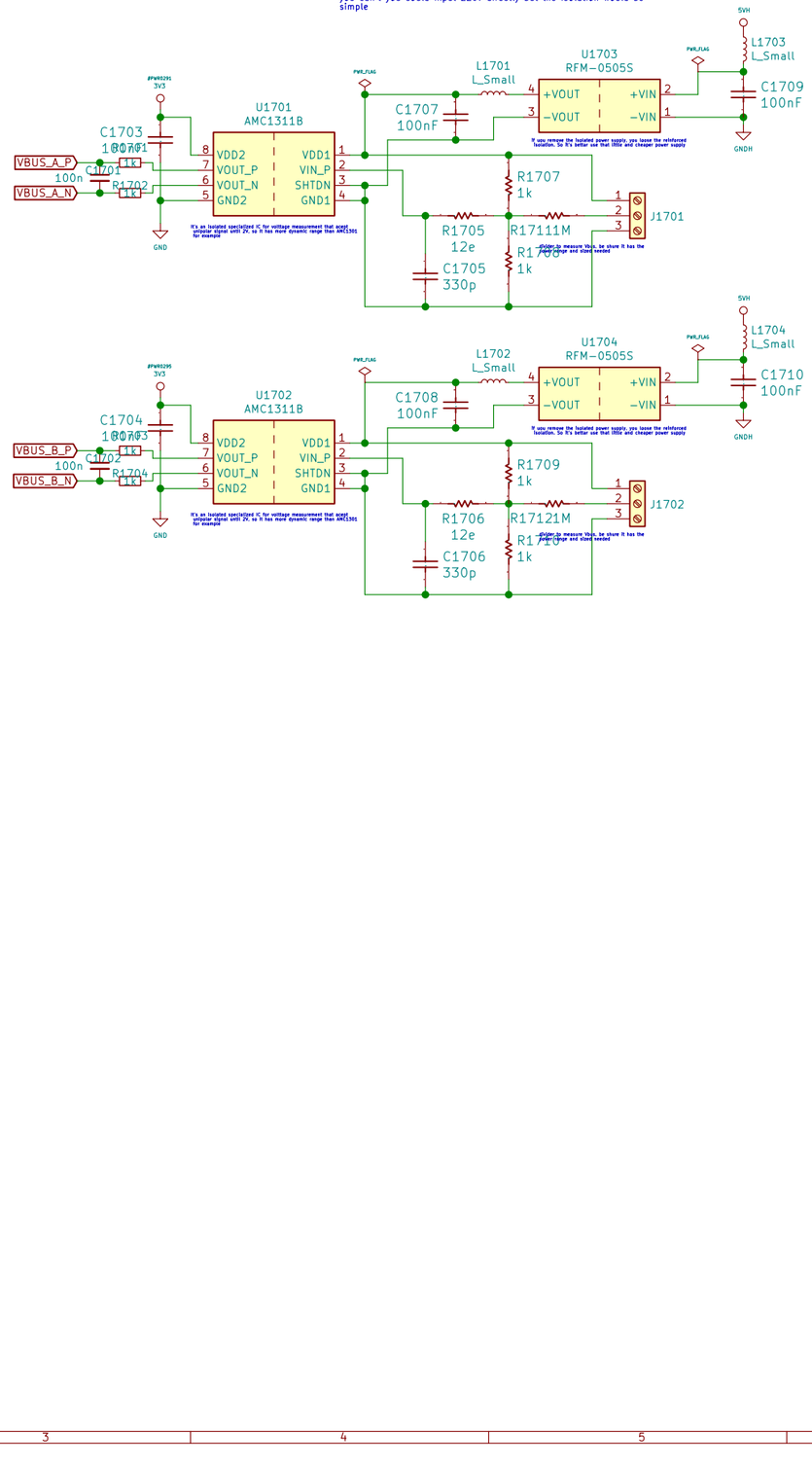
Title: LEM currente measurement

Size: A3	Date: 2020-01-09	Rev: 1.0
KiCad E.D.A. kicad 5.0.2+dfsg1-1		Id: 16/18

VBUS -> R divider -> ISO ADC -> uC

It's intended to measure the Vbus, one per motor, but they cold be joined if both motor share same VBus. The Vbus informatio will be used by the control algorith and to drive the break resistor PWM to protect the rise of the Vbus more than a threshold

The input is expected not to be 220v or 380v. It's supoused to be a isolated low voltage to maintaint the reinforced insulation. In case you can't you could input 220v directly but the isolation would be simple



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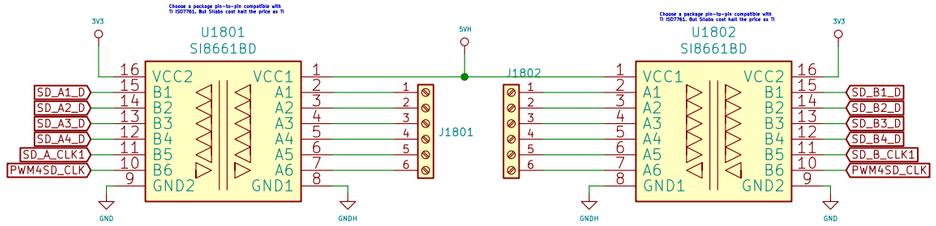
Sheet: /Vbus measurement/		
File: vbus_meas.sch		
Title: Shunt isolated		
Size: A3	Date: 2020-01-09	**Rev: 1.0**
KiCad E.D.A. kicad 5.0.2+dfsg1-1		Id: 17/18

Isolated sigma delta ADC

It's intended for power board circuitery to supply all the signals to control board, the control board will use the SD filter to aquire the data. All the power part will be at power board.

PWM clk output to powerboard and then come back again to maintain delays with respect to SD data channels. On power board you have to respect traces length between clk and data

I use 5VH on power side to be less prone to noise error on the way on connection the two boards (and i've decided to not supply 3v3H too)



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Sheet: /sigma delta interface/ File: sd_interface.sch		
Title: Shunt Sigma Delta isolated		
Size: A3	Date: 2020-01-09	**Rev: 1.0**
KiCad E.D.A. kicad 5.0.2+dfsg1-1		Id: 18/18