SERVO DRIVER BLOCKS

The project is divided in blocks. Each block join a group os signals and circuits depending on his function. The project is liberaided to have reinforced insulation using deutale single isolatios. For that reason, the 4C circuitry is on a cold supply and the output logic is at het supply, BUT take in account that HOT is not 220. It just a name

sigma_delta uC **ENDAT SDELTA GPIO** uc_gpio.sch sigma_delta.sch uC AC **STEP** CLK SYM **TEMP** LEM IN DIR Dbg **VBUS** uC **QEP** UI **MEAS** Power vbus_meas.sch connectors uC **IGBT** CONN **ADC**

ENDAT

t.sch

dir

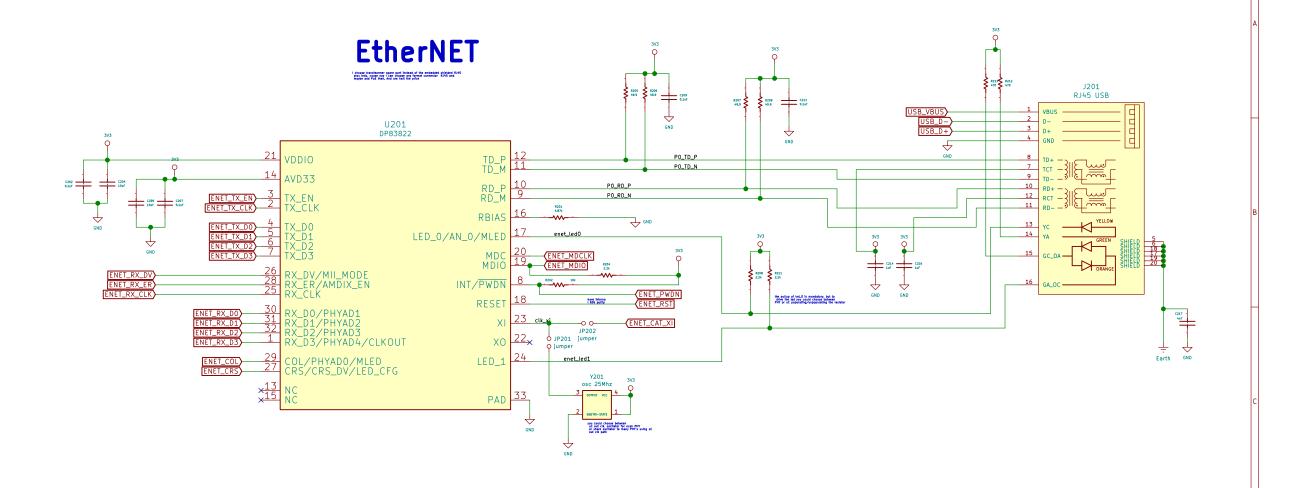
STEP
DIR

Can_rs485

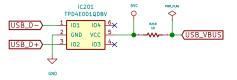
CAN
RS485

Ether NET

Ether CAT



USB HOST



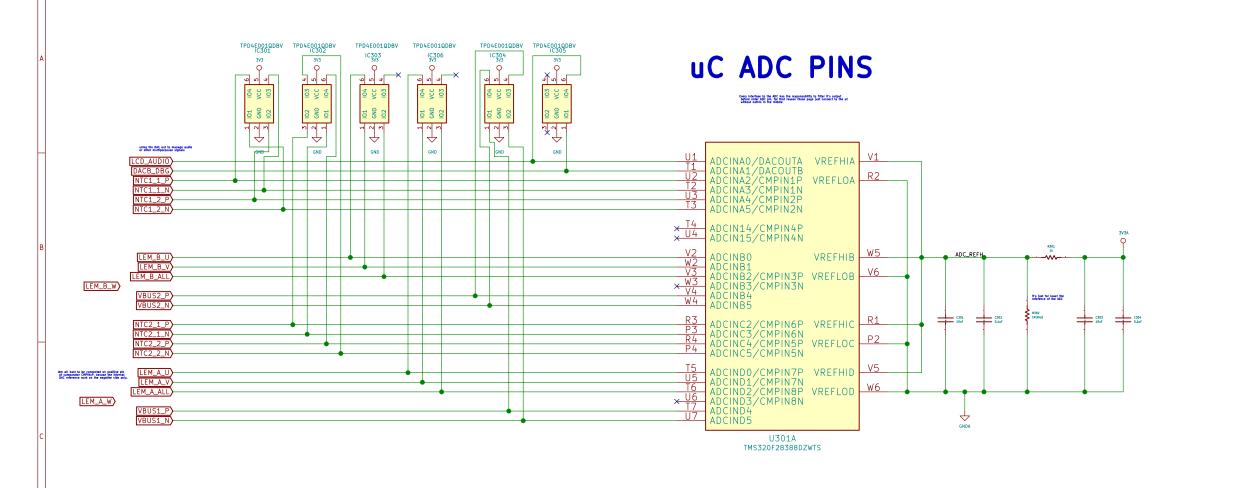
 Pablo Slavkin

 dci
 Sheet: /ethernet/

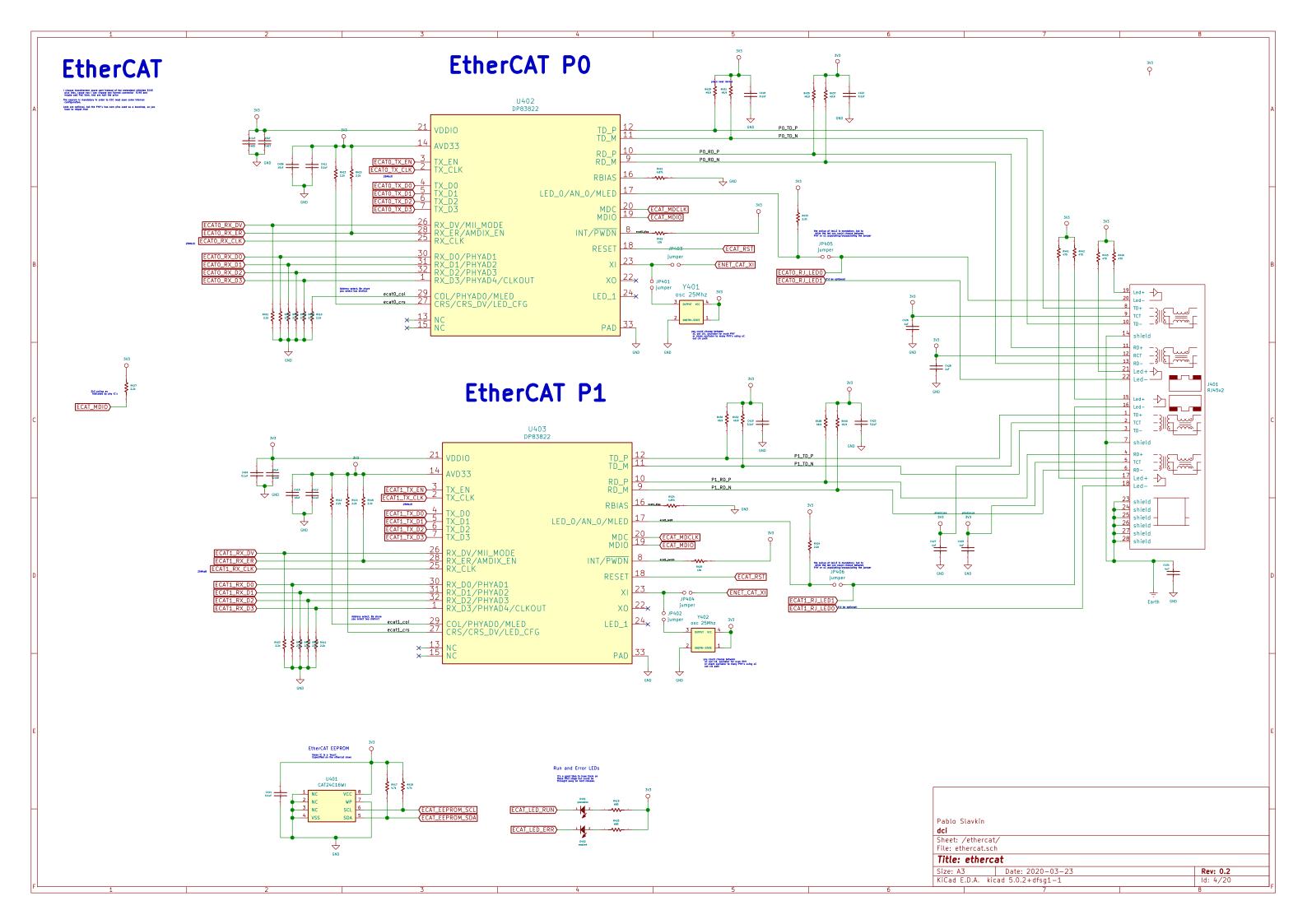
 File: ethernet.sch
 Title: ethernet

 Size: A3
 Date: 2020-03-23
 Rev: 0.2

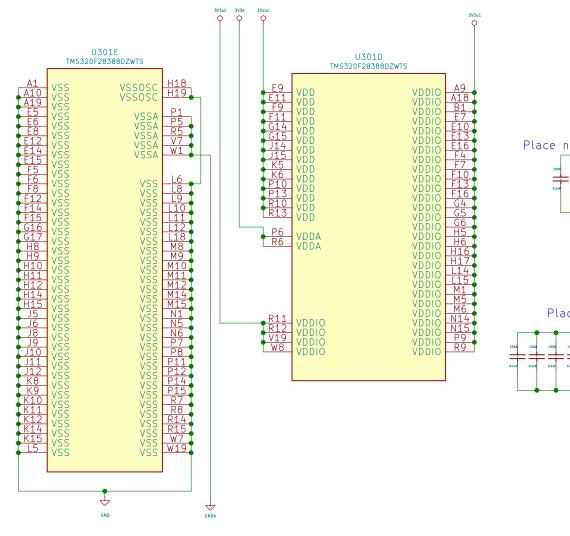
 KiCad E.D.A. kicad 5.0.2+dfsg1-1
 Id: 2/20



KiCad E.D.A. kicad 5.0.2+dfsg1-1

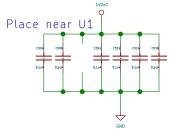


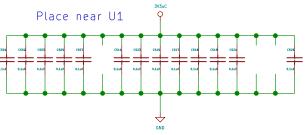
DECOUPLING FILTERS

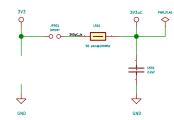


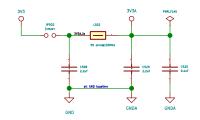
Ferrite Beads Place near U1

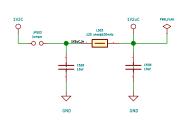




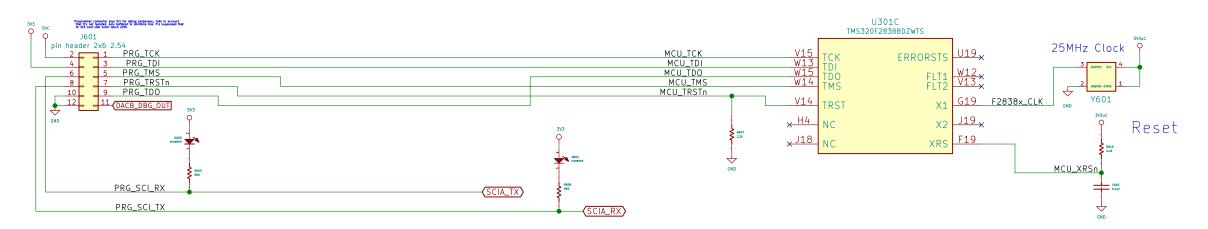




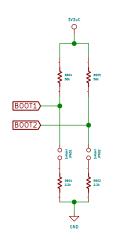




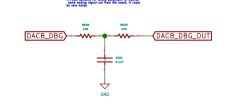
CLK + JTAG + SCI



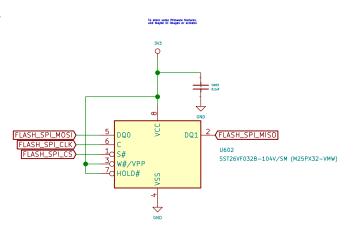
BOOTSRAP R's



ADC/DAC DBG OUT



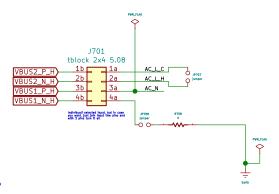
SPI FLASH



| Pablo Slavkin | | |
|----------------------------------|------------------|----------|
| dci | | |
| Sheet: /uc_clk_d | ibg/ | |
| File: uc_clk_dbg | sch | |
| Title: clk | | |
| Size: A3 | Date: 2020-03-23 | Rev: 0.2 |
| KiCad E.D.A. kicad 5.0.2+dfsg1-1 | | ld: 6/20 |
| | 7 | 8 |

Main Power

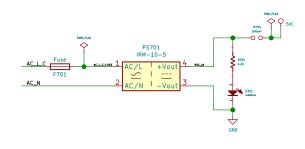
in case the control board have to be supply effectly with societ voltage (220) populate these. It's not a good idea cause I'll the to keep hight voltage outside these controller board, but it's a requeriment, so I let it as an option. But you have the law voltage input 15vc and 15vh connections also commercial and 2 power supply for Cold and first sides because for Colore to and 2 power supply for Cold and first sides because a Colore Colore to the Colo

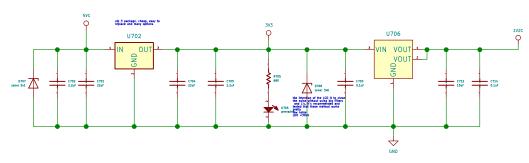


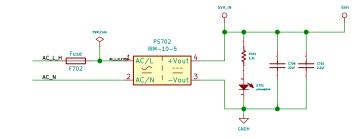
COLD SUPPLY

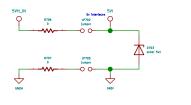
It is inteded to use only, I mean ONLY inside the control board, none of these coopers wires has to leave the board. I isolate every single pin from these supply to go outside, take these in account

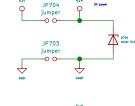
HOT SUPPLY The description for the first same and the description of the same and the description of the same and the sam

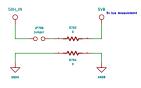








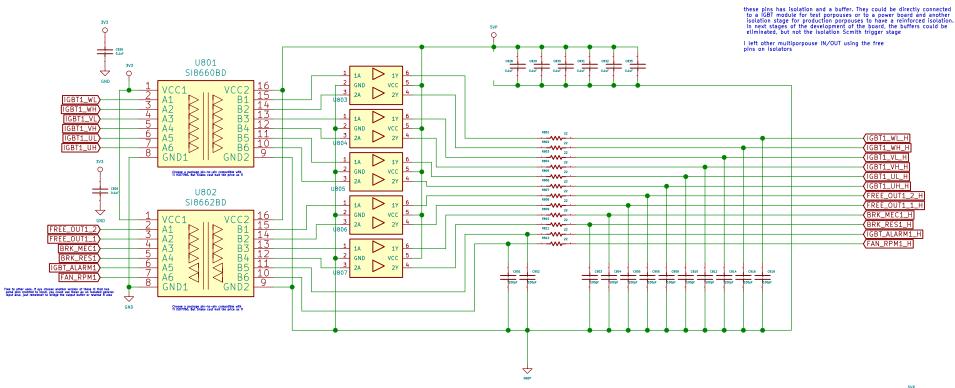


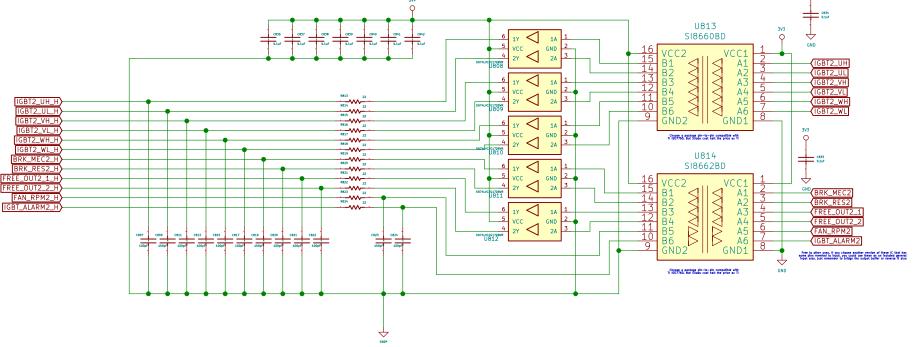


Pablo Slavkin dci
Sheet: /ac_in/
File: ac_in.sch

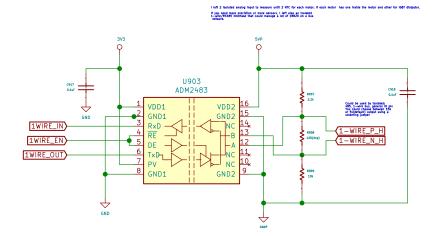
Title: AC input Size: A3 Date: 2020-03-23 KiCad E.D.A. kicad 5.0.2+dfsg1-1

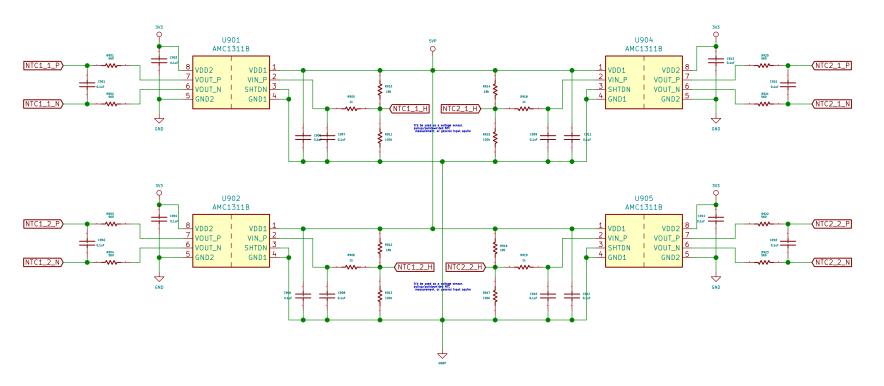
PWM OUT -> ISOLATOR -> BUFFER -> FILTER



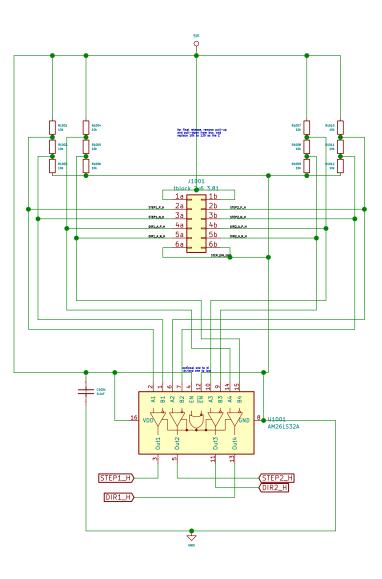


2 isolated NTC interfase + 1 isolated 1-wire/485





Differential STEP-DIR input HOT



Pablo Slavkin

dci

Sheet: /step_dir/
File: step_dir.sch

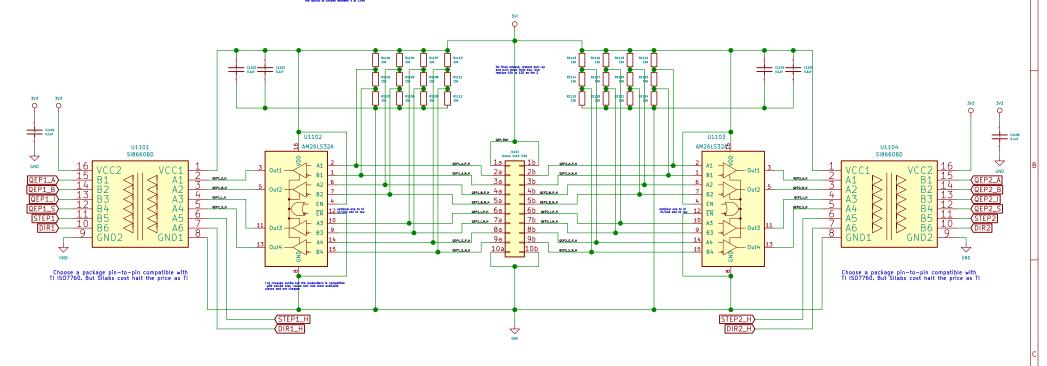
Title: ENDAT/BISS Interface

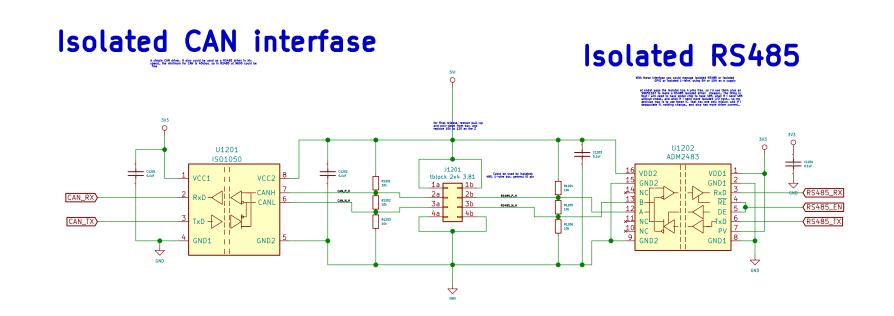
Size: A3 Date: 2020-03-23 Rev: 0.2

KiCad E.D.A. kicad 5.0.2+dfsg1-1 Id: 10/20

2x Isolated Idifferential incremental encoder interfase 5v input A-B-I-S

I left the Input for two Isolated Incremental encoders.
I left the 4 signals Input plus two auxiliary output for eny perpous plu





KiCad E.D.A. kicad 5.0.2+dfsg1-

Symbols Slots fiducials, and others

Case



Fiducials TOP

● H1301 ● H1303 ● H1305 ● H1307 fiducials ● H1307

Fiducials Bottom

H1302 H1304 H1306 H1308 H1308 H1308 H1308

mounting holes

SLOT V LEMs

● H1345 ● H1346 ● H1348 ● H1347 Slot

● H1349 ● H1351 ● H1353 ● H1355 Slot

● H1350 ● H1352 ● H1354 ● H1356 Slot

logo recycler

logo nanocut

logo kicad

OOO pslavkin_bottom

O O O pslavkin_top

4444

logo neurona



logo stackup

logo design

SLOT 'I' anyware

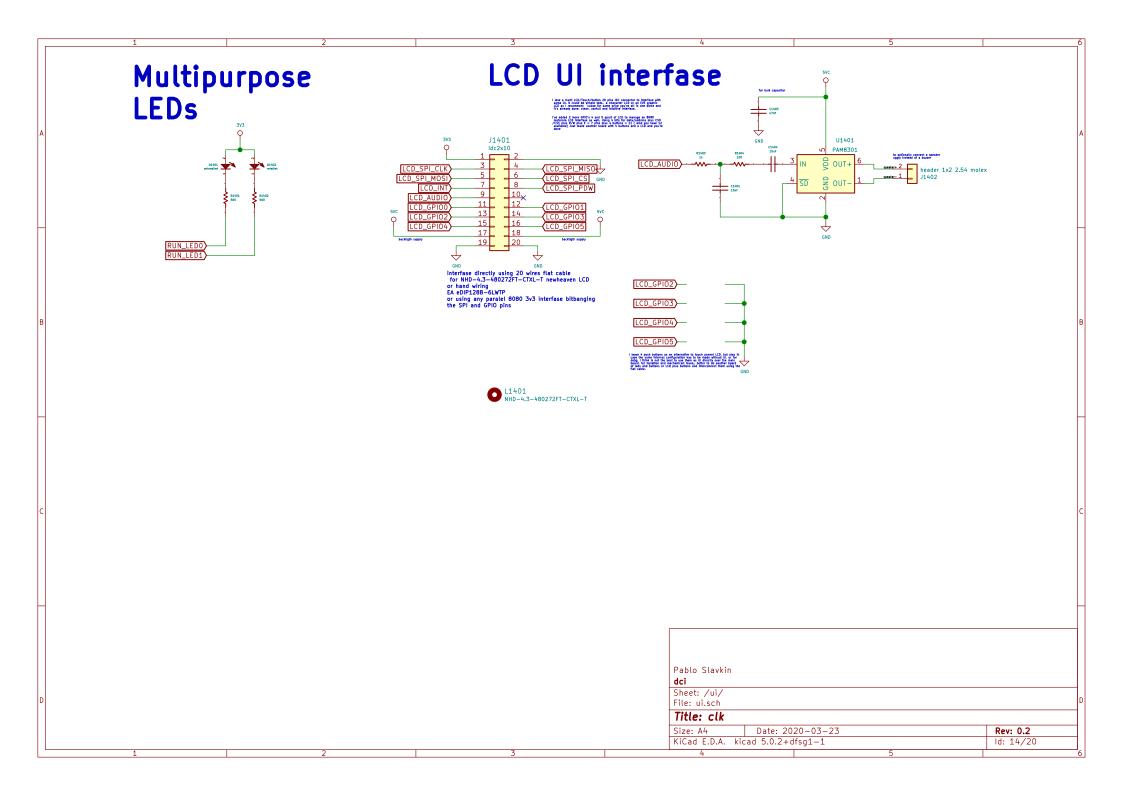
H1338 H1340 H1342 H1344 Slot Slot

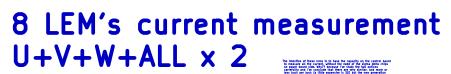
H1358 H1357 Slot

Pablo Slavkin

Sheet: /symbols/ File: symbols.sch Title: gpio

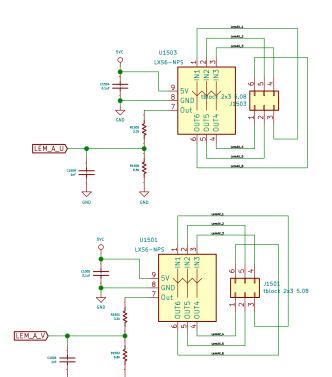
Size: A3 Date: 2020-03-23 KiCad E.D.A. kicad 5.0.2+dfsg1-1

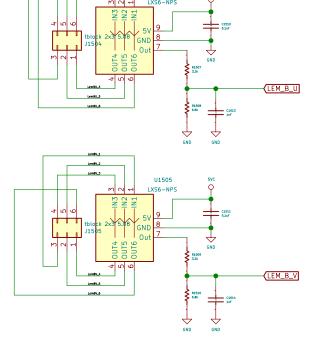


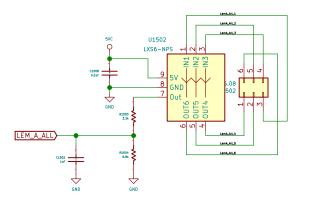


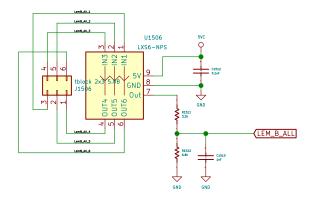
controlled must be approximately a state of policy designed and the controlled must be approximately as the controlled must be

anlog1: I've decided to return to a 2x3 terminal block output 'caus match the size of the LEM









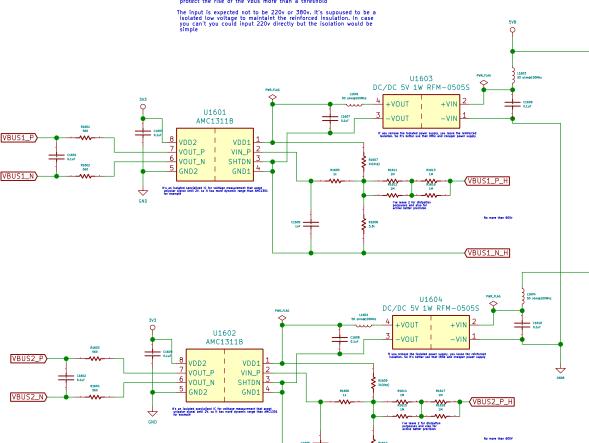
LEM_A_W XLEM_B_W

decided to eliminate 1 LEM, you could use 3 in line measurement, I in line plus one for all. De reason is alze of board and complexity

| Pablo Slavkin | |
|----------------------------------|-----------|
| dci | |
| Sheet: /lem/ File: lem.sch | |
| Title: LEM currente measurement | |
| Size: A3 Date: 2020-03-23 | Rev: 0.2 |
| KiCad E.D.A. kicad 5.0.2+dfsg1-1 | ld: 15/20 |
| 7 | 9. |

VBUS -> R divider -> ISO ADC -> uC

t's intended to measure the Vbus, one per motor, but they cold be joined if both motor share same VBus. The Vbus informatio will be used by the control algorith and to drive the break resistor PWM to



VBUS2_N_H

Pablo Slavkin

dci

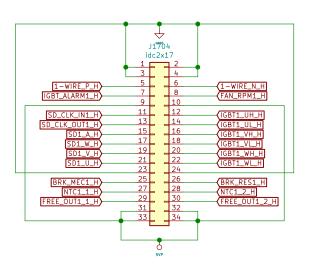
Sheet: //bus meas/
File: vbus_meas.sch

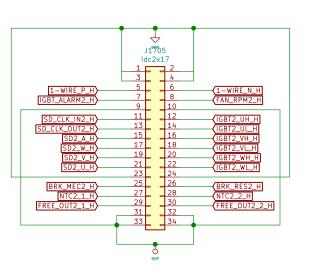
Title: Shunt isolated

Size: A3 Date: 2020-03-23 Rev: 0.2

KiCad E.D.A. kicad 5.0.2+dfsg1-1 Id: 16/20

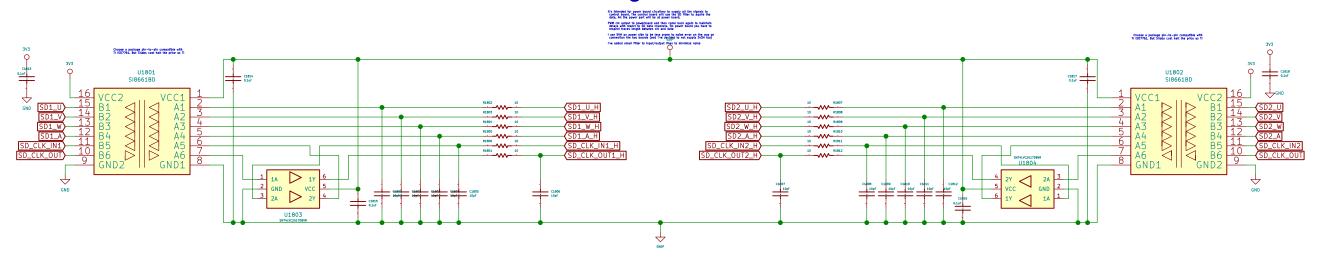
Common Connections





Pablo Slavkin Sheet: /connectors/ File: conn.sch Title: Common connections Size: A3 Date: 2020-03-23 KiCad E.D.A. kicad 5.0.2+dfsg1-1

Isolated sigma delta ADC



Pablo Slavkin

dci

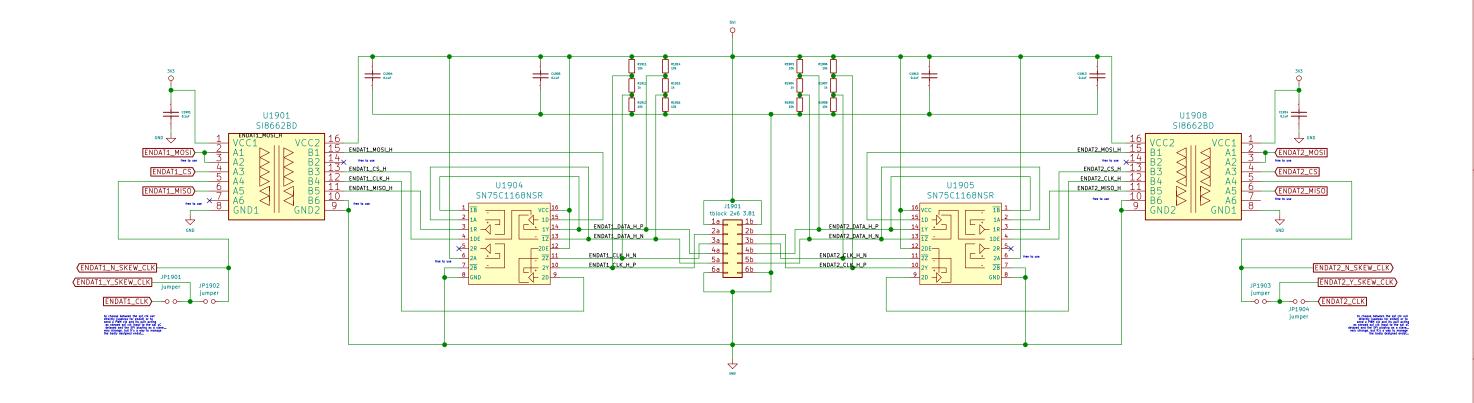
Sheet: /sigma_delta/
File: sigma_delta.sch

Title: Shunt Sigma Delta isolated

Size: A3 Date: 2020-03-23 Rev: 0.2

KiCad E.D.A. kicad 5.0.2+dfsg1-1 Id: 18/20

2X Isolated diferential ENDAT interface



 Pablo Slavkin

 dci
 Sheet: /endat/

 File: endat.sch

 Title: ENDAT/BISS Interface

 Size: A3
 Date: 2020-03-23
 Rev: 0.2

 KiCad E.D.A. kicad 5.0.2+dfsg1-1
 Id: 19/20

uC GPIO's pins

I've spend hours to choose the GPIO's for each laterface trying to not creat one to the other, just pay attention if you wanna move some I've used global labels connector to go from one page to another isseed the off-page connector because it's more proue to errors. I know that is not too controllor, but I've better and fastly for now

