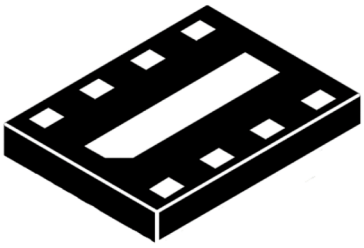
1 A very low dropout fast transient ultra-low noise linear regulator



DFN8 1.2 x 1.6 mm

Features

- Input voltage from 1.8 to 5.5 V
- Ultra-low dropout voltage (120 mV typ. at 1 A load and V_{OUT} = 3.3 V)
- Very low quiescent current (100 µA typ. at no-load, 0.03 µA typ. in off mode)
- Output voltage tolerance: ± 1% from -40 °C to +85 °C
- Ultra-low Noise: 13 µV RMS Noise from 10 Hz to 100 kHz at V_{OUT} = 3.0 V
- High PSRR (70 dB@1 kHz)
- Wide range of output voltages available on request: from 1.0 V up to 5.0 V in 50 mV step
- Logic-controlled electronic shutdown
- Internal soft-start
- Optional output voltage discharge feature
- Compatible with ceramic capacitor C_{OUT} = 1 µF
- Internal current limit foldback and thermal protections
- Available in DFN8 (1.2x1.6 mm)
- Operating temperature range: -40 °C to 125 °C

Applications

- Mobile phones
- Tablets
- Battery-powered systems
- Camera supply

Maturity status link
LD56100

Description

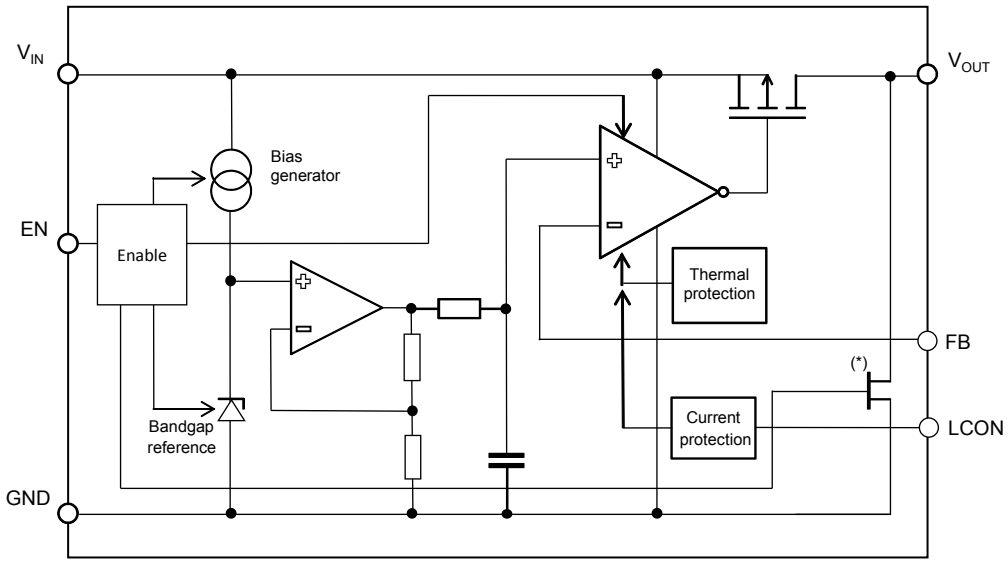
The LD56100 high accuracy voltage regulator provides 1 A of current from an input voltage ranging from 1.8 V to 5.5 V, with a typical dropout voltage of 120 mV.

It is available in DFN8 (1.2 x 1.6 mm) package, allowing the maximum space saving.

The device is stabilized with a ceramic capacitor on the output. The ultra-low drop voltage, low quiescent current and fast transient response, together with the internal soft-start circuit, make the LD56100 suitable for low power battery-operated applications.
An enable logic control function puts the LD56100 in shutdown mode allowing a total current consumption lower than 0.1 µA. Short-circuit protection with current limit foldback and thermal protection are also included.

1 Diagram

Figure 1. Block diagram



Note: (*) The output discharge MOSFET is optional.

2 Pin configuration

Figure 2. **Pin connection (top view)**

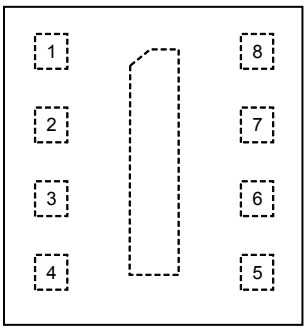
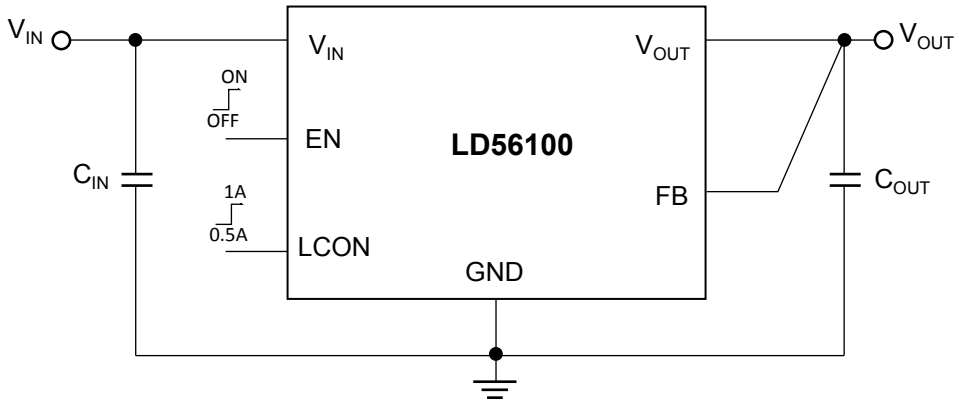


Table 1. **Pin description**

Pin # DFN8	Symbol	Function
1	V_{OUT}	Output voltage
2	V_{OUT}	
3	LCON	Current limit selection. High 1 A, low 0.5 A
4	FB	Feedback pin, to be connected as close as possible to the load positive terminal
5	GND	Common ground
6	EN	Enable pin logic input: low = shutdown, high = active
7	V_{IN}	Input voltage
8	V_{IN}	
Thermal pad	GND	Connect to GND on the PCB

3 Typical application

Figure 3. **Typical application circuit**



4 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input voltage	- 0.3 to 7	V
V_{OUT}	Output voltage	- 0.3 to V_{IN} + 0.3	V
V_{EN}, FB, LCON	Enable and feedback input voltage	- 0.3 to 7	V
I_{OUT}	Output current	Internally limited	mA
P_D	Power dissipation	Internally limited	mW
T_{STG}	Storage temperature range	- 40 to 150	°C
T_{OP}	Operating junction temperature range	- 40 to 125	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	80	°C/W

Table 4. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD Protection voltage	HBM	2	kV
		CDM	500	V

5 Electrical characteristics

V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or V_{IN} = 1.8 V if greater; C_{IN} = C_{OUT} = 1 µF, I_{OUT} = 1 mA, V_{EN} = 1.2 V, typical values are at T_J = 25 °C; min./max. values are at -40 °C ≤ T_J ≤ 125 °C, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage			1.8		5.5	V
V_{OUT}	V_{OUT} accuracy	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V; I_{OUT} = 0 to 1 A; -40 °C ≤ T_J ≤ 85 °C		-1.0		1.0	%
		$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V; I_{OUT} = 0 to 1 A; -40 °C ≤ T_J ≤ 125 °C		-2.0		1.0	%
ΔV_{OUT}	Static line regulation (1)	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 5.0 V, I_{OUT} = 10 mA			0.002	0.06	%/V
ΔV_{OUT}	Static load regulation	I_{OUT} = 10 mA to 1000 mA			2	6	mV
V_{DROP}	Dropout voltage	I_{OUT} = 1 A; V_{OUT} = $V_{OUT(NOM)}$ -0.1 V	$V_{OUT(NOM)}$ = 1.2 V (2)		370	585	mV
			$V_{OUT(NOM)}$ = 1.75 V		220	295	
			$V_{OUT(NOM)}$ = 1.8 V		200	285	
			$V_{OUT(NOM)}$ = 1.85 V		195	280	
			$V_{OUT(NOM)}$ = 2.5 V (2)		140	190	
			$V_{OUT(NOM)}$ = 2.8 V (2)		130	175	
			$V_{OUT(NOM)}$ = 3.0 V		125	165	
			$V_{OUT(NOM)}$ = 3.3 V		120	155	
			$V_{OUT(NOM)}$ = 3.5 V (2)		100	145	
			$V_{OUT(NOM)}$ = 3.9 V (2)		90	135	
e_N	Output noise voltage	10 Hz to 100 kHz, I_{OUT} = 10 mA, V_{OUT} = 3.0 V			13		μV_{RMS}
SVR	Supply voltage rejection	V_{IN} = $V_{OUT(NOM)}$+ 1 V +/- V_{RIPPLE} V_{RIPPLE} = 0.2 V Freq = 1 kHz, I_{OUT} = 30 mA			70		dB
		V_{IN} = $V_{OUT(NOM)}$+ 1 V +/- V_{RIPPLE} V_{RIPPLE} = 0.2 V freq. = 100 kHz I_{OUT} = 30 mA			55		
I_Q	Quiescent current	I_{OUT} = 0 mA			100	155	µA
$I_{Standby}$	Standby current	V_{IN} input current in OFF MODE: V_{EN} = GND			0.03	2.0	µA
I_{LIM}	Output current limit	V_{OUT} = 0.9 x $V_{OUT(NOM)}$; LCON=V_{IN} or floating		1100	1600		mA
		V_{OUT}= 0.9 x $V_{OUT(NOM)}$; LCON=GND		600	800		
I_{SC}	Short-circuit current	V_{OUT} = 0 (foldback protection); LCON=V_{IN} or floating V_{IN} < 5.0 V			400		mA
		V_{OUT} = 0 (foldback protection); LCON=GND, V_{IN} < 5.0 V			180		
R_{ON}	Output voltage discharge MOSFET	(LD56100DT version)			40		Ω

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{EN}	Enable input logic low	V_{IN} = 1.8 V to 5.5 V			0.4	V
	Enable input logic high	V_{IN} = 1.8 V to 5.5 V	1			
I_{EN}	Enable pin input current			100	400	nA
V_{LCON}	LCON input logic low	V_{IN} = 1.8 V to 5.5 V			0.4	V
	LCON input logic high	V_{IN} = 1.8 V to 5.5 V	1			
I_{LCON}	LCON pin current	LCON=GND		550	700	nA
		LCON = V_{IN}		0.1	1	
T_{ON} (3)	Turn-on time	V_{OUT} = 1.8 V		60		µs
T_{SHDN}	Thermal shutdown			170		°C
	Hysteresis			20		
C_{OUT}	Output capacitor		1.0		22	µF

1. *Not applicable for $V_{OUT(NOM)}$≥ 5.0 V.*
2. *Simulation data.*
3. *Turn-on time is time measured between the enable input just exceeding VEN high value and the output voltage just reaching 95 % of its nominal value.*

6 Application information

6.1 Soft-start function

The LD56100 has an internal soft-start circuit. By increasing the start-up time up to 100 µs, without the need of any external soft-start capacitor, this feature is able to keep the regulator inrush current at start-up under control.

6.2 Output discharge function

The LD56100 integrates a MOSFET connected between V_{out} and GND. This transistor is activated when the EN pin goes to low logic level and has the function to quickly discharge the output capacitor when the device is disabled by the user.

The device is available with or without the auto-discharge feature.

See Ordering information for more details.

6.3 Short-circuit and current limitation

The LD56100 is protected against short-circuit on the output. When the load current increases above 1.6 A typical the device starts limiting it to the I_{LIM} value. If the load resistance decreases even more then the foldback, circuit starts limiting the current to 0.4 A when V_{OUT} = 0.

When pulling LCON pin to ground, the I_{LIM} and I_{SC} values are reduced to 0.8 A and 0.18 A respectively.

6.4 Input and output capacitors

The LD56100 requires external capacitors to assure the regulator control loop stability.

Any good quality ceramic capacitor can be used but, the X5R and the X7R are suggested since they guarantee a very stable combination of capacitance and ESR overtemperature.

Locating the input/output capacitors as closer as possible to the relative pins is recommended.

The LD56100 requires an input capacitor with a minimum value of 1 µF. This capacitor must be located as close as possible to the input pin of the device and returned to a clean analog ground.

The control loop is designed to be stable with any good quality output ceramic capacitor (such as X5R/X7R types) with a minimum value of 1 µF and equivalent series resistance in the [3 – 300 mΩ] range. It is important to highlight that the output capacitor must maintain its capacitance and ESR in the stable region over the full operating temperature, load and input voltage ranges, to assure stability. Therefore, capacitance and ESR variations must be taken into account in the design phase to ensure the device works in the expected stability region.

The suggested combination of 1 µF input and output capacitors offers a good compromise among the stability of the regulator, optimum transient response and total PCB area occupation.

7 Typical characteristics

(C_{IN} = C_{OUT} = 1 µF, V_{OUT} = 3.0 V, V_{EN} to V_{IN}, T_J = 25 °C unless otherwise specified)

Figure 4. Output voltage vs. temperature (V_{IN} = 3.0 V, I_{OUT} = 1 mA, normal mode)

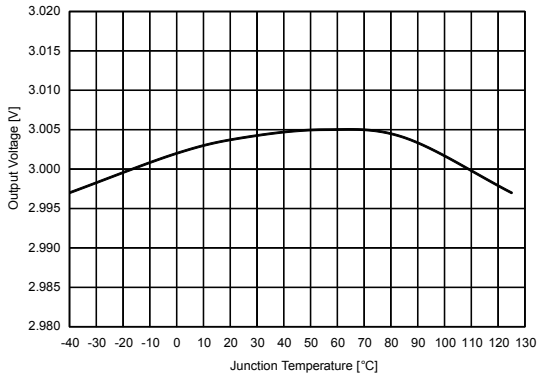


Figure 5. Output voltage vs. temperature (V_{IN} = 3.0 V, I_{OUT} = 1 A, normal mode)

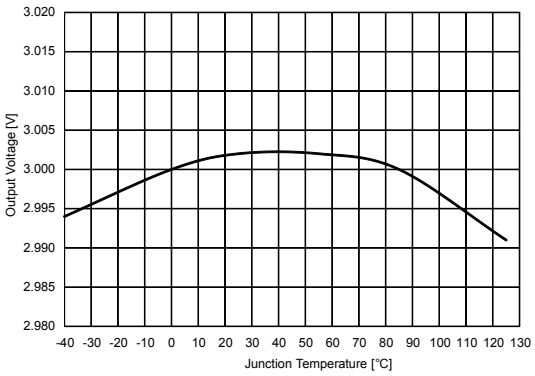


Figure 6. Line regulation vs. temperature (V_{OUT} = 3.0 V, I_{OUT} = 1 mA)

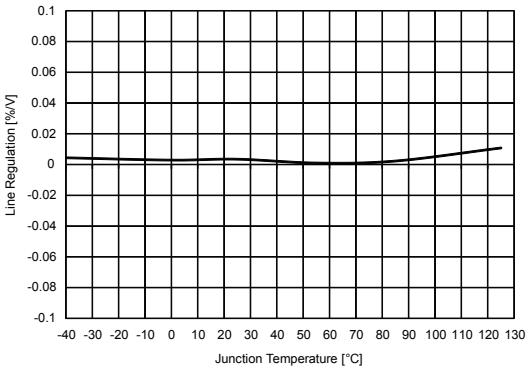


Figure 7. Load regulation vs. temperature (V_{OUT} = 3.0 V, I_{OUT} = 1 A to 10 mA)

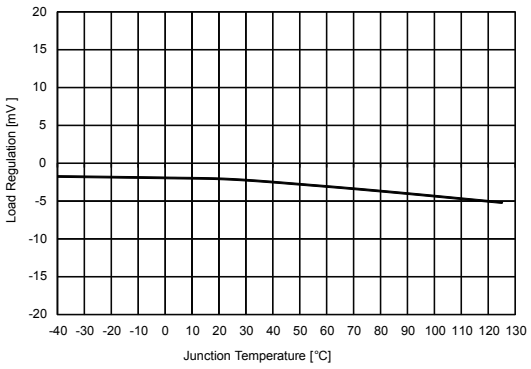


Figure 8. Quiescent current vs. temperature (V_{OUT} = 3.0 V, I_{OUT} = 0 mA)

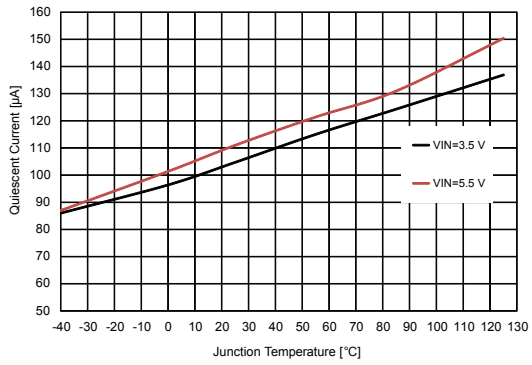


Figure 9. Quiescent current vs. temperature (V_{OUT} = 3.0 V)

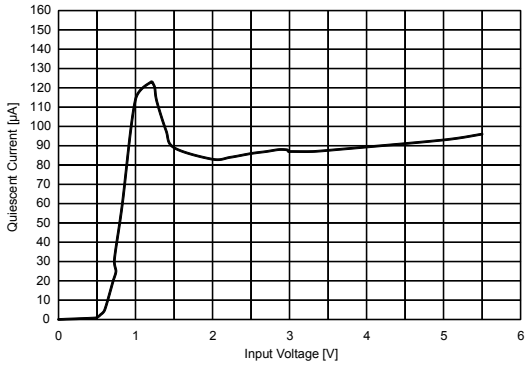


Figure 10. Quiescent current vs. temperature (V_{IN} = 3.5 V, I_{OUT} = 3.0 mA)

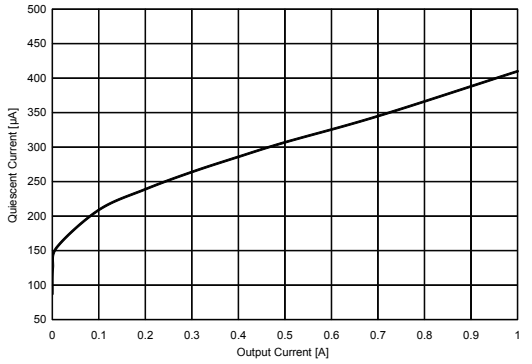


Figure 11. Output voltage vs. input voltage (I_{OUT} = 1 mA)

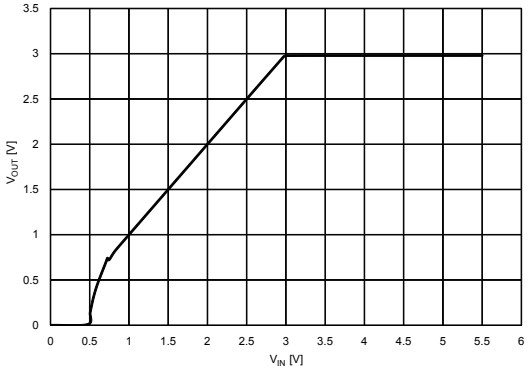


Figure 12. Dropout voltage vs. load current

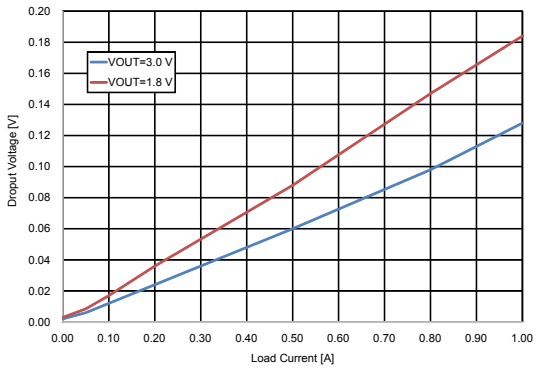


Figure 13. Dropout voltage vs. temperature (V_{OUT} = 3.0 V; I_{OUT} = 1 A)

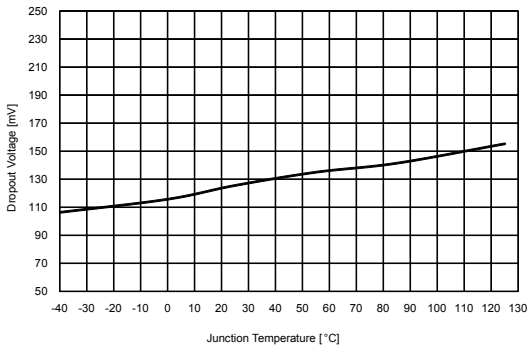


Figure 14. Foldback characteristic (LCON = V_{IN})

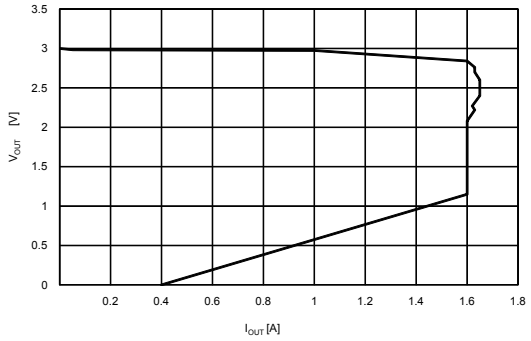


Figure 15. Foldback characteristic (LCON = GND)

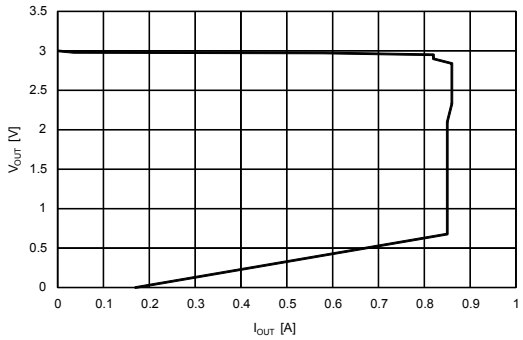


Figure 16. Supply voltage rejection vs. frequency (V_{OUT} = 3.0 V; I_{OUT} = 1 mA)

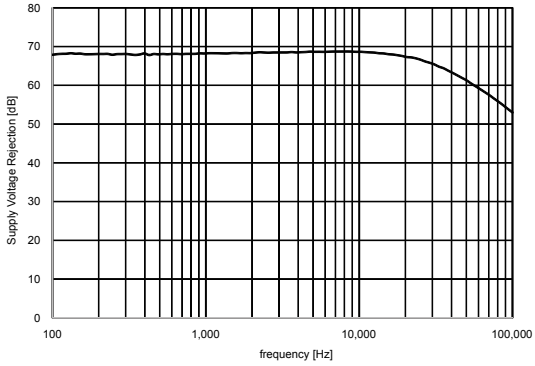


Figure 17. Noise spectral density (V_{OUT} = 3.0 V; I_{OUT} = 10 mA)

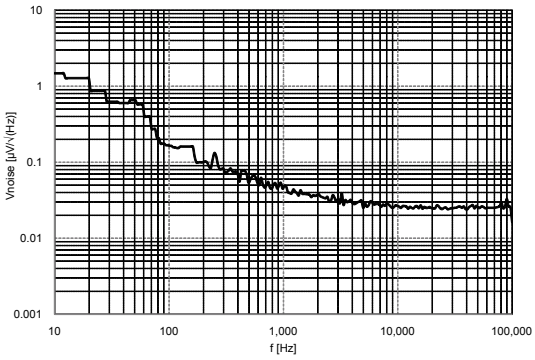


Figure 18. EN current vs. temperature

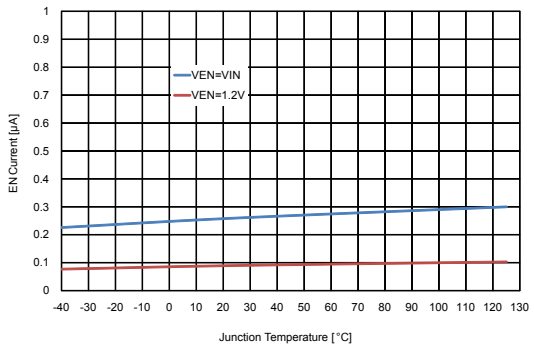


Figure 19. LCON current vs. temperature

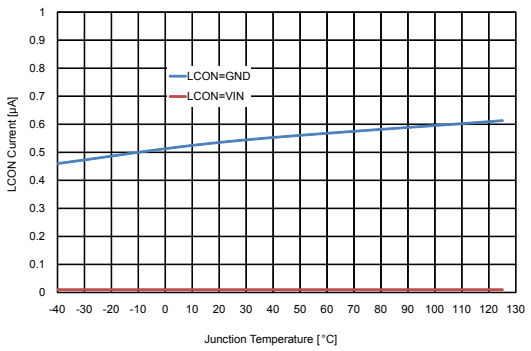


Figure 20. Line transient (V_{IN} = 3.5 V to 4.5 V; I_{OUT} = 1 mA)

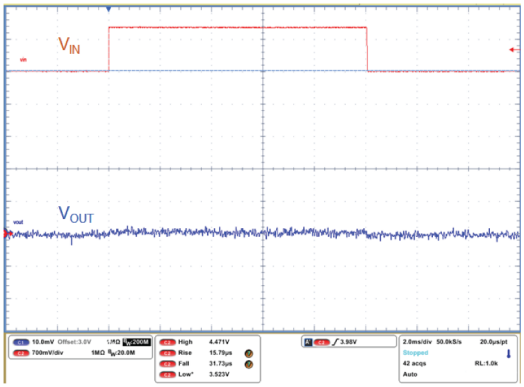


Figure 21. Turn-on V_{IN} driven (V_{IN} = V_{EN} = 0 V to 3.5 V; I_{OUT} = 1 mA)

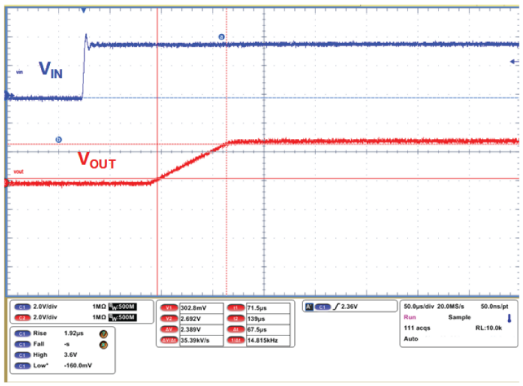


Figure 22. Turn-on driven light load (V_{IN} = 3.5 V; V_{EN} = 0 V to V_{IN}; t_{RISE} = 1 µs; I_{OUT} = 1 mA)

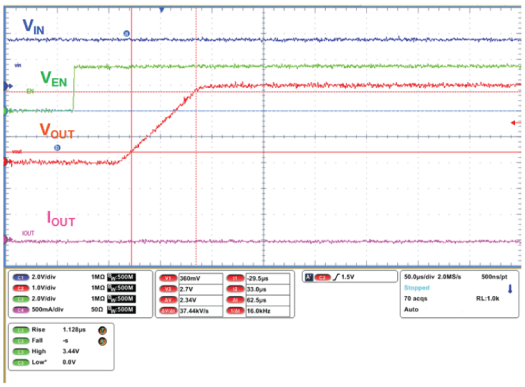


Figure 23. Turn-on driven full load (V_{IN} = 3.5 V; V_{EN} = 0 V; t_{RISE} = 1 µs; I_{OUT} = 1 A)

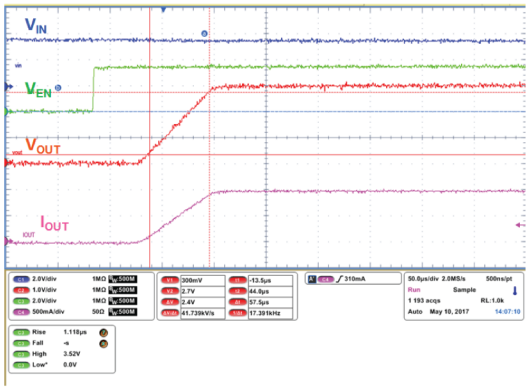
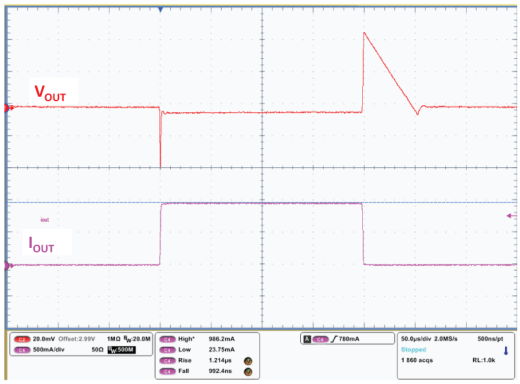


Figure 24. Load transient (V_{IN} = V_{EN} = 3.5 V; t_{RISE}= 1 µs; I_{OUT} = 1 mA to 1 A)



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

8.1 DFN8 (1.6x1.2 mm) package information

Figure 25. **DFN8 (1.6x1.2 mm) package outline**

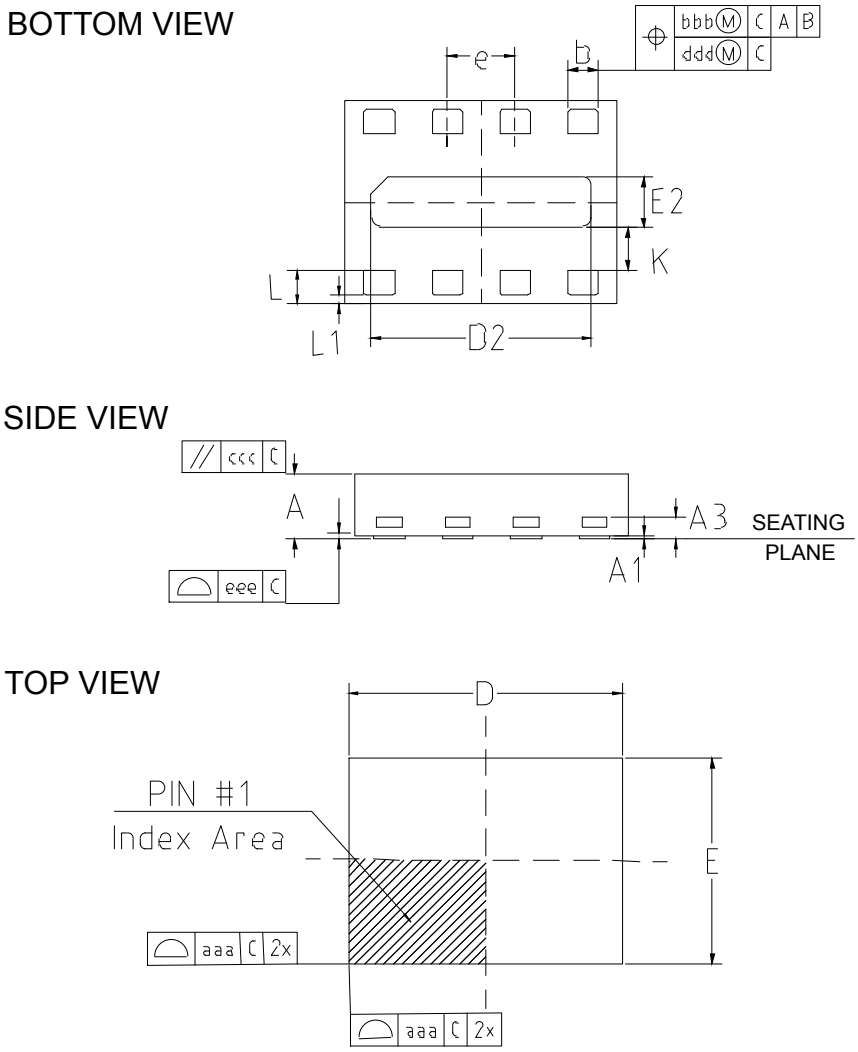


Table 6. DFN8 (1.6x1.2 mm) package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.40	0.45	0.50
A1	0.00	0.02	0.05
A3		0.127 Ref.	
b	0.13	0.18	0.23
D		1.60 BSC	
E		1.20 BSC	
e		0.40 BSC	
D2	1.20	1.30	1.40
E2	0.20	0.30	0.40
K	0.20		
L	0.15	0.20	0.25
L1		0.05 Ref.	

Figure 26. DFN8 (1.6x1.2 mm) recommended footprint

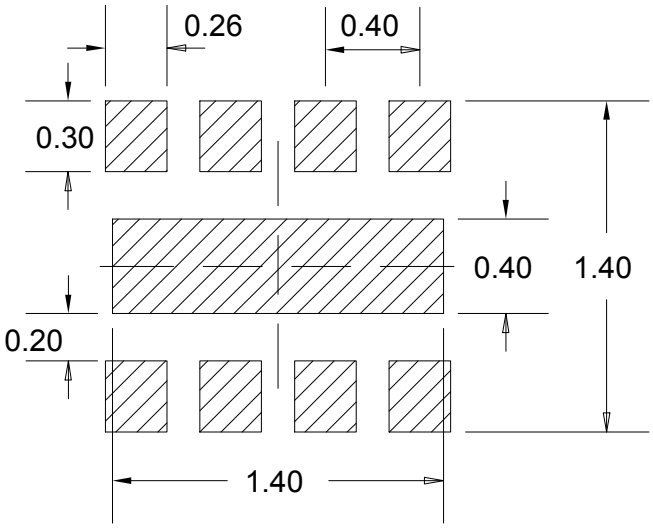
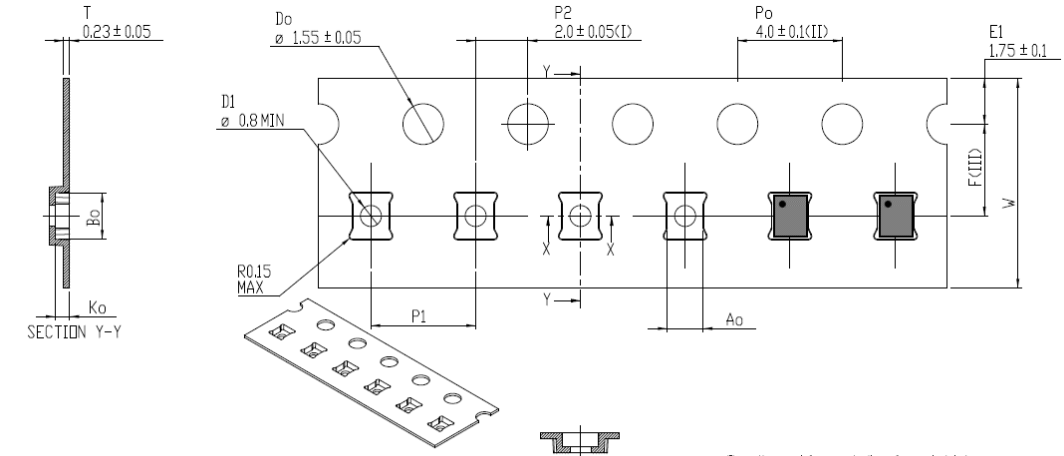


Figure 27. Carrier tape information



Ao	1.37	+/- 0.05
Bo	1.77	+/- 0.05
Ko	0.55	+/- 0.05
F	3.50	+/- 0.05
P 1	4.00	+/- 0.1
W	8.00	+0.3/-0.1

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

9 Ordering information

Table 7. **Order code**

Order code	Output voltage (V)	Auto-discharge	Marking
LD56100DPU115R	1.15	Yes	S1E
LD56100DPU125R	1.25	Yes	S1F
LD56100DPU15R	1.5	Yes	S15
LD56100DPU175R	1.75	Yes	S1A
LD56100DPU18R	1.8	Yes	S18
LD56100DPU185R	1.85	Yes	S1B
LD56100DPU28R	2.8	Yes	S28
LD56100DPU30R	3.0	Yes	S30
LD56100DPU31R	3.1	Yes	S31
LD56100DPU33R	3.3	Yes	S33

Revision history

Table 8. **Document revision history**

Date	Revision	Changes
09-Jan-2018	1	Initial release.

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