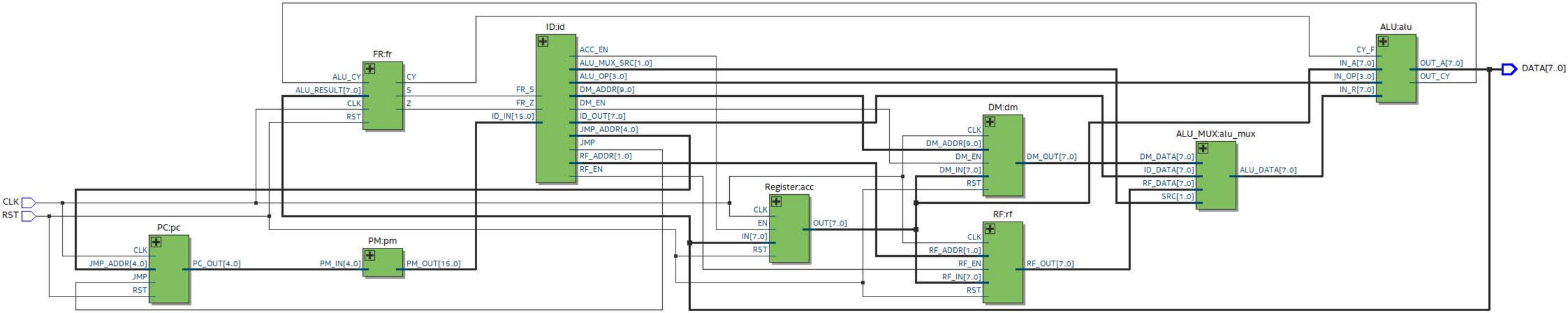
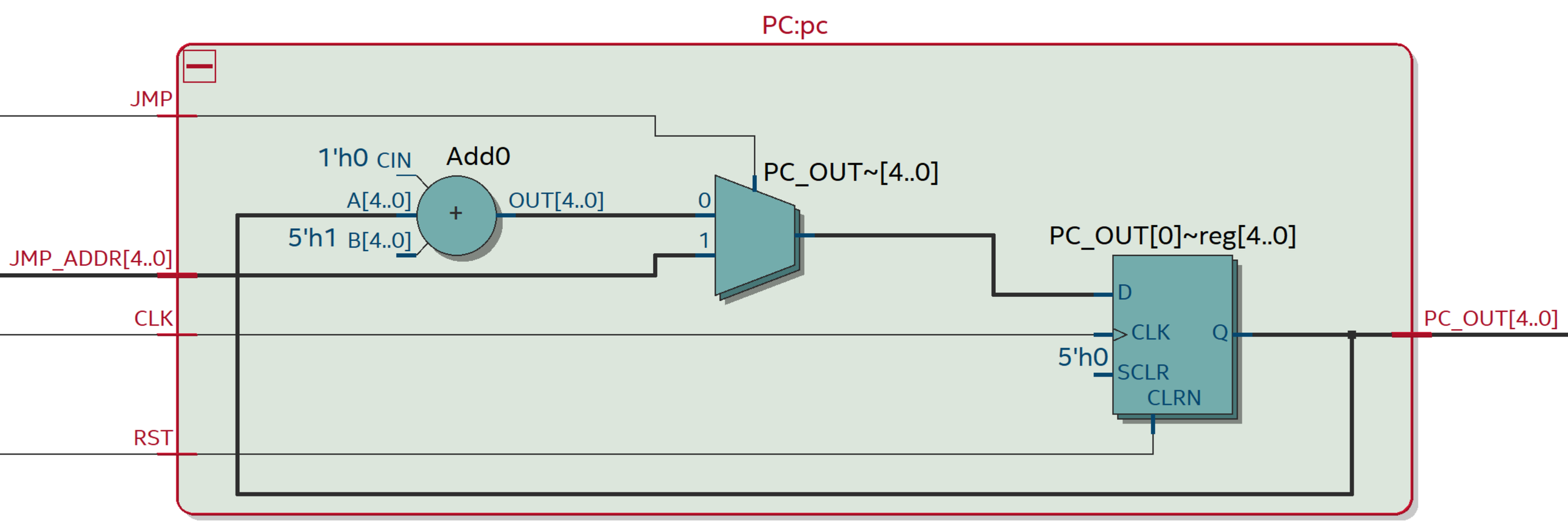
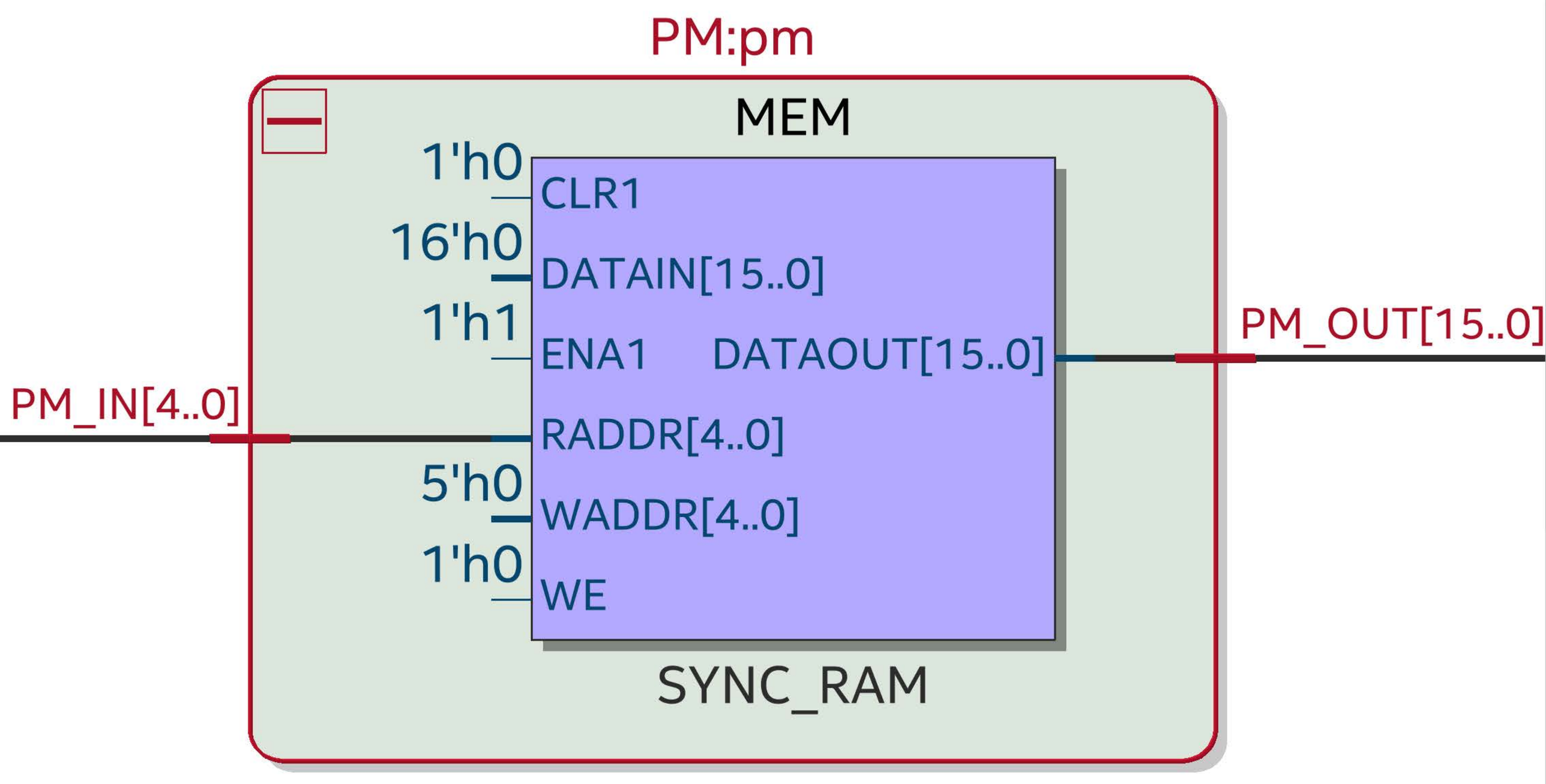
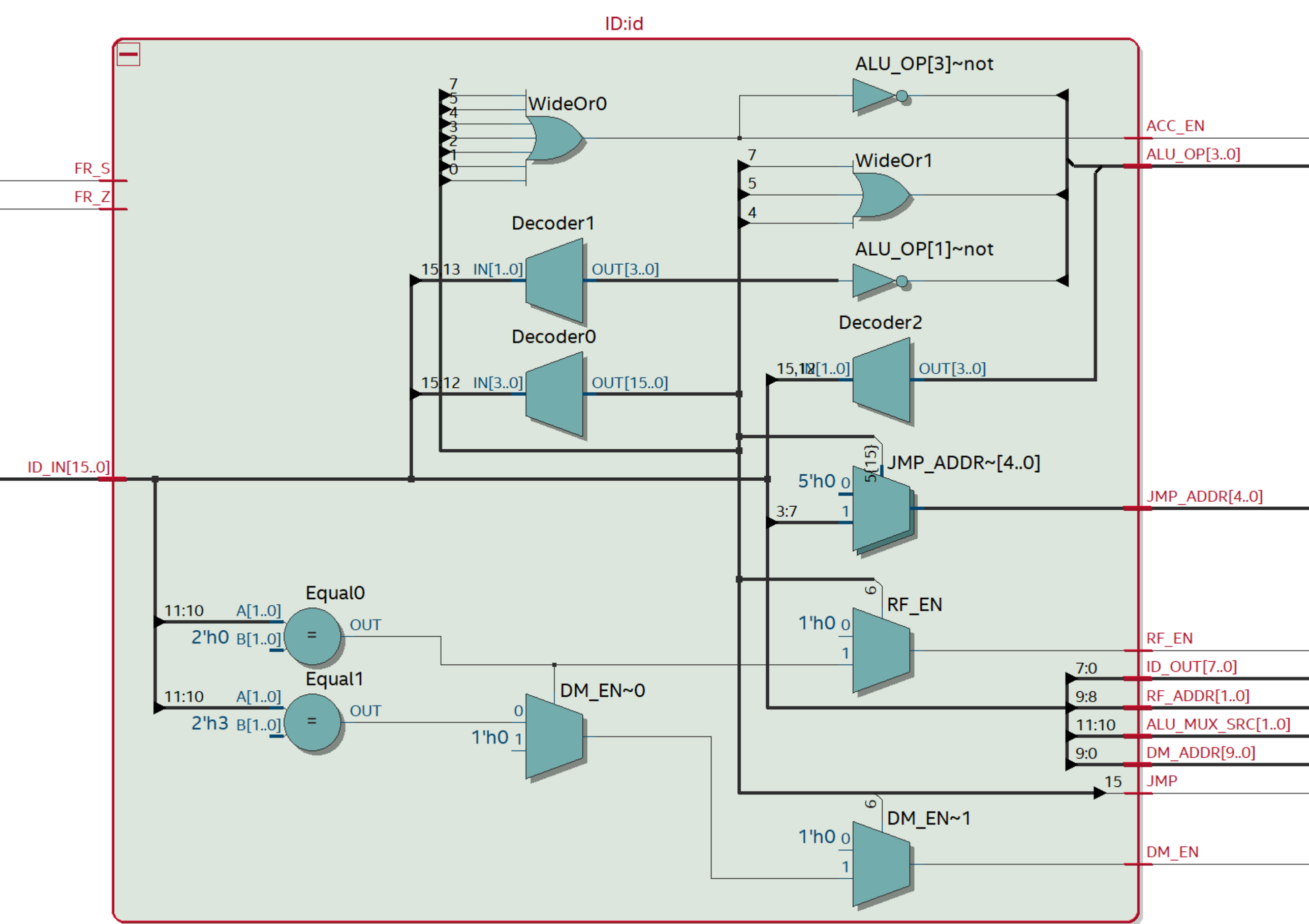

CLK
RST
PC:pc
CLK
JMP_ADDR[4..0]
JMP
RST
PC_OUT[4..0]
PM:pm
PM_IN[4..0]
PM_OUT[15..0]
FR:fr
ALU_CY
ALU_RESULT[7..0]
CLK
RST
CY
S
Z
ID:id
FR_S
FR_Z
ID_IN[15..0]
ACC_EN
ALU_MUX_SRC[1..0]
ALU_OP[3..0]
DM_ADDR[9..0]
DM_EN
ID_OUT[7..0]
JMP_ADDR[4..0]
JMP
RF_ADDR[1..0]
RF_EN
Register:acc
CLK
EN
IN[7..0]
RST
OUT[7..0]
DM:dm
CLK
DM_ADDR[9..0]
DM_EN
DM_IN[7..0]
RST
DM_OUT[7..0]
RF:rf
CLK
RF_ADDR[1..0]
RF_EN
RF_IN[7..0]
RST
RF_OUT[7..0]
ALU_MUX:alu_mux
DM_DATA[7..0]
ID_DATA[7..0]
RF_DATA[7..0]
SRC[1..0]
ALU_DATA[7..0]
ALU:alu
CY_F
IN_A[7..0]
IN_OP[3..0]
IN_R[7..0]
OUT_A[7..0]
OUT_CY
DATA[7..0]


PC:pc
JMP
JMP_ADDR[4..0]
CLK
RST
1'h0 CIN
Add0
A[4..0]
5'h1 B[4..0]
+
OUT[4..0]
0
1
PC_OUT~[4..0]
PC_OUT[0]~reg[4..0]
D
CLK
Q
5'h0
SCLR
CLRN
PC_OUT[4..0]


PM:pm
MEM
1'h0
CLR1
16'h0
DATAIN[15..0]
1'h1
ENA1
DATAOUT[15..0]
PM_OUT[15..0]
PM_IN[4..0]
RADDR[4..0]
5'h0
WADDR[4..0]
1'h0
WE
SYNC_RAM


ID:id
FR_S
FR_Z
ID_IN[15..0]
WideOr0
7
5
4
3
2
1
0
ALU_OP[3]~not
WideOr1
7
5
4
ALU_OP[1]~not
ACC_EN
ALU_OP[3..0]
Decoder1
15:13
IN[1..0]
OUT[3..0]
Decoder0
15:12
IN[3..0]
OUT[15..0]
Decoder2
15:12
IN[1..0]
OUT[3..0]
JMP_ADDR~[4..0]
5'h0
0
1
3:7
5[15]
JMP_ADDR[4..0]
Equal0
11:10
A[1..0]
2'h0
B[1..0]
=
OUT
Equal1
11:10
A[1..0]
2'h3
B[1..0]
=
OUT
DM_EN~0
0
1'h0
1
RF_EN
6
1'h0
0
1
RF_EN
7:0
ID_OUT[7..0]
9:8
RF_ADDR[1..0]
11:10
ALU_MUX_SRC[1..0]
9:0
DM_ADDR[9..0]
15
JMP
DM_EN~1
6
1'h0
0
1
DM_EN

RF:rf

CLK
RF_IN[7..0]
RF_EN
RST
RF_ADDR[1..0]

Decoder0
IN[1..0]
OUT[3..0]

Registers~[31..24]
Registers~[23..16]
Registers~[15..8]
Registers~[7..0]

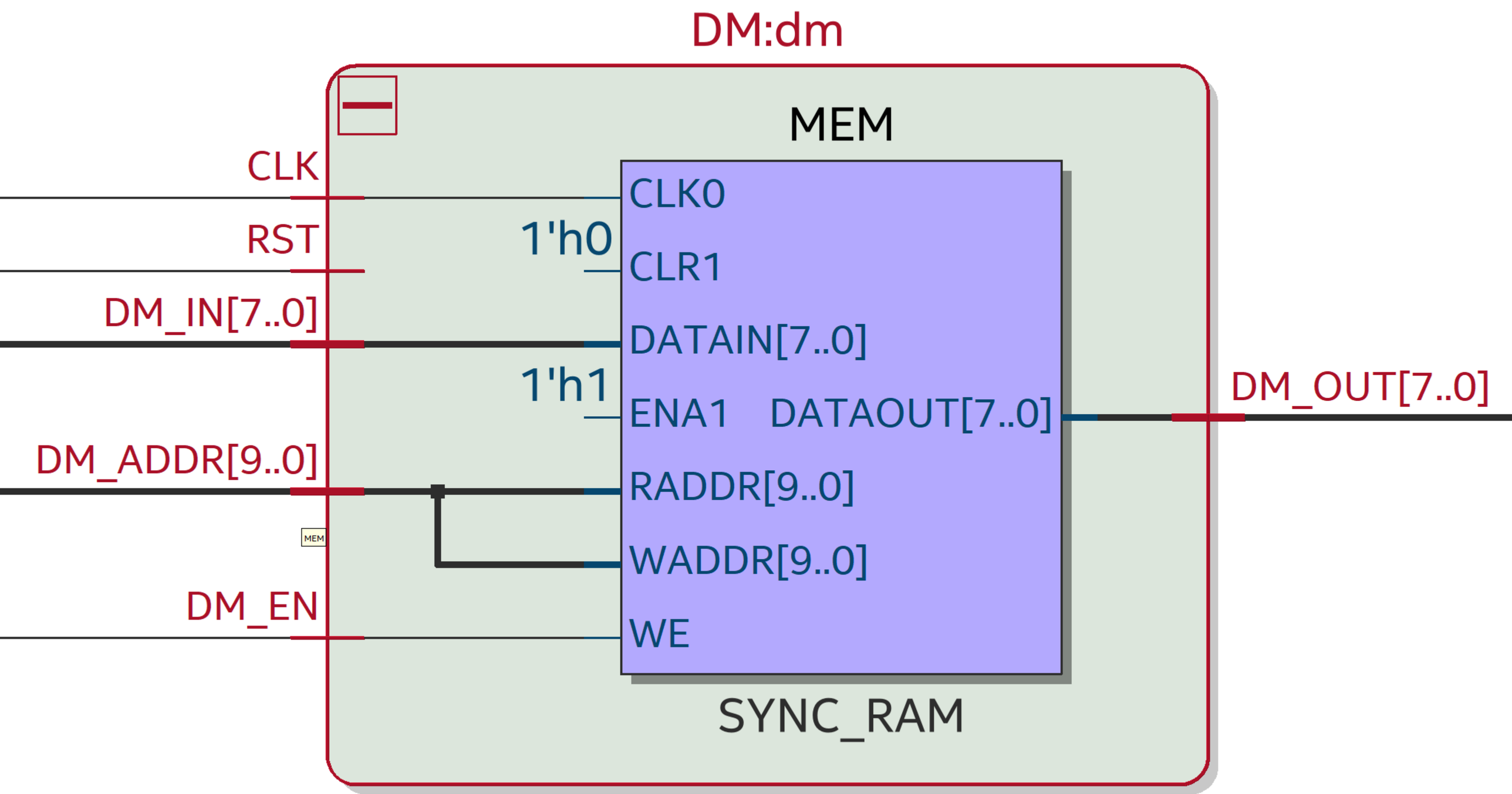
Registers[0][7..0]
Registers[1][7..0]
Registers[2][7..0]
Registers[3][7..0]

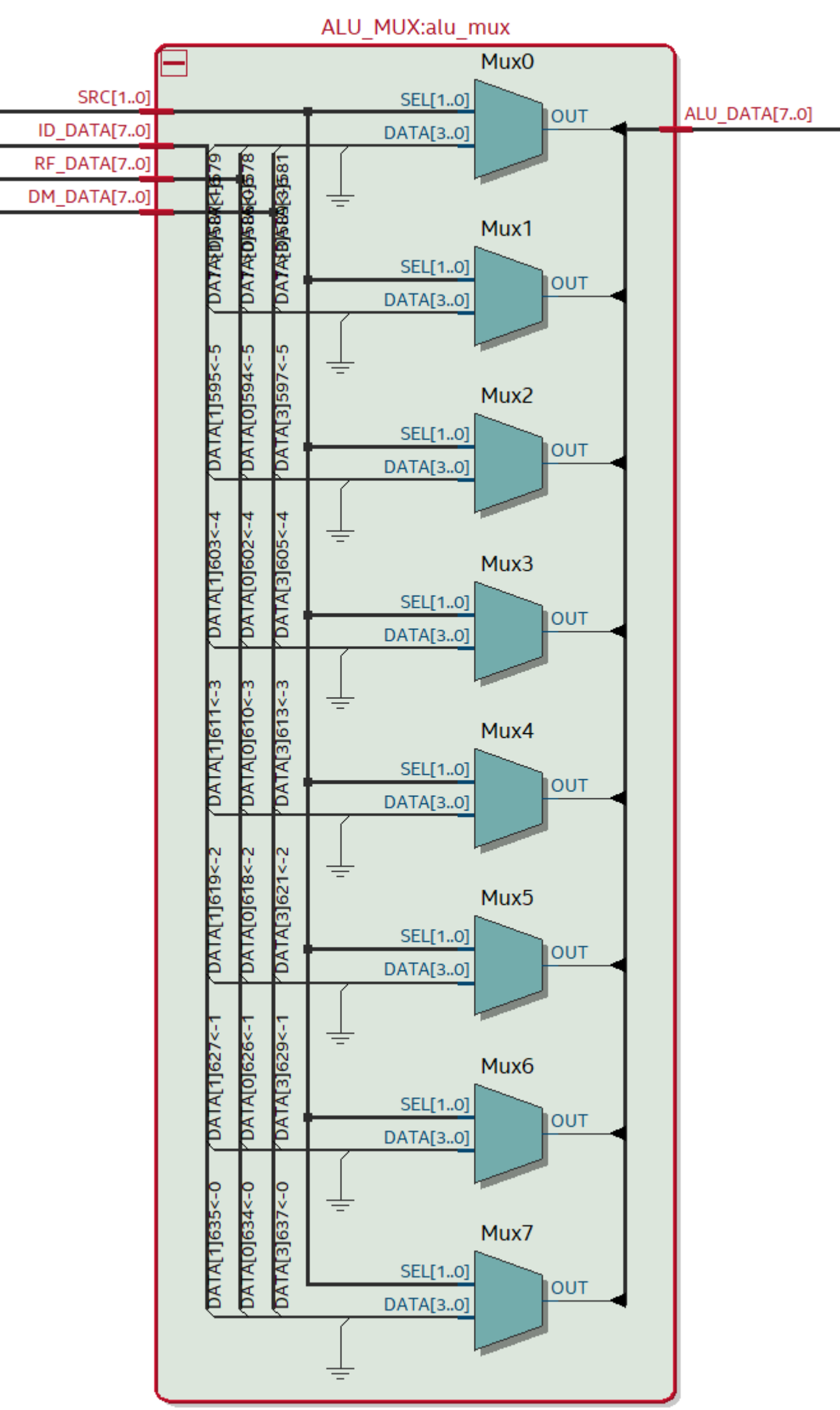
D
CLK
ENA
8'h0
SCLR
CLRN
Q

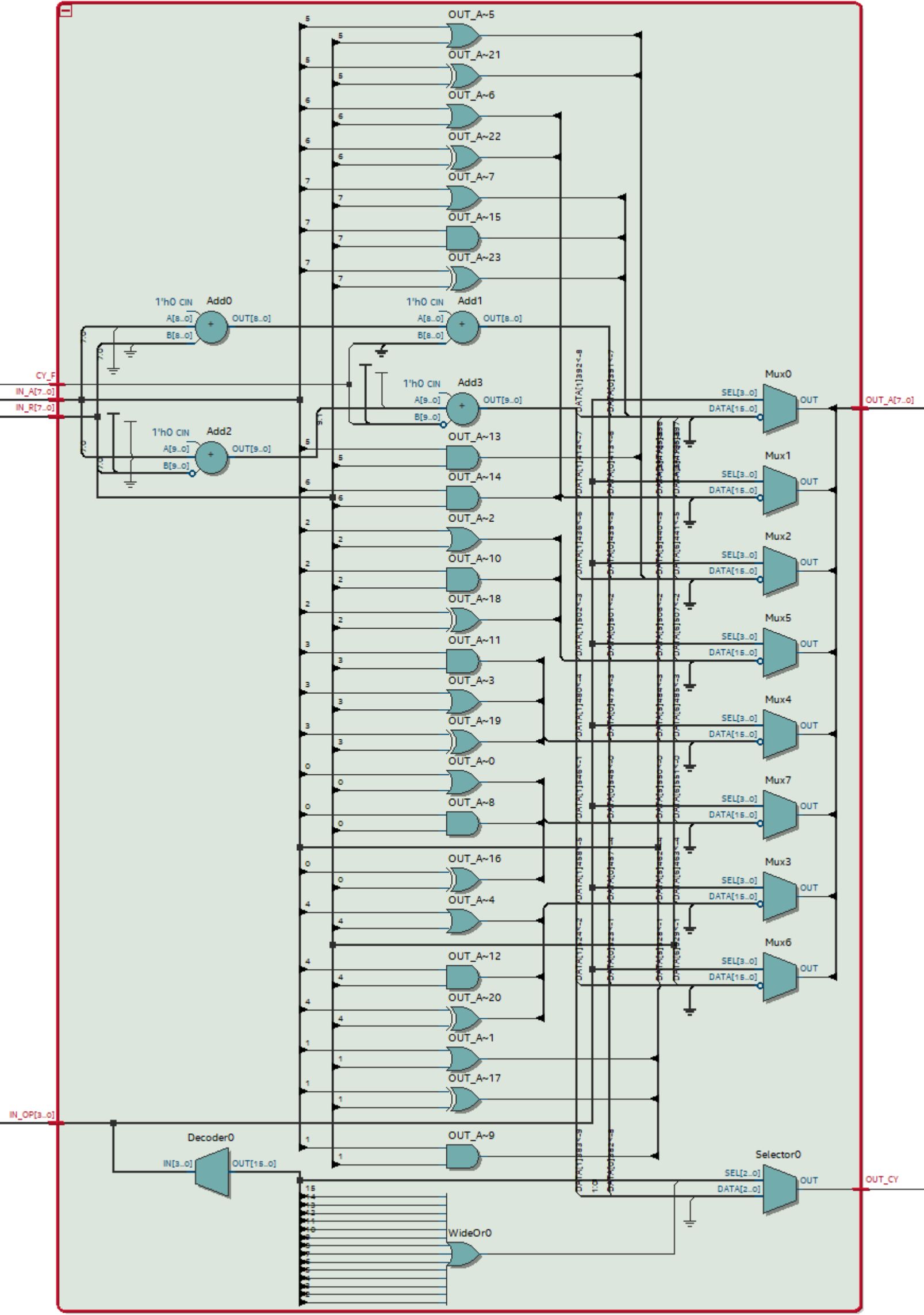
Mux0
Mux1
Mux2
Mux3
Mux4
Mux7
Mux6
Mux5

SEL[1..0]
DATA[3..0]
OUT

RF_OUT[7..0]


DM:dm
MEM
CLK
RST
DM_IN[7..0]
DM_ADDR[9..0]
DM_EN
1'h0
1'h1
CLK0
CLR1
DATAIN[7..0]
ENA1
DATAOUT[7..0]
RADDR[9..0]
WADDR[9..0]
WE
DM_OUT[7..0]
SYNC_RAM


ALU_MUX:alu_mux
SRC[1..0]
ID_DATA[7..0]
RF_DATA[7..0]
DM_DATA[7..0]
ALU_DATA[7..0]
Mux0
Mux1
Mux2
Mux3
Mux4
Mux5
Mux6
Mux7
SEL[1..0]
DATA[3..0]
OUT
DATA[1]595<-5
DATA[0]594<-5
DATA[3]597<-5
DATA[1]603<-4
DATA[0]602<-4
DATA[3]605<-4
DATA[1]611<-3
DATA[0]610<-3
DATA[3]613<-3
DATA[1]619<-2
DATA[0]618<-2
DATA[3]621<-2
DATA[1]627<-1
DATA[0]626<-1
DATA[3]629<-1
DATA[1]635<-0
DATA[0]634<-0
DATA[3]637<-0


OUT_A~5
OUT_A~21
OUT_A~6
OUT_A~22
OUT_A~7
OUT_A~15
OUT_A~23
1'h0 CIN
Add0
A[8..0]
B[8..0]
OUT[8..0]
1'h0 CIN
Add1
A[8..0]
B[8..0]
OUT[8..0]
CY_F
IN_A[7..0]
IN_R[7..0]
1'h0 CIN
Add3
A[9..0]
B[9..0]
OUT[9..0]
1'h0 CIN
Add2
A[9..0]
B[9..0]
OUT[9..0]
OUT_A~13
OUT_A~14
OUT_A~2
OUT_A~10
OUT_A~18
OUT_A~11
OUT_A~3
OUT_A~19
OUT_A~0
OUT_A~8
OUT_A~16
OUT_A~4
OUT_A~12
OUT_A~20
OUT_A~1
OUT_A~17
OUT_A~9
Mux0
Mux1
Mux2
Mux5
Mux4
Mux7
Mux3
Mux6
SEL[3..0]
DATA[15..0]
OUT
OUT_A[7..0]
IN_OP[3..0]
Decoder0
IN[3..0]
OUT[15..0]
Selector0
SEL[2..0]
DATA[2..0]
OUT
OUT_CY
WideOr0

Register:acc

OUT[0]~reg[7..0]

IN[7..0]

CLK

EN

RST

D

CLK

ENA

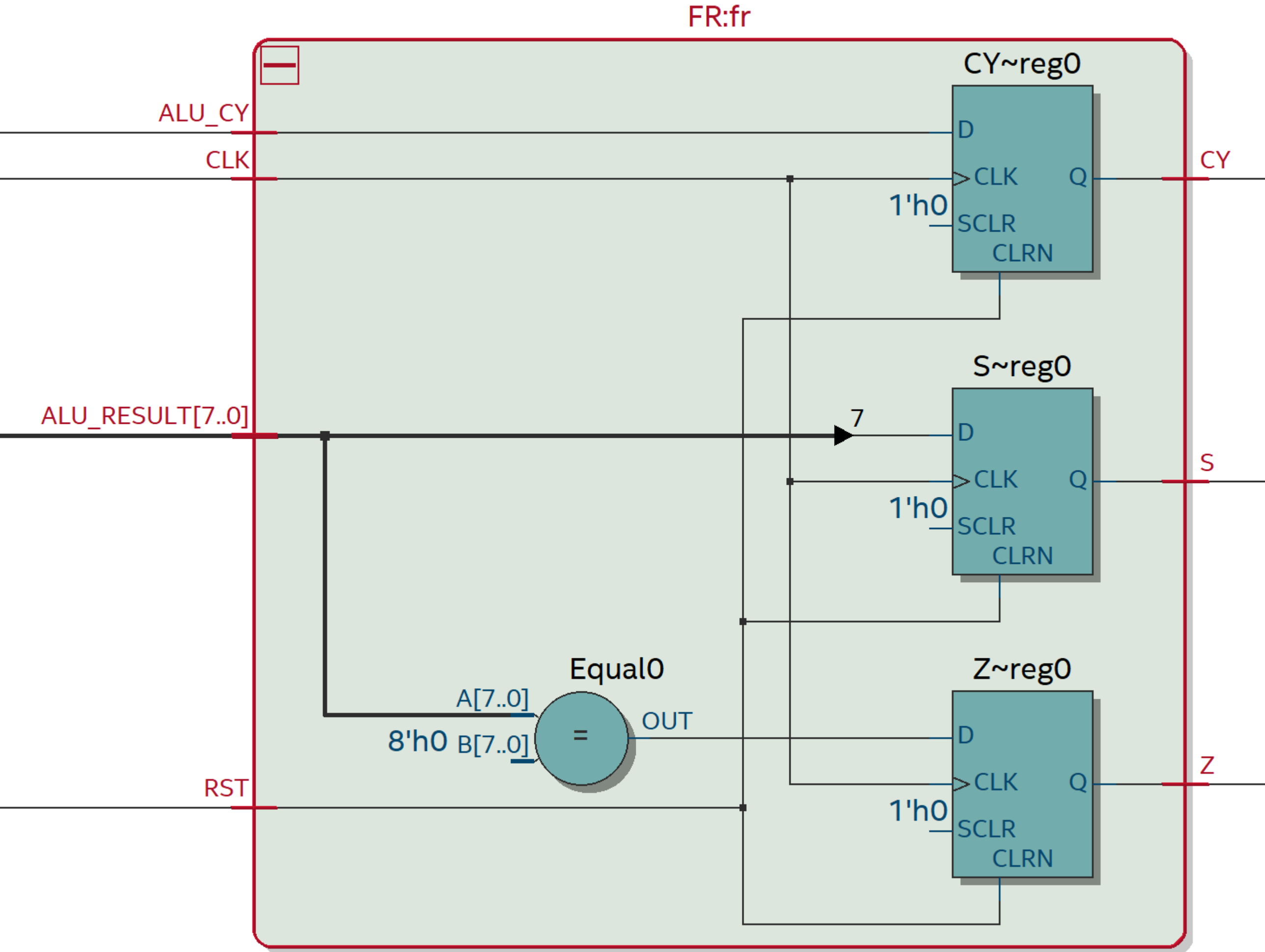
8'h0

SCLR

CLRN

Q

OUT[7..0]


FR:fr
ALU_CY
CLK
ALU_RESULT[7..0]
RST
CY~reg0
D
CLK
Q
1'h0
SCLR
CLRN
CY
S~reg0
7
S
Equal0
A[7..0]
8'h0
B[7..0]
=
OUT
Z~reg0
Z