Static Noise Margin Analysis for Cryo-CMOS SRAM Cell

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***Abstract*—In this work, we analyzed the static noise margin (SNM) of cryo-CMOS SRAM cells operated at superthreshold (Vdd = 0.75 V) and subthreshold (Vdd = 0.2 V) regions. The impact of the temperature and write-assist (WA) technique on the ultra-thin-body (UTB) SOI SRAM cell has been examined. UTB SOI MOSFET at 77K shows a steep subthreshold slope and reduced leakage, which enables the UTB SOI SRAM cell to operate at low Vdd. Our results show that at Vdd = 0.2V, compared to 300K, UTB SOI SRAM with WA at 77K shows 39.6%, 32.2%, and 11% improvements in read, hold, and write SNM, respectively. Therefore, cryo-CMOS SRAM enabling low Vdd operation and improving stability is a highly promising solution to improve both performance and power efficiency.**

Keywords—Cryo-CMOS, cryogenic, SRAM, static noise margin, write-assist technique, subthreshold operation

I. Introduction

As the technology scaling continues, it is getting more challenging to improve the CMOS power performance by reducing the supply voltage (Vdd) and threshold voltage (Vth) without prohibitively increasing its leakage power. Moreover, continued scaling of the metal interconnection geometry increases wire resistance which degrades the circuit performance in advanced technology nodes [1]. Cryo-CMOS has emerged as a highly promising solution to improve performance and power efficiency by operating the devices at ultra-low temperatures [2-5]. The low-temperature operation of CMOS shows the advantages of increased carrier mobility, decreased leakage, and steep subthreshold slope. At the circuit and system level, the low-temperature operation reduces the wire resistance and decreases unwanted energy dissipation [6]. SRAM is the most common embedded memory for CMOS ICs and represents a large portion of the chip. However, SRAM operated at ultra-low temperature has rarely been examined. In this work, we analyzed the static noise margin of ultra-thin-body (UTB) SOI SRAM cells at temperatures varying from 300K to 77K. The impact of Vdd and cell supply lowering write-assist technique (Vcs lowering) on the UTB SOI SRAM cell has also been investigated. Our results show that cryo-CMOS SRAM with write-assist (WA) operated at subthreshold region exhibits superior static noise margin compared to the SRAM worked at 300K.

II. Device Design and Simulation Framework

Fig. 1 shows the schematic of UTB SOI MOSFET. The device parameters are listed below: gate length (Lg) = 20 nm, channel thickness (Tch) = 3 nm, EOT = 0.7 nm, buried oxide thickness (TBOX) = 10 nm, and ground-plane substrate doping = 1E20 cm-3. The temperature-dependent mobility and band-gap model parameters are calibrated with experimental data at 300K and 77K [4]. Fig. 2(a) shows that the Id-Vg characteristics of UTB SOI MOSFETs at 300 K, 220K, 150 K, and 77K are designed to have the same threshold voltage at Vds = 0.2V. As temperature decreases from 300K to 77K, the subthreshold swing (SS) changes from 75 mV/dec to 22 mV/dec. As can be seen, low-temperature CMOS reduces its SS and leakage current dramatically compared to room temperature CMOS. Fig. 3 shows the schematic of a 6T SRAM cell and the definitions of read and write SNM (RSNM and WSNM). The stability of UTB SOI SRAM cells is analyzed using TCAD mixed-mode simulations [7].

III. Analysis of Static Noise Margin

Fig. 4(a) shows the impact of temperature on RSNM for UTB SOI SRAM operated at superthreshold (Vdd = 0.75 V) and subthreshold (Vdd = 0.2 V) regions. As temperature decreases from 300 K to 77 K, UTB SOI SRAM cell shows 39.6% improvements in RSNM at Vdd = 0.2 V. This is because, at Vdd = 0.2 V, the UTB SOI SRAM entirely operated in the subthreshold region as shown in Fig. 4(b). Therefore, UTB SOI MOSFET with steep SS at 77K will show a steeper transition of data storage voltage (Vsl, Vsr) from high to low. Besides, the read '0' disturb voltage is also lowered at 77K due to its steep SS [8]. Therefore, cryo-CMOS SRAM at 77K improves RSNM at Vdd = 0.2V. At Vdd = 0.75V, UTB SOI SRAM at 77K slightly increases the read '0' disturb compared to 300K in Fig. 4(c), thus reducing RSNM by 11.5%. Hold SNM (HSNM) shows similar characteristics with RSNM. The cryo-CMOS SRAM (77K) at Vdd = 0.2 V shows a steep transition of data storage nodes (Vsl and Vsr) which increases the HSNM by 32.3% compared to 300K. At Vdd = 0.75 V, UTB SOI SRAM at 77K shows slight reduction (-6.2%) in HSNM compared to 300K. Fig. 6 shows the impact of temperature on WSNM for UTB SOI SRAM without the write-assist (w/o WA) technique. It can be seen that the WSNM becomes worse as temperature reduces at both Vdd = 0.75 V and 0.2 V. This is because, for writing '0' in the data storage nodes (Vsl, Vsr), pull-up (PU) PFET is operated in the linear region, and becomes stronger at 77K compared to 300K. Therefore, UTB SOI SRAM w/o WA at 77K shows worse WSNM compared to that at 300K. Fig. 7 shows the WSNM of UTB SOI SRAM considering the cell supply (Vcs) lowering WA at Vdd = 0.75 V and 0.2 V. It can be seen that the WA technique is much efficient to improve the WSNM at Vdd = 0.2V than that at Vdd = 0.75 V. This is because, at Vdd = 0.2 V, the cryo-CMOS SRAM (77K) is entirely operated in the subthreshold region. At Vdd = 0.2 V, using Vcs lowering WA will exponentially reduce the strength of PU devices, and thus improving the WSNM by 11% as temperature reduces from 300K to 77K.

In summary, cryo-CMOS SRAM cell with WA shows superior read, hold and write SNM at Vdd = 0.2V, making cryo-CMOS SRAM a promising solution to improve both performance and power efficiency.

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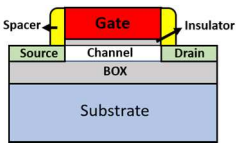

Fig. 1. Ultra-thin-body (UTB) SOI structure with gate length (L_g) = 20 nm, channel thickness (T_{ch}) = 3nm, and EOT = 0.7 nm.

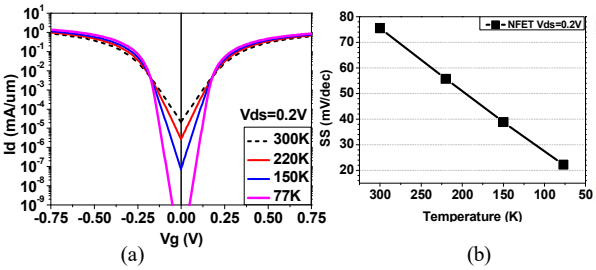

Fig. 2. (a) Id-Vg curves with different temperatures at V_{ds} = 0.2 V. (b) Subthreshold swing (SS) of NFET at 300 K, 220 K, 150 K and 77 K.

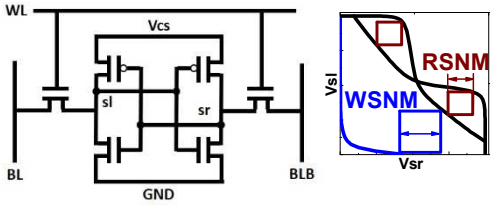

Fig. 3. (a) Schematic of 6T SRAM cell. Vcs lowering write-assist technique is considered in this work to improve the write-ability. (b) The definitions of read static noise margin (RSNM) and write static noise margin (WSNM).

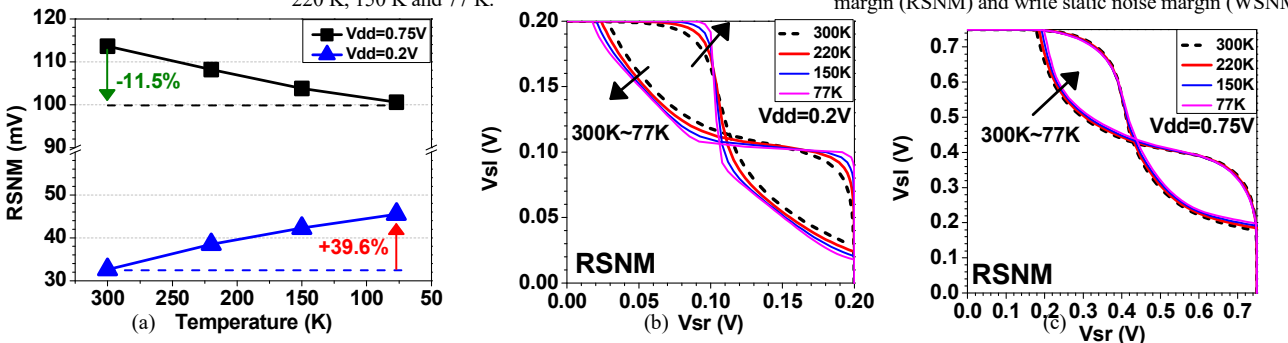

Fig. 4. (a) Impact of temperature on RSNM at Vdd = 0.75V and 0.2V, respectively. As temperature reduces, the RSNM degrades at Vdd = 0.75V and improves at Vdd = 0.2V. RSNM butterfly curves with different temperatures at (b) Vdd = 0.2V and (c) Vdd = 0.75V, respectively.

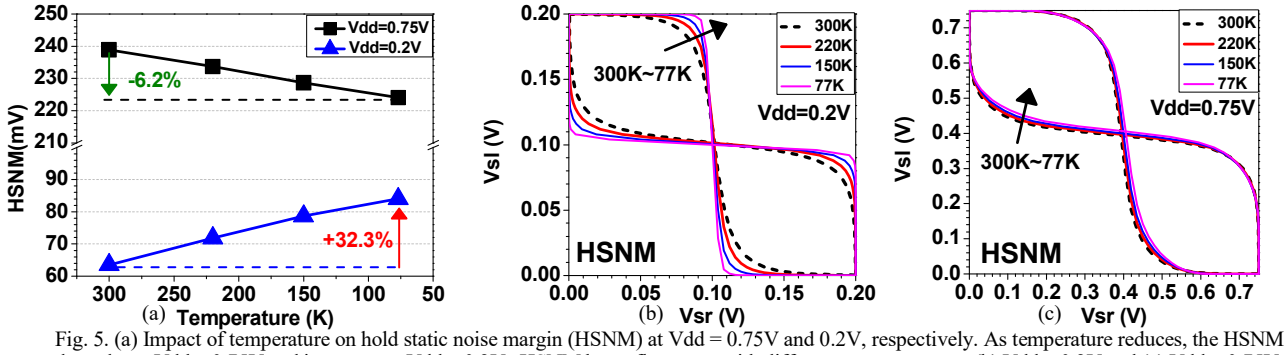

Fig. 5. (a) Impact of temperature on hold static noise margin (HSNM) at Vdd = 0.75V and 0.2V, respectively. As temperature reduces, the HSNM degrades at Vdd = 0.75V and improves at Vdd = 0.2V. HSNM butterfly curves with different temperatures at (b) Vdd = 0.2V and (c) Vdd = 0.75V, respectively.

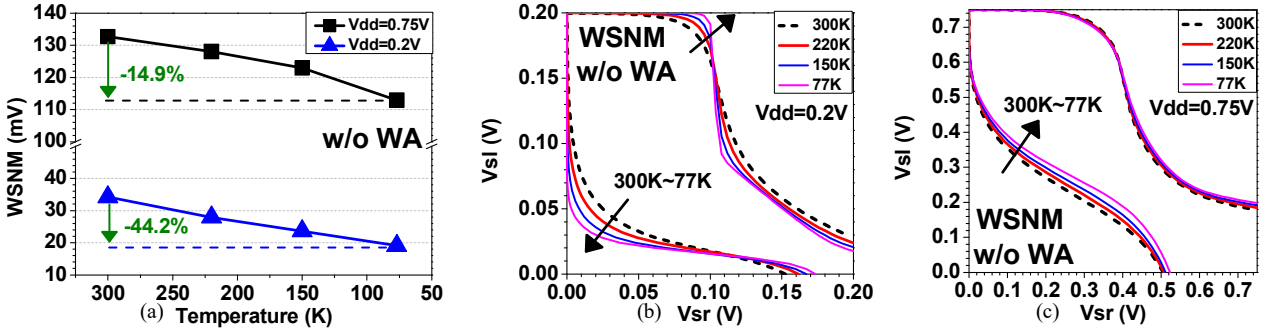

Fig. 6. (a) WSNM vs. temperature for SRAM cell without write-assist circuit (w/o WA). As temperature reduces, the WSNM w/o WA degrades at both Vdd = 0.75V and Vdd = 0.2V. WSNM butterfly curves w/o WA with different temperatures at (b) Vdd = 0.2V and (c) Vdd = 0.75V.

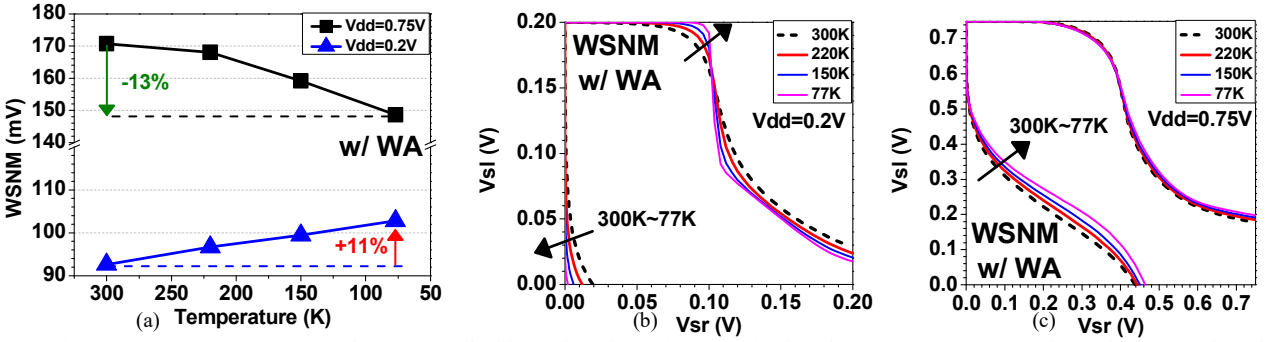

Fig. 7. (a) WSNM vs. temperature for SRAM cell with Vcs lowering write-assist circuit (w/ WA). As temperature reduces, the WSNM degrades at Vdd = 0.75V even considering Vcs lowering WA technique (ΔVcs = -50 mV). However, for SRAM with Vcs lowering WA at Vdd = 0.2V, WSNM increases by 11% as temperature reduces from 300K to 77K. WSNM butterfly curves w/ WA with different temperatures at (b) Vdd = 0.2V and (c) Vdd = 0.75V.