Toward 7 Bits per Cell: Synergistic Improvement of 3D Flash Memory by Combination of Single-crystal Channel and Cryogenic Operation.

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***Abstract*— In this paper, it is shown that the combination of single-crystal channel and cryogenic operation at 77 K using liquid nitrogen improves the cell transistor characteristics and the storage performance of 3D Flash memory. Compared to the cryogenic operation with poly-Si channels, that we have already reported, the cryogenic operation with single-crystal channels results in a steepening of the cell transistor subthreshold slope and reduced read noise. In particular, read noise is significantly suppressed to one-third due to the synergistic effect of the improvement by single-crystal and the cryogenic operation, compared with poly-Si channel in room temperature. Furthermore, data retention is improved at cryogenic temperature compared to room temperature. These improvements lead to a narrower Vth distribution of the cell, which enables bit-cost scaling through a multi-level cell. An ultra-multi-level cell of 7 bits per cell is successfully demonstrated for the first time, and its feasibleness in future storage products is shown.**

Keywords—3D Flash Memory, Single-crystal Channel, Cryogenic, Liquid Nitrogen, 7 Bits per Cell

I. INTRODUCTION

Digital data generated in the world is rapidly increasing. In 2025, the global datasphere, i.e., the total generated data amount, will grow to 175 ZB [1]. HDD and SSD are widely used as storage devices for large data, and SSD is replacing HDD because it is superior in terms of read and write speeds and power consumption. The replacement of HDD with SSD is driven by continuous bit cost scaling of the Flash memory. Although bit cost scaling of the 3D Flash memory is achieved by bit density increase utilizing highly stacked word line (WL), it is difficult to keep the same manner because of the increase of manufacturing cost. Therefore, there is a need for an alternative method without increasing the process steps and manufacturing cost.

In general, semiconductor devices including 3D Flash memory operate at a temperature range from −40 to 125 °C. On the other hand, there are some reports of semiconductor device operation at cryogenic temperature, and their cryogenic operation can improve the device performance. Liquid cooling of computers has already been used in data centers. Cryogenic cooling with liquid nitrogen is widely used in quantum computers and several industries such as superconducting power transmission and magnetically levitated trains. Liquid nitrogen has already been mass produced by air freezing, so it is sustainable and inexpensive. Therefore, cryogenic operation using liquid nitrogen is applicable even in general data centers in the future, when the benefits of performance improvement are worth more than the additional cooling cost.

For CMOS logic device, improvements in the trade-off between the switching speed and power consumption of state-of-the-art FinFET devices at cryogenic temperature of 77 K were reported [2]. For DRAM, the data retention characteristics, one of the most important memory performance factors, are significantly improved at 77 K [3]. The read and write latency, power consumption and refresh operation are also improved; thus, cryogenic operation is able to boost the DRAM performance [4].

For 3D Flash memory, cryogenic operation can improve the storage performance and scale the bit cost. It was reported that cryogenic operation of 3D Flash memory is possible and has the potential for an ultra-multi-level cell of 6 bits per cell with suppressed read noise together with improved data retention and endurance characteristics, and these evaluations were performed with poly-Si channels [5, 6]. To achieve ultra-multi-level cell beyond 6 bits per cell it requires a much tighter cell Vth distribution. It is well known that applying a single-crystal Si to the channels instead of defect-rich poly-Si is effective to tighten the cell Vth distribution [7]. A single-crystal channel fabricated by metal induced lateral crystallization (MILC) [8] and combination with annealing [9] were also reported.

In this work, a 3D Flash memory with a single-crystal Si channel is fabricated, and evaluated under the cryogenic temperature. We observe the synergistic improvements in the read noise characteristics. Moreover, we demonstrate 7 bits multi-level cell successfully that is clearly indicating it is highly feasible for the future storage devices.

II. DEVICE SETUPS

A 3D Flash memory with the channel filled with single-crystal Si by epitaxial growth from a silicon substrate was fabricated. In this chip, the entire channel is filled with silicon (full channel structure). It was compared with the macaroni-channel structure as a reference, in which only the bottom side of the channel is filled with single-crystal Si and the top side has a thin poly-Si. Fig. 1 shows the illustration of the device structures of the channel areas and their TEM images. The tunnel oxide layer, charge trap (CT) layer, block layer and WL metal are the same in these devices.

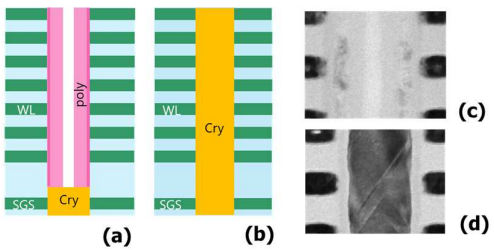

Fig. 1 Device structures and TEM pictures of (a and c) the macaroni channel with poly-Si and (b and d) the full channel with single-crystal Si by epitaxial growth from a silicon substrate.

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The device characteristics were measured at room temperature (300 K) and cryogenic temperature (77 K) using liquid nitrogen, which is the same as in our previous experiment [5].

III. Cell Transistor Characteristics

The cell transistor characteristics of the single-crystal Si and the poly-Si channels are compared. Fig. 2 shows the I-V curves at 77 K and Fig. 3 shows the cell transistor subthreshold slope (SS) at 300 and 77 K. The single-crystal channel has a steeper SS than the poly-Si channel. The SS of both the single-crystal and poly-Si channels are improved when operated at 77 K. The improvement of SS increases the actual read current because the overdrive of read voltage to the selected WL is limited [5]. When the read current is increased, it is expected improved signal-noise ratio and suppressed read noise. In addition, this is also effective in reducing read time. In ultra-multi-level cell such as 6 bits per cell or more, read time has more impact for the storage performance because a large number of read operations are required to determine the value in memory cell. Therefore, steeper SS is effective for ultra-multi-level cell in terms of suppressing read noise to narrow the Vth distribution, and reducing the read time to shorten the total operation time.

These evaluations were performed with different channel structures: a full channel of single-crystal Si and a macaroni channel of thin poly-Si. It is known that the macaroni-channel structure improves the SS compared to the full channel structure [10]. Therefore, further improvement of SS is expected when the cells with macaroni-channel structure using single-crystal Si as the channel material are operated at 77 K.

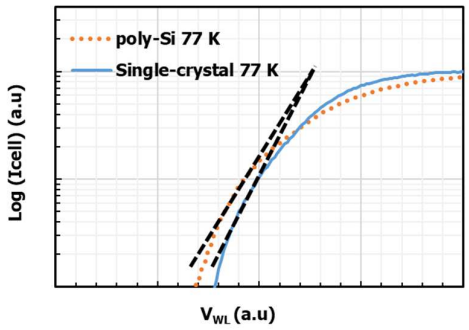

Fig. 2 Logarithmic plot of the *I–V* curves of the cell transistor of the single-crystal and poly-Si channels at 77 K. The single-crystal channel cell shows steeper SS.

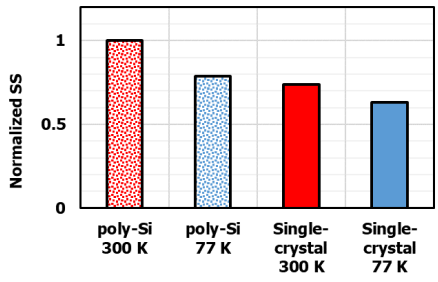

Fig. 3 Comparison of the SS at 300 and 77 K of the single-crystal and poly-Si channels. The single-crystal channel cell at 77 K shows the steepest SS.

IV. ISPP and ISPE Characteristics

Incremental step pulse programming (ISPP) is a method of programming 3D Flash memory from an erase state to a target Vth value by repeatedly increasing the programming voltage. This method is used to obtain a narrow Vth distribution to achieve a multi-level cell. Fig. 4 shows the ISPP characteristics of the single-crystal and the poly-Si channels at 300 and 77 K. The cell Vth at the same program voltage of the single-crystal channel is smaller than that of the poly-Si channel. Therefore, it is necessary to increase the programming voltage for the single-crystal channel. This is because the neutral Vth changes due to the difference in the channel material and structure (see Fig. 1), and thus different flat band voltage. The ISPP slopes are almost the same between the single-crystal and the poly-Si channels. There is no significant difference in the ISPP characteristics between the different temperatures of 300 and 77 K for both the single-crystal and the poly-Si channels, indicating that program operation is applicable for single-crystal channel at 77 K by adjusting programming voltage.

Fig. 5 shows the device characteristics of the erase operation by incremental step pulse erase (ISPE). The erase voltage of the single-crystal channel is smaller than that of the poly-Si channel due to lower neutral Vth. Therefore, the single-crystal channel can be erased with a smaller erase voltage. The erase voltages of both the single-crystal and the poly-Si channels shift to higher values at 77 K. This indicates that carrier excitation mechanisms, such as the Poole-Frenkel effect, affect the erase operation, which has already been reported for the poly-Si channel [6], and the similar characteristics is observed for the single-crystal channel. The shift is smaller in the single-crystal channel than in the poly-Si channel. Erase operation is also applicable for single-crystal channel at 77 K by adjusting erase voltage.

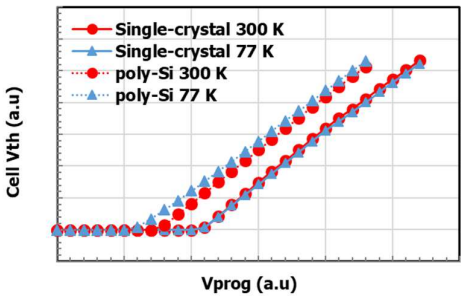

Fig. 4 ISPP characteristics of the single-crystal and poly-Si channels at 300 and 77 K. There was no significant difference between the different temperatures of 300 and 77 K for both the single-crystal and the poly-Si channels.

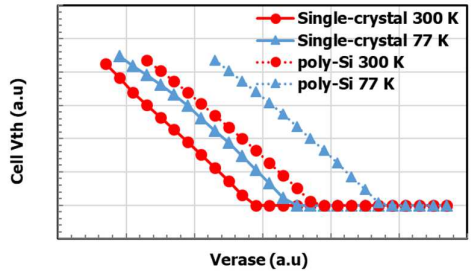

Fig. 5 ISPE characteristics of the single-crystal and poly-Si channels at 300 and 77 K. The erase voltages of both the single-crystal and the poly-Si channels shift to higher values at 77 K.

V. Read Noise Characteristics

To achieve an ultra-multi-level cell of 3D Flash memory, narrowing the Vth distribution of cells is strongly required. There are three major factors that determine the Vth distribution of cells: read noise, cell endurance and data retention. Read noise indicates the Vth difference when a cell is repeatedly read. The distribution of the Vth difference of 16 kiB cells is shown in Fig. 6. The read noise in the single-crystal and poly-Si channels are suppressed at 77 K, which is the same as in our previous report [5]. In addition, at the same temperature, the single-crystal channel shows better read noise characteristics than poly-Si channel. Along with the effect of the SS improvement, it can also be explained that its grain boundary less channel structure suppresses to form percolation path which causes Vth difference [11].

Fig. 7 shows the comparison of the read noise normalized by the poly-Si channel at room temperature. Read noise is suppressed by changing the operating temperature from 300 to 77 K. It is also improved by changing the channel from poly-Si to single-crystal Si. When the single-crystal channel is operated at 77 K, the smallest read noise is obtained, which is about one-third of the reference. This improvement is more than multiply of each method: single-crystal channel at 300 K and poly-Si channel at 77 K. Therefore, applying a single-crystal channel to 3D Flash memory with cryogenic operation can synergistically improve the read noise characteristics.

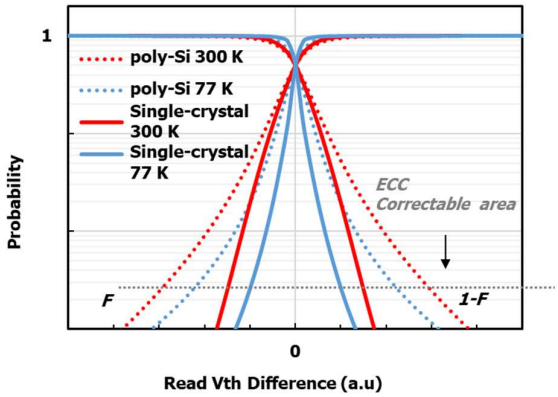

Fig. 6 Comparison of the read Vth differences for 16 kiB cells of the single-crystal and poly-Si channels at 300 and 77 K. The read noise characteristics in the single-crystal and poly-Si channels are suppressed at 77 K.

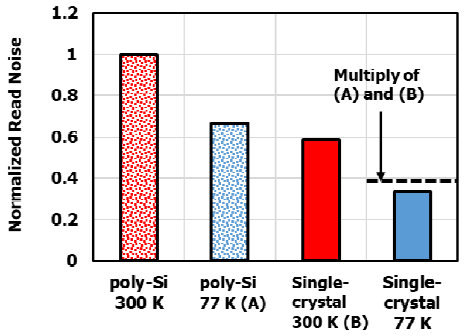

Fig. 7 Read noise characteristics normalized by the poly-Si channel at 300 K. The single-crystal channel at 77 K obtains synergistic improvement of read noise characteristics, compared with multiply of each method: single-crystal channel at 300 K and poly-Si channel at 77 K.

VI. Data Retention Characteristics

The data retention characteristics of the 3D Flash memory improve in cryogenic operation because the thermal excitation in the CT decreases at low temperatures, resulting in a decrease in charge loss. Regardless of the channel material, this improvement at cryogenic operation is effective in single-crystal channel as well as poly-Si channel. Fig. 8 shows the average cell Vth shifts after each retention time. The cells are initially programmed at a high Vth level. The improvement of the data retention characteristics at cryogenic operation is suppressed to one-third at room temperature, and there is not much difference between the single-crystal and the poly-Si channels. Fig. 9 shows the variation of the cell Vth shifts due to data retention for the single-crystal and poly-Si channels at 77 K. Including the variation of cell Vth decrease, the data retention characteristics of the single-crystal channel at 77 K has no difference compared with the poly-Si channel.

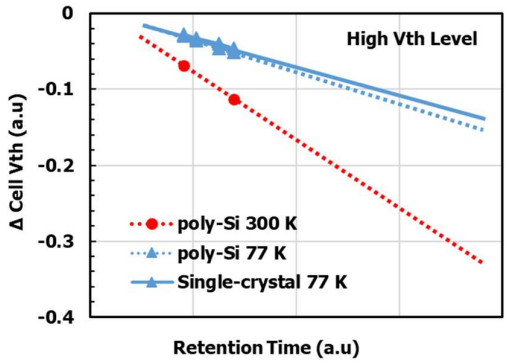

Fig. 8 Data retention characteristics of the single-crystal and poly-Si channels at 300 and 77 K. The shift of the cell Vth due to charge loss becomes small at 77 K. There is not much difference between the single-crystal and the poly-Si channels.

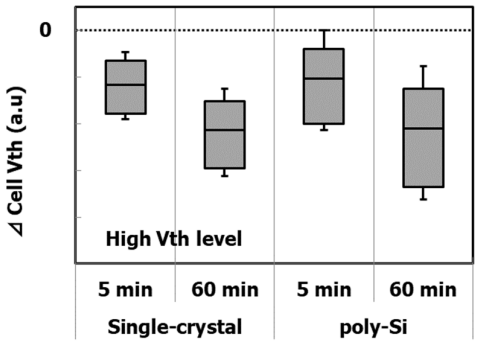

Fig. 9 Variation of the cell Vth decrease due to data retention for the single-crystal and poly-Si channels at 77 K. The data retention characteristics of the single-crystal channel at 77 K has no difference compared with the poly-Si channel.

VII. 7 Bits per Cell Demonstoration

Cryogenic operation of 3D Flash memory with ultra-multi-level cell of 6 bits per cell has been previously demonstrated [6]. When a 3D Flash memory with single-crystal channel is operated at cryogenic temperature, the cell transistor characteristics and storage performances are further improved.

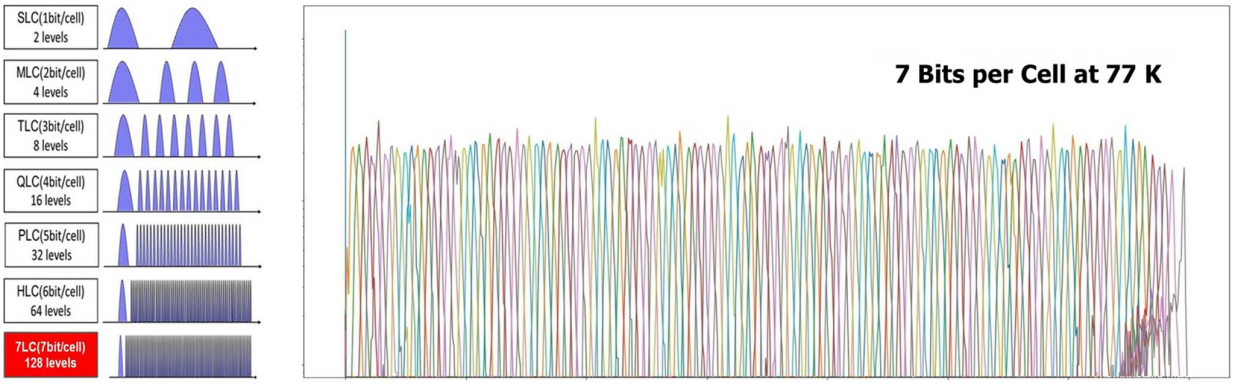

Fig. 10 The demonstration of the Vth distribution of 7 bits per cell with the single-crystal channel at 77 K. It clearly indicates that the 128 Vth distributions required for 7 bits per cell are successfully programmed and read. Observed failure bit rate is less than ECC correctable range based on our estimation.

Fig. 10 shows the demonstration of the Vth distribution of 7 bits per cell with the single-crystal channel at 77 K. It clearly indicates that the 128 Vth distributions required for 7 bits per cell are successfully programmed and read. It also shows further narrower Vth distribution than that of our previous report for 6 bits per cell [6]. Observed failure bit rate is less than ECC correctable range based on our estimation.

Multi-level cell operation of 3D Flash memory contributes to bit cost scaling. Cryogenic operation using liquid nitrogen requires to consider the cooling cost with power consumption. In our estimation, the cooling cost is less than 10% of the chip fabrication cost, [6]. Compared to 4bits per cell (QLC) in 300 K, 7 bits per cell in 77 K reduces the bit cost to x0.64.

VIII. Conclusion

We evaluated the 3D Flash memory with single-crystal channel combined with cryogenic operation at 77 K using liquid nitrogen. The improvements of cell transistor characteristics and storage performance with poly-Si and single-crystal Si channels at 77 K, compared with poly-Si channel at 300 K as reference, are summarized in Table 1. Single-crystal channel operated at 77 K brings significant improvement for the cell transistor SS, synergistic improvement of the read noise characteristics, and long data retention. We took advantage of these characteristics to narrowing Vth distribution and successfully demonstrated 7 bits per cell. It strongly indicates the feasibleness to the bit cost scaling of 3D Flash memory through a multi-level cell for future storage products.

Characteristics	poly-Si Channel at 77 K	Single-crystal Channel at 77 K (this work)
ISPP	Same	Shift ~+2V
ISPE	Shift ~+2V	Shift ~-1V
Subthreshold Slope (SS)	Steeper ~x0.75	Steeper ~x0.6
Read Noise	Suppressed ~x0.65	Suppressed ~x0.33
Data Retention	Longer ~x3	Longer ~x3
Demonstration	6 Bits per Cell [6]	7 Bits per Cell

Table. 1 Summary of the characteristics of 3D Flash memory with poly-Si and single-crystal channels at 77 K compared with poly-Si channel at 300 K as reference. SS and read noise characteristics are synergistically improve at 77 K with single-crystal channel.

Acknowledgment

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