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Modeling and Benchmarking 5nm Ferroelectric FinFET from Room Temperature down to Cryogenic Temperatures

Shivendra Singh Parihar[1,2,*], Swetaki Chatterjee[1,2,*], Girish Pahwa[3],
Yogesh Singh Chauhan[2], and Hussam Amrouch[1,4,5]

[1]Semiconductor Test and Reliability (STAR), University of Stuttgart, Germany
[2]Department of Electrical Engineering, Indian Institute of Technology Kanpur, India
[3]Department of Electrical Engineering & Computer Sciences, University of California, Berkeley, USA
[4]Munich Institute of Robotics and Machine Intelligence, Munich, Germany
[5]AI Processor Design, Technical University of Munich (TUM), Germany
Email: amrouch@tum.de

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***Abstract*—The rise in quantum-computing systems, space electronics, and superconducting processors requires compatible cryogenic memories. The stringent operating conditions for these applications put additional constraints on the endurance and reliable operation of such memories. Ferroelectric-Field Effect Transistors (FeFETs) based on ferroelectric properties of the Hafnium Zirconium Oxide (HZO) can be an excellent choice for these systems. This requires a thorough characterization of FeFET at deep cryogenic temperatures. Also, the scalability of the FeFET to lower technology nodes implies a lower area and reduced leakage. In this work, we, therefore, fully characterize the 5 nm node Fe-FinFET from 10 K to 400 K. To this end, the underlying 5 nm node FinFET transistor is calibrated with experimental data from cryogenic temperatures to above-room temperatures. The material parameters of the Ferroelectric layer are also calibrated with reported measurement data. We propose that the reported endurance improvement of the HZO layer at cryogenic temperatures can improve the reliability of the Fe-FinFET. The observed wake-up and fatigue at higher temperatures are also non-existent at cryogenic temperatures. Although the memory window is reduced at cryogenic temperature compared to room temperature, we can still hold multiple states. This is also verified through our simulations. Lastly, we demonstrate the variability in high and low threshold voltage (V_{TH}) states due to extrinsic variation sources of the underlying transistor and ferroelectric material parameters. We observe a relatively lower variation at cryogenic temperature.**

***Index Terms*—FeFET, Cryogenic, Quantum computing**

I. INTRODUCTION

The recent discovery of ferroelectricity in doped Hafnium-Oxide has sparked renewed interest in ferroelectric devices [1]. This is primarily due to the excellent CMOS process compatibility, low-power read and write operation, and long-term data retention [2]. Different interesting applications, ranging from conventional multi-level-cell (MLC) storage to in-memory-computing for deep neural networks and hyperdimensional computing, have been demonstrated exploiting Ferroelectric Field–Effect Transistor (FeFET) [3]–[7]. However, FeFETs suffer from a few key challenges, limited endurance, wake-up and fatigue for consecutive cycling, and variability. Operation at cryogenic temperature can help us to overcome these challenges and offer better performance [2], [8].

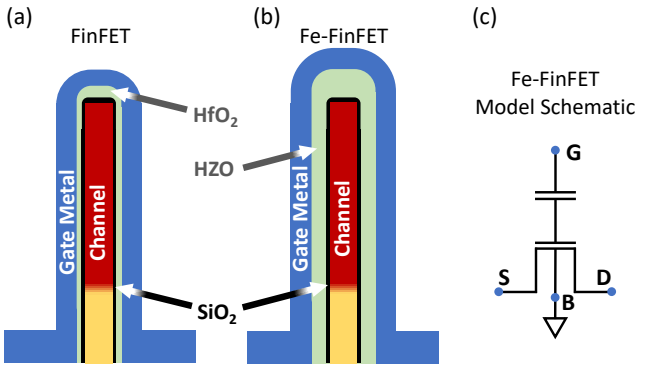

Fig. 1: Cross-sectional representation of the (a) characterized FinFET and (b) simulated Ferroelectric Fin Field–Effect Transistor (Fe–FinFET), a 10 nm ferroelectric (HZO) layer is sandwiched between interfacial layer (SiO_2) and metal gate. (c) Equivalent model schematic for SPICE.

Cryogenic memories have garnered huge interest from industry and academia for applications in quantum computer peripherals, data centers, and space electronics [9]–[11]. The stringent operation conditions for these applications require a fast, precise, and error-free operation. A careful characterization and simulation of such systems are therefore indispensable. The promise of FeFET to perform better at cryogenic temperatures needs to be validated with cryogenic-aware compact models to explore the available design space. This opens new avenues for systems based on FeFET that can operate at cryogenic temperatures and compare it with designs at room temperature.

Characterization of the HZO capacitor has been presented in the literature for a wide temperature range (400 K down to 4 K) [12]. However, the simulations of FeFET for the said temperature range have been limited to 45 nm node Bulk FeFET, which is also not calibrated for cryogenic

*The authors contributed equally to this work.

TABLE I: Impact of Temperature on Ferroelectric Properties at initial, wake-up and fatigue states

Parameter Name	Temperature				
	400 K	358 K	300 K	77 K	10 K
Ferroelectric Thickness (t_{fe}) [nm]	10	10	10	10	10
Coercive Field (E_C) [V/cm]	1.6	1.6	1.6	1.6	1.6
Relative Permittivity (ϵ_r)	28.5	28.04	27.52	26.28	25.25
	Initial State				
Remnant Polarization (P_r) [μC/cm^2]	9.905	9.295	9.650	9.065	8.899
Saturation Polarization (P_s) [μC/cm^2]	22.500	21.870	21.000	16.317	18.000
	Wake-up State				
Remnant Polarization (P_r) [μC/cm^2]	16.360	14.705	13.580	10.020	9.620
Saturation Polarization (P_s) [μC/cm^2]	25.000	23.950	22.500	20.577	20.000
	Fatigue State				
Remnant Polarization (P_r) [μC/cm^2]	11.090	10.555	10.375	10.425	9.970
Saturation Polarization (P_s) [μC/cm^2]	22.500	22.710	23	20.693	20.000

temperatures. It has also been shown that FeFET can offer excellent scalability to lower technology nodes [13]. However, demonstration and simulations have been limited to non-cryogenic calibrated models of the underlying transistor. In this work, we simulate the operations of the 5 nm node Ferroelectric Fin Field–Effect Transistor from cryogenic temperature (10 K) to above room temperature (400 K). This is made possible by an adequately calibrated cryogenic-aware compact model of the underlying transistor for a wide temperature range and a physics-based compact model of the Ferroelectric capacitor (Fe–cap). Our work is divided as follows: Section II details the working of the Fe–FinFET as a memory cell. Section III presents the compact modeling and model calibration methodology of the 5 nm node FinFET and Fe–FinFET down to cryogenic temperatures. The characterization of the Fe–FinFET for the temperature range of 10 K to 400 K is discussed in Section IV, followed by the conclusion of our findings in Section V.

II. Working of Fe-FinFET

The structure of the simulated Fe–FinFET is shown in Fig. 1. This is similar to that of conventional FinFET (Fig. 1(a)), except for the composition of the gate stack, where an extra Zr-doped HfO_2 (HZO) layer is added (Fig. 1(b)). This HZO layer acts as the ferroelectric (FE) layer. The gate stack in Fe–FinFET also has a higher thickness than conventional FinFET. Effective polarization in the FE layer can be changed by the application of an Electric field [2], [14]. The polarization describes the orientation of the permanent electric dipoles, which arises from the non-centrosymmetric arrangement of atoms in the FE material [2]. Depending on the polarization, the underlying channel electron density changes. The channel electron density reduces for the upward polarized domains, and a higher voltage is required to achieve the threshold. Similarly, the channel electron density increases for down-polarised domains and a lower voltage is sufficient to achieve the threshold condition. The difference in the voltages of the two states is termed the memory window (MW) and is the most important metric for characterizing the Fe–FinFET. The FE material parameters, namely, remnant polarization (P_r), saturation polarization (P_s), and coercive field (E_C), play an integral role in determining the characteristics of the Fe–FinFET.

To simulate the Fe–FinFET, we used a Fe–cap in series with the FinFET gate, as shown in Fig. 1(c). While this setup approximates the Fe–FinFET structure, it does not account for the spatial variation of ferroelectric domains or charge trapping at the FE-interfacial layer interface. However, it accurately captures the impact of FE layer material parameters on Fe–FinFET characteristics.

The material parameters change widely depending on the temperature, thus changing the characteristics of the Fe–FinFET. The observed trends on real fabricated ferroelectric capacitors vary widely in the literature depending upon the fabrication method [12], [15], [16]. However, for our work, we have adopted the FE parameters reported in [12], where the P_r increases with an increase in temperature. One possible explanation for this is the higher ferroelectric-dielectric phase ratio of the domains at higher temperatures due to the deposition method of the FE layer. However, there is also a slight increase in the relative permittivity with an increase in temperature. The quality of the fabricated FE layer is better due to plasma-enhanced deposition, and there exists a significant ferroelectric phase from the beginning [17]. Higher temperature facilitates further redistribution of the phases resulting in an effective increase in P_r. The extracted material parameters of the Fe–cap are shown in Table I. Next, we discuss the calibration methodology for the 5 nm node FinFET and the integration of the FE layer to simulate

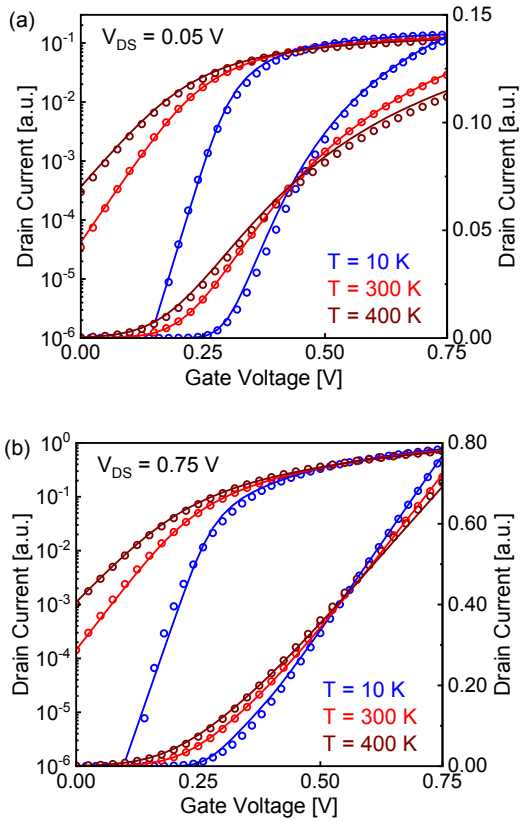

Fig. 2: Transfer characteristics of characterized FinFET for (a) linear (V_{DS} = 0.05 V) and (b) saturation (V_{DS} = 0.75 V) in the temperature range of 10 K to 400 K.

the Fe–FinFET.

III. Cryogenic Modeling and Compact Model Calibration of Fe-FinFET

To develop a Verilog–A–based Fe–FinFET compact model, we have integrated a Fe–cap compact model presented in [18] into the cryogenic aware FinFET compact model [19]–[21]. In this section, firstly, we discuss the cryogenic aware Fe–FinFET model development, and secondly, we briefly discuss the compact model calibration methodology with the help of experimentally measured 5 nm FinFET and the simulated Fe–FinFET for a temperature range of 10 K to 400 K.

A. Cryogenic Aware Fe–FinFET Model Development:

In this work, we have used the Metal-Ferroelectric-Metal-Insulator-Semiconductor (MFMIS) modeling approach to develop the compact model of the Fe–FinFET. The Preisach model (to model the ferroelectric layer), along with the cryogenic aware BSIM–CMG model (for FinFET modeling), is used in our modeling approach to model the switching characteristics of Fe–FinFET accurately for a wide temperature range.

Modeling the Impact of Ferroelectric Layer: To incorporate the impact of field dependence on the ferroelectric domains in the stacked FE layer, we use equations (1) and (2). Firstly, we calculate an auxiliary voltage (V_{aux}) using equation (1), and secondly, we use the extracted V_{aux} to calculate the effective polarization across the FE layer in equation (2). The V_{aux} is formulated with the help of an R-C network, which renders the relaxation time for the dipoles while applying a voltage at the gate terminal of the Fe–FinFET. Once the V_{aux} is determined, the upward or downward polarization of the dipoles is modeled using the tanh function in equation (2). The (-) and (+) signs inside the tanh function mimic the impact of upward and downward polarization, respectively. The slope of the polarization vs. voltage curve is determined by the model parameter 'm', and the parameter 'P_{off}' is used to set the offset polarization.

$$V_{aux} = V_{\mathrm{GS}} - \tau \frac{d}{dt} V_{aux} \tag{1}$$

$$P_{aux} = P_{off} + m \cdot P_s \cdot tanh\left[\frac{1}{2 \cdot E_c} \cdot ln\left(\frac{P_s + P_r}{P_s - P_r}\right) \cdot \left(V_{aux} \pm \frac{E_c}{t_{fe}}\right)\right] \tag{2}$$

Here, P_s, P_r, E_C, τ, and t_{fe} represent saturation polarization, remnant polarization, the coercive field of ferroelectric material, relaxation time for V_{aux}, and the ferroelectric layer thickness, respectively.

Modeling the Impact of Cryogenic Temperatures: The CMOS control circuitry in quantum computers is required to work on cryogenic temperatures for scalable quantum computing. However, the primary obstacle in designing large-scale cryogenic circuits is the unavailability of the cryogenic-aware industry standard compact models for advanced node transistors. In this work, we incorporate the model equations presented in [19], [20] into the industry standard compact model of FinFETs (BSIM–CMG) to model the impact of cryogenic temperatures on 5 nm node FinFET characteristics. Several physical phenomena, such as incomplete ionization, interface trapping, reduced charge carrier scattering, and band-gap widening at cryogenic temperatures, are not observable at room and higher temperatures. These physical effects at lower temperatures result in several benefits in transistor characteristics, i.e., improved mobility, subthreshold swing (SS), saturation velocity, etc. However, these benefits come with a major drawback of higher V_{TH}. An increase in the effective interface trap density and the existence of the band-tail states are the most common explanations proposed in the literature for the saturation of the SS at cryogenic temperatures. In this study, we have utilized the Maxwell–Boltzmann Statistics for charge density calculations. However, to capture the impact of band-tail states, an effective temperature expression shown in equation (3) is utilized in the effective density of states model [19], [20].

$$T_{eff} = \frac{1}{2}\left[T_{sub} + T_0 + \sqrt{(T_{sub} - T_0)^2 + \frac{1}{4}D_0^2}\right] \tag{3}$$

where T_{sub}, T_0, and D_0 represent the substrate temperature, the temperature below which SS saturate and a model parameter for a smooth transition from T_{sub} to T_0, respectively.

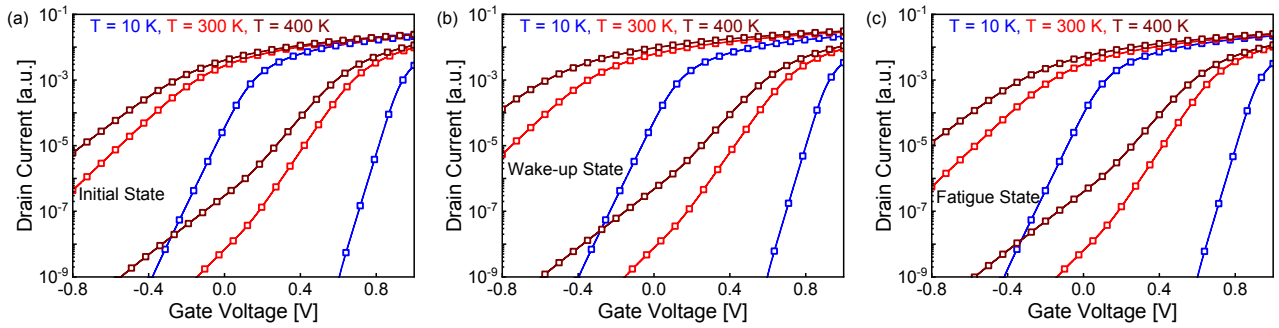

Fig. 3: Transfer characteristics of simulated Fe–FinFET for (a) initial, (b) wake-up, and (c) fatigue states in the temperature range of 10 K to 400 K at V_{DS} = 750 mV.

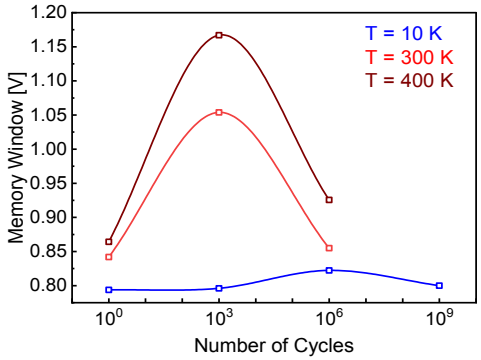

Fig. 4: Endurance characteristics of simulated Fe–FinFET for a write voltage of 3.5 V and V_{DS} = 0.75 V. The MW remains almost constant with no significant wake-up or fatigue at 10 K, whereas at 300 K and 400 K, there is wake-up, and fatigue sets in much earlier.

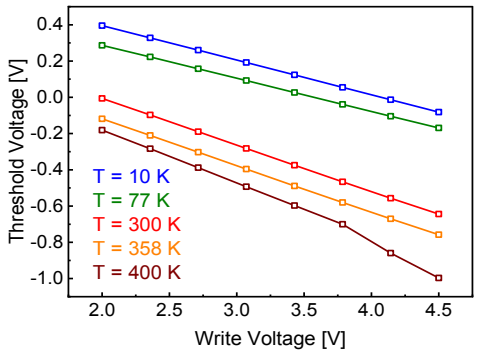

Fig. 5: Threshold voltage modulation using the write voltage (V_{write}) in wake-up state of Fe–FinFET. The V_{write} dependence on net polarization charges results in different threshold voltages for a V_{write} variation in the range of 2 V to 4.5 V.

At cryogenic temperatures, the thermal energy of the charge carriers drops significantly and results in lower over-the-barrier transport from source to drain. Although this reduction in the mobile charge carriers helps to improve the SS at cryogenic temperatures, it also causes an increase in the V_{TH} of transistors. To model the V_{TH} increase, a V_{TH} correction term given in equation (4) is added to the existing threshold voltage model of the BSIM–CMG [19]–[21].

$$\Delta V_{TH} = KT_{11} \cdot \left[\left(1 + exp\left(\frac{T_{sub} - T_{VTH}}{KT_{12}} \right) \right)^{-1} - \left(1 + exp\left(\frac{TNOM - T_{VTH}}{KT_{12}} \right) \right)^{-1} \right] \quad (4)$$

here, KT_{11}, T_{VTH}, KT_{12} are temperature-independent model parameters for V_{TH} correction at cryogenic temperatures, and TNOM represents the nominal temperature.

At cryogenic temperatures, the mobility of mobile charge carriers is significantly affected by Coulomb centers and interface trap charges due to their lower thermal energy. At lower electric fields, Coulomb scattering limits the mobility, while at higher electric fields, surface roughness scattering becomes the limiting factor. Additionally, reduced lattice vibrations at cryogenic temperatures lead to decreased phonon scattering, resulting in higher peak mobility and enhanced current in transistors. To accurately capture the mobility characteristics of charge carriers over a wide temperature range, a modified temperature-dependent mobility model, as presented in [19], [20], is employed. The existing BSIM-CMG model in the literature assumes a linear temperature dependence for the velocity saturation model parameters (VSAT, VSAT1, and MEXP). However, experimental data suggest a non-linear temperature dependence. Hence, the modified velocity saturation model is utilized to account for the temperature-dependent non-linearity in the saturation velocity [19], [20]. This paper outlines a comprehensive model extraction approach for both FinFET and Fe–FinFET devices, covering temperatures ranging from cryogenic to above room temperature.

B. Fe–FinFET Model Calibration:

The model calibration is performed in two stages: firstly, we calibrate the cryogenic aware FinFET compact model with measured characteristics from 10 K to 400 K, and secondly, we calibrate the Fe–cap model to mimic the temperature dependency of the FE layer accurately. The FinFET model calibration starts with setting the correct temperature environment for simulations using the SPICE variable TEMP and model parameter TNOM followed by

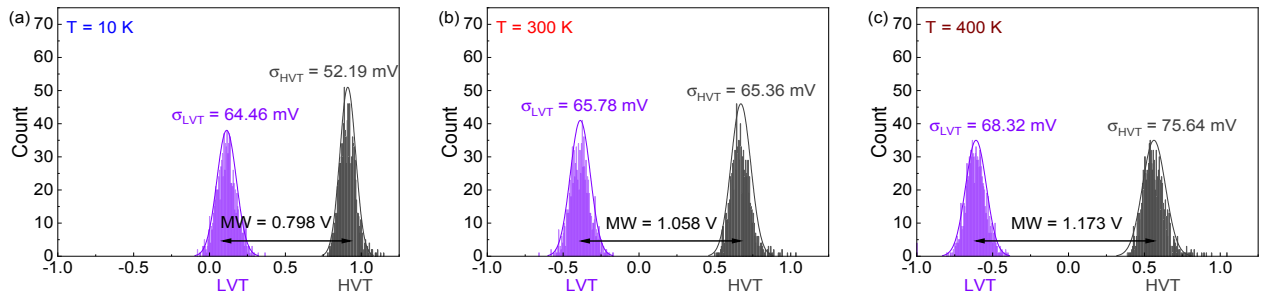

Fig. 6: Impact of process variation on the High V_{TH} (HVT) and Low V_{TH} (LVT) states of the Fe–FinFET for a write voltage (V_{write}) = 3.5 V, read voltage (V_{read}) = 1.5 V, and V_{DS} = 0.75 V.

other model parameter extraction. To do so, we first extract the model parameters at room temperature. Subsequently, the temperature dependence of all the parameters related to various physical effects (e.g., mobility, velocity saturation, channel length modulation, etc.) is extracted. We extract the V_{TH} and SS-related model parameters (PHIG, CIT, CDSC) at room temperature by carefully fitting the transfer characteristics ($I_{DS}-V_{GS}$) of the FinFET in the linear regime of operation (V_{DS} = 0.05 V) (Fig. 2(a)). Parameters related to low-field mobility (U0), mobility degradation (UA, UD, EU, ETAMOB), and series resistance (RSW, RDW, RSWMIN, and RDWNMIN) are extracted from $I_{DS} - V_{GS}$ curves at lower V_{DS} and moderate to strong inversion regimes, respectively. The parameters related to drain-induce-barrier-lowering (DIBL) are extracted from the subthreshold regime of operation by carefully fitting the $I_{DS}-V_{GS}$ and $I_{DS}-V_{DS}$ characteristics at higher V_{DS} (Fig. 2(b)). Model parameters related to velocity saturation (VSAT, VSAT1, MEXP, KSATIV) are extracted in the moderate to strong inversion at higher V_{DS}. Next, we extract the impact of the vertical field on the transconductance degradation using the parameter PTWG by fitting the $I_{DS} - V_{GS}$ curves in strong inversion and saturation regions (V_{DS} = 0.75 V). The channel length modulation parameter PCLM is extracted by carefully minimizing the error between $I_{DS} - V_{GS}$ and $I_{DS} - V_{DS}$ curves at higher V_{DS} and V_{GS}. Once the extracted model accurately predicts the experimentally measured FinFET characteristics, we move to the extraction of temperature-dependent parameters.

In Section III-A, we discussed the significant influence of cryogenic temperatures on the SS and V_{TH}. We capture this temperature impact using various model parameters in the temperature range of 10 K to 400 K. Mobility at above-room temperatures is adjusted using UTE, UTL, UA1, UD1, and EMOBT, while at cryogenic temperatures, UDS, UDD, UDS1, UDD1, UTE1, UA2, EU1, and UD2 are optimized. Series resistance is calibrated by analyzing the $I_{DS}-V_{GS}$ in the linear region at strong inversion for different temperatures, utilizing parameters PRT, PRT1, TR0, and SPRT. DIBL parameters (TETA0) and velocity saturation model parameters (AT, AT2, KSATIV1, KSATIV2, PTWGT, TMEXP, TMEXP2) are extracted from sub-threshold and strong inversion regions of the transfer characteristics, accounting for temperature dependence. Channel length modulation is modeled using parameter PCLMT, considering the slope of the saturation transition region in $I_{DS} - V_{DS}$ at various temperatures and V_{GS}. By accurately incorporating the temperature dependence of both the intrinsic FinFET and the FE layer (described in Table I), our developed cryogenic-aware Fe–FinFET model provides comprehensive characterization.

IV. Characterization of Fe-FinFET

Using the 5 nm calibrated Fe–FinFET, we simulate the transfer characteristics at three different temperatures. Also, to determine the effect of endurance cycling, three different conditions are chosen (a) initial, (b) wake-up, and (c) fatigue. Positive-up and negative-down pulses are applied continuously to test the devices' endurance, and the characteristics are noted. Initial refers to the pristine device before any pulses are applied. At this point, the value of P_r is usually low because few domains are available to switch. After applying a certain number of pulses, more domains are activated, and thus, a maximum peak in the value of P_r is seen. This is referred to as the wake-up stage. Finally, just before the FE layer completely breaks down is called fatigue. The values at different temperatures were taken from [12]. It is seen that at cryogenic temperatures, the value of P_r remains almost constant. This also shows that it can have a higher endurance (up to 10^{10} cycles).

Fig. 3 displays the $I_{DS} - V_{GS}$ characteristics of the Fe–FinFET at different temperatures and stages (initial, wake-up, fatigue). The simulations used a V_{write} of ± 3.5 V and a pulse width of 10 µs. Lower temperatures increase the threshold voltage and improve the subthreshold slope, matching experimental measurements. The MW remains constant, depending on the difference between P_s and P_r. This difference remains constant over a 10 K range. Cryogenic temperatures provide better subthreshold slope and read margin, with a higher current ratio at 4K compared to higher temperatures at V_{read} of 0.4V.

At room temperature and higher, the domains in the FE layer first activate and then deteriorates sooner than at 10 K. Correspondingly, the MW first increases and then decreases, as shown in Fig. 4. However, for the case of 10 K, the MW remains relatively constant for the entire lifetime. This is very advantageous for the operation of the Fe–FinFET. The reported endurance of the Fe–cap is among the highest at cryogenic temperatures [12].

One promising application of the Fe–FinFET is for multi-level-cell storage. This is possible because of the intermediate polarization levels in the FE layer. A variation in the write voltage magnitude or pulse width sets the FE layer into intermediate polarization levels. This sets the Fe–FinFET into intermediate V_{th} values between High-V_{TH} (HVT) and Low-V_{TH} (LVT). Fig. 5 shows the evolution of V_{TH} against the write voltage magnitude. We have selected 8 intermediate states with different write voltages. It is shown that even at $10\,\mathrm{K}$, we can operate with 8 distinct V_{TH} levels. The material parameter values are chosen at the wake-up state. This is to allow the maximum available memory window for higher temperatures. However, due to the degradation with the increasing number of cycles, it will not be possible to hold all the states at higher temperatures significantly. Lastly, we study the impact of process variations on the HVT and LVT states at wake-up for three different temperatures. We consider the measured variations in the V_{TH} of the underlying transistor and also variations in the ferroelectric material parameters. The variations in V_{TH} are given using the model parameter "DELVTRAND" for BSIM-CMG. The ferroelectric material parameters are varied around the mean value by $7.8\,\%$ [22]. The corresponding distribution is shown in Fig. 6. The variability at low temperatures is relatively reduced because of the reduction in switchable polarization values. Also, at cryogenic temperatures, it is generally assumed secondary effects such as charge trapping and domain pinning are significantly reduced.

V. Conclusion

We presented how the $5\,\mathrm{nm}$ node Fe-FinFET behaves for a wide temperature range from $10\,\mathrm{K}$ to $400\,\mathrm{K}$. Using well-calibrated models, we conclude that there is no gain in the memory window while going to cryogenic temperatures. However, the endurance improves while operating at cryogenic temperatures. A relatively-steady operation of the Fe–FinFET for the entire lifetime is observed with no loss in states from the initial state to fatigue. This work forms the basis for future FeFET-based cryogenic systems that can be used for quantum computing and other applications.

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