13.4 A 28nm 360ps-Access-Time Two-Port SRAM with a Time-Sharing Scheme to Circumvent Read Disturbs*

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With the rapid growth in the market for mobile information terminals such as smart phones and tablets, the performance of image processing engines (e.g., operation speed, accuracy in digital images) has improved remarkably. In these processors, 2-port SRAM (2P-SRAM) macros [1], in which a read port and a write port are operated synchronously in a single clock cycle, are widely used. As shown in Fig. 13.4.1, since the 2P-SRAM is placed in front of large scale logic circuitry for image processing, a faster access time (e.g., <1ns) is required. In general, the read-out operation in 2P-SRAM utilizes full-swing of the single read bitline (BL), so a drastic improvement of the access time is not expected. On the other hand, the dual-port SRAM (DP-SRAM) makes use of the voltage difference between BL pair in the read-out operation, which is suitable for the high-speed operation. In this study, we present a time-sharing scheme using a DP-SRAM cell to achieve high-speed access in 2P-SRAM macros in such image processors.

There are several conventional methods to realize 2P-SRAM operation within a single clock cycle. A single-port SRAM (SP-SRAM) can be double-clocked with consecutive read and write operations, but such 2× operating frequency is generally hard to achieve. Alternatively, the read and write ports of a DP-SRAM can be operated in parallel; however, this causes a read-disturb issue [2] (Fig. 13.4.2), in which the cell current (I_{read}) is degraded when the read and write ports access the same row simultaneously. To achieve <1ns access time, such I_{read} degradation is not acceptable. Our method, using a DP-SRAM cell, performs consecutive read and write operations in a single clock cycle with a small delay between the WL pulses. The two operations effectively share time in the overall clock cycle as the rising edge of WLW is delayed until the sense amplifier (SA) has completed the read operation. Our method realizes i) high-frequency operation (or reduced cycle time) compared with conv. 1 (of Fig. 13.4.1) since the read and write operations are independently executed by independent peripheral circuits for each port, and (ii) high-speed access time due to prevention of read-disturb issue in conv. 2.

Figure 13.4.2 illustrates a situation in which data is read out from the left memory cell while a data is written to the right cell. Note that both cells are in the same row. Focusing on the left cell, since the read wordline (WLRn) is activated, the internal node MT discharges BLR (I_{read}). On the other hand, the write wordline (WLWn) is also activated to write a data to the right cell, so WLWn behaves as the dummy read operation for the left cell. The MT in the left cell (storing "0") is ramped up via the precharged BLW, reducing the power of MT to discharge the BLR. Thus, the cell current (I_{read}) decreases, which is referred to as the read-disturb issue. Figure 13.4.2 shows the simulated I_{read} with and without the read-disturb issue. To take the 6σ variation into account, we introduce the worst combination of the local V_{th} variation referring to the worst-vector method in [3]. Due to the read-disturb issue, I_{read} is decreased by 48%, which means that it takes twice as long to achieve the same amount of BL swing without the read disturb. Therefore, by circumventing the read-disturb issue, we can accelerate the time for BL swing by 50% compared with conventional DP-SRAM.

Another merit of our implementation is shown in Fig. 13.4.3, in which the left cell is written and read simultaneously. The unselected right cell in the same row is half-selected due to activation of both WLRn and WLWn and thus sees a strong dummy read operation. In this case, MT is raised significantly above ground by BLR and BLW. If MT becomes higher than the threshold voltage of the inverter in the cell, the storage nodes are flipped, causing data destruction. Figure 13.4.3 compares the waveforms of the WLs and the storage nodes for proposed and conventional circuit. In the conventional method, the longer the simultaneous-WL-activation period (indicated by the dashed arrow) becomes, the more easily the storage nodes are flipped, indicating low cell stability. This period for the time-sharing method is shorter than that used in conventional parallel read/write DP-SRAM because the write WL is activated only when the read BL swing is complete. Thus, this implemenatation realizes the high cell stability. In this study, we applied the conventional 8T DP-SRAM cell layout to our circuit, however the proposed circuit enables us to use smaller cell size owing to this advantage.

Figure 13.4.4 shows the circuitry and corresponding waveforms of our implementation. When the TDEC signal generated by CLK is activated, one read wordline, WLRn, is selected to begin the read operation. Note that in the conventional design, this TDEC also activates the WLWn, which results in the read disturb issue mentioned earlier. To circumvent this, we introduce a new BACK signal, which is activated by TDEC with a delay element This delay is designed so that the SA can detect the worst BL swing including the local V_{th} variation. The BACK signal activates the SA and the read-out data is transferred as the output Q. At the same time, the BACK signal also selects the WLWn so that the write operation is executed after the read-out is completed. In this way, the time-sharing scheme is achieved and the read-disturb issue is prevented. Note that WTE, which activates the write-driver (WD), is synchronized with TDEC, however, the data to be written is transferred to the WD in advance, so the peak current due to concurrent activation of SA and WD is effectively avoided. Simulated waveforms show that WLW1 activation is delayed until SAE is enabled, so that the read BLs (BLR0 and /BLR0) are discharged without disturbance from WLW1. In addition, WTE is enabled prior to SAE activation, which helps to reduce peak current as previously mentioned. Simulation results show that the cycle time and access time are 1GHz and 360ps, respectively.

The table in Fig. 13.4.5 summarizes the features of the circuit as designed in a test-chip in a 28nm high-k metal-gate process. The graph represents a Shmoo plot at 25°C, showing the relationship between minimum operating voltage (V_{min}) and read access time. The lowest V_{min} is 0.56V, while the access time at 1.0V is 500ps. This access time achieves 5× speed-up in comparison with our previous data (2.5 ns at 1.0 V using the same DP-SRAM in 28 nm process [4].) Figure 13.4.6 compares the data for this scheme with that for the conventional method (conv. 2 in Fig. 13.4.1.) The simulation result (solid line) is in good accordance with the measurement data for a wide range of supply voltage V_{DD}. A 100mV reduction in V_{min} is observed due to improvement of cell stability while the access time at worst-case temperature was improved by 13% to 360ps at 1.2V due to elimination of the read-disturb issue.

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References:
[1] T. Suzuki, H. Yamauchi, Y. Yamagami, K. Satomi, and H. Akamatsu, "A stable 2-port SRAM cell design against simultaneously read/write-disturbed accesses," *IEEE J. Solid-State Circuits*, pp. 2109-2119, Sep. 2008.
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[4] Y. Ishii, H. Fujiwara, K. Nii, H. Chigasaki, O. Kuromiya, T. Saiki, A. Miyanishi, and Y. Kihara, "A 28-nm dual-port SRAM macro with active bitline equalizing circuitry against write disturb issue," *Symp. VLSI Circuits Dig. Tech. Papers*, 2010, pp. 99–100.

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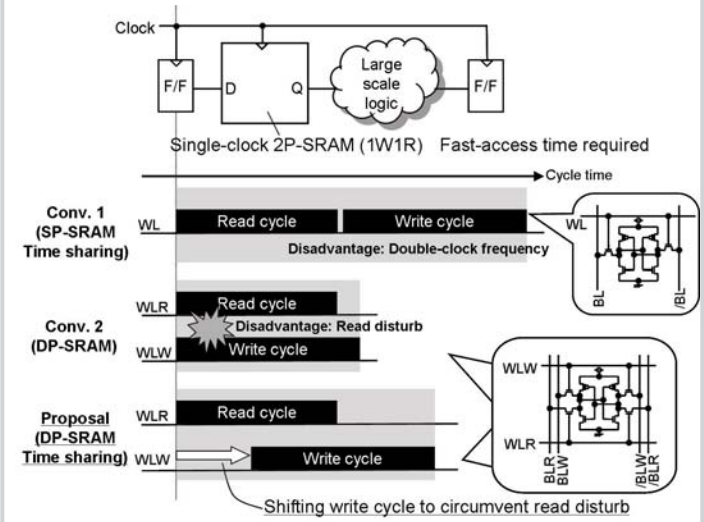


Figure 13.4.1: 2P-SRAM for image processing unit.

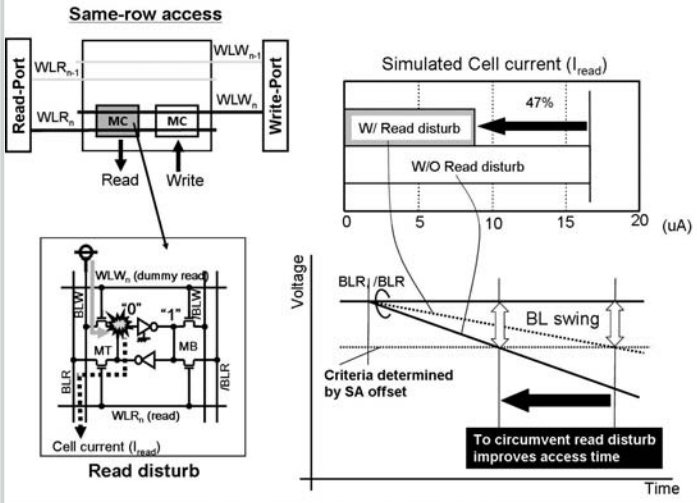


Figure 13.4.2: Advantage: Fast read access time.

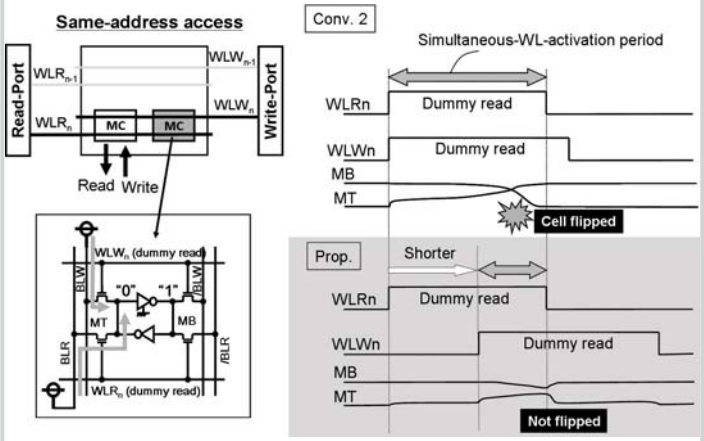


Figure 13.4.3: Advantage: Cell stability improved.

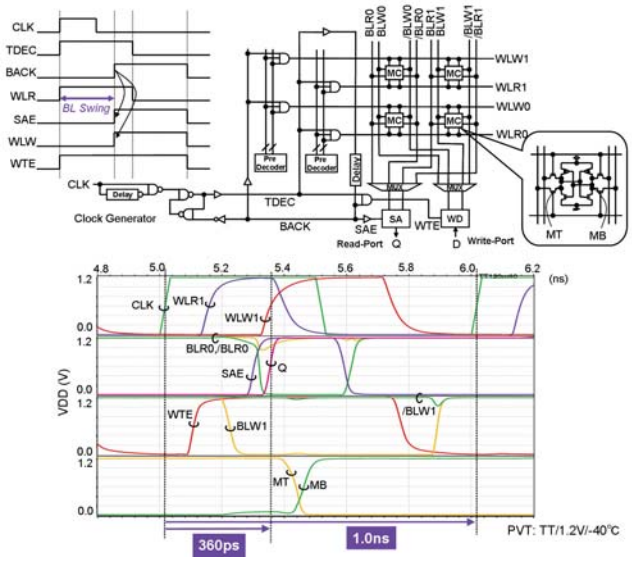
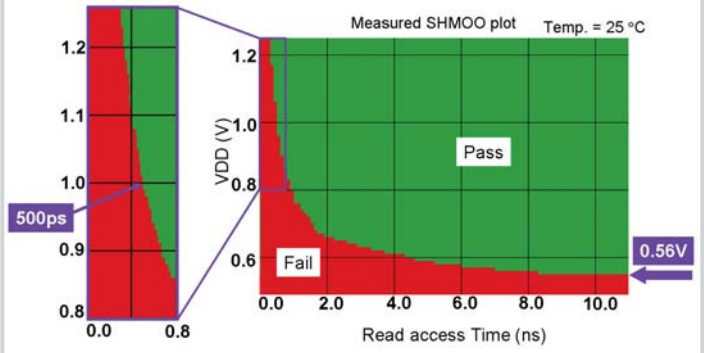


Figure 13.4.4: Circuit and simulated waveforms.



	Features
Technology	28-nm HK/MG Low-power CMOS process
Macro configuration	8-kb (128 words x 64 bits/word)
Macro size	4982 μm^2
Total capacity	128-kb (8-kb x 16)
Bit density	1.57-Mb/mm^2

Figure 13.4.5: Measured Shmoo plot and features of the test-chip.

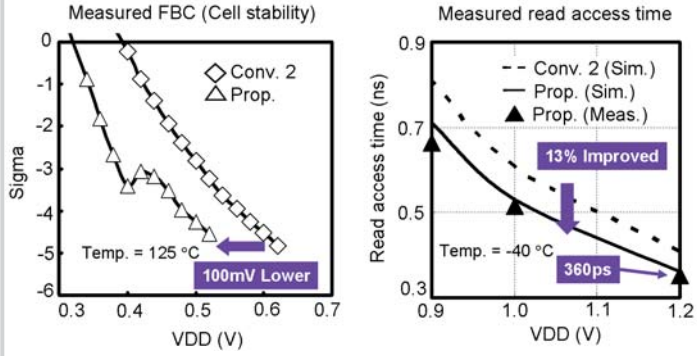


Figure 13.4.6: Measured FBC and read access time.

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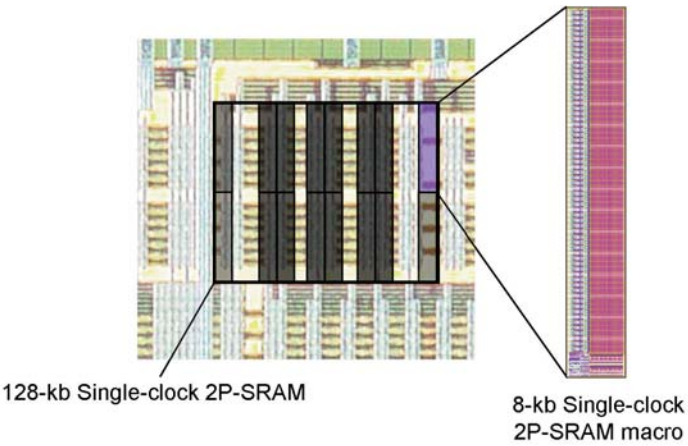

Figure 13.4.7: Microphotograph of the test chip.

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