Gain-Cell Embedded DRAM Under Cryogenic Operation—A First Study

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***Abstract*— Operating circuits under cryogenic conditions is effective for a large spectrum of applications. However, the refrigeration requirement for the cooling of cryogenic systems introduces serious issues in terms of power dissipation. Gain-cell embedded dynamic random access memory (GC-eDRAM) is a low-area, logic-compatible embedded memory alternative to static random access memory (SRAM), which has the potential to provide ultralow-power operation under cryogenic conditions due to the lower leakages at these temperatures. In this article, we present the first comparative design exploration of GC-eDRAM under cryogenic conditions performed with transistor models characterized based on actual silicon measurements under temperatures as low as 77 K. Our study shows that the two-transistor (2T)-based GC-eDRAM configurations turn out to be the best solutions for very low-temperature operation. In particular, the 2T mixed GC-eDRAM configurations allow read sensing margin improvements (up to 99%) within the 2T-based configurations while at the same time excel in terms of data retention time (+44%) and power consumption (−27%) when compared to more complex GC-eDRAM topologies. Moreover, even better improvements in terms of area (−73%), leakage power (−97%), retention power (−76%), and energy (−66%) are observed when compared to conventional 6T-SRAM.**

***Index Terms*— Cryogenic, data retention time (DRT), edge-direct tunneling, embedded memory, gain-cell embedded DRAM (GC-eDRAM), subthreshold leakage.**

I. Introduction

CRYOGENIC semiconductor (Cryo-Semi) electronics has been making its way into the aerospace/defense, cloud, scientific, and medical markets in different domain areas, including digital logic, sensors, mixed-signal circuits, and memories [1]–[3]. In particular, memories operating at cryo-temperatures exhibit improvements in terms of speed and energy [4]–[7]. Despite the favorable features of Cryo-Semi electronics, the need of a refrigeration system to cool down to extremely low-temperature levels incurs power consumption restrictions [7]. This further raises the importance of increasing the capacity of the on-die memory, which provides several orders of magnitude better power consumption and performance compared to off-chip solutions, such as dynamic random access memory (DRAM) [8]–[10]. Moreover, recent cryogenic computing studies [9]–[11] have been raised as a potential alternative to deal with the performance limitations in classical room-temperature computing while dramatically reducing the standby power of classical room-temperature computing. In the above context, gain-cell embedded DRAM (GC-eDRAM) represents a promising alternative to six-transistor static random access memory (6T-SRAM), due to its reduced area, which enables more on-die memory integration. Furthermore, the main limitation of GC-eDRAM reduced data retention time (DRT) is mitigated at low temperatures, due to the leakage current lowering. This potentially leads to significant power savings for GC-eDRAM at cryogenic temperatures, as the longer retention reduces the need for too frequent energy-wasting refresh operations.

This article presents a first fine-grained study of GC-eDRAM under cryogenic temperature conditions. While a very recent work has considered using GC-eDRAM for cryogenic operation [9], this was done at a high level based on an architectural memory modeling tool [8]. Differently, our analysis was carried out at the transistor level, utilizing a 65-nm CMOS technology that was characterized for cryogenic temperatures based on silicon measurements at temperatures ranging from room temperature (300 K) down to liquid nitrogen temperature (77 K). Note that several applications, and most specifically, quantum computer control circuits, target even lower temperatures of liquid helium (4 K) [12]. However, due to the very challenging cooling requirements, the power budgets of operating at such low temperatures are extremely limited [13]. Therefore, in this work, we have focused on the liquid nitrogen operating point, which is commonly used in applications such as infrared image sensors [14] and has been recently suggested as an attractive operating point for high-performance computing [9], [15].

As a main result of this work, we have shown the outstanding suitability of gain-cell (GC) topologies to design cryogenic memory systems. More precisely, our study finds

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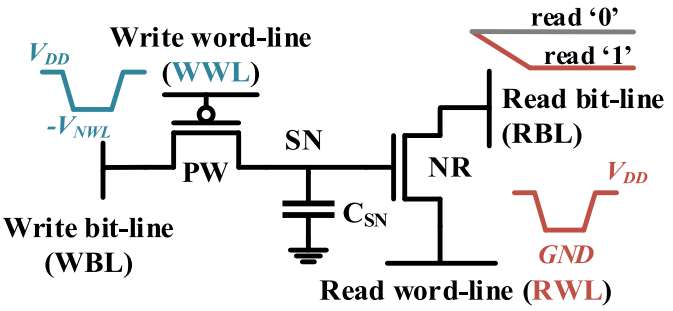


Fig. 1. 2T Mixed pMOS–nMOS GC-eDRAM bitcell with the respective control signals.

that the two-transistor (2T) GC topology is an advantageous candidate for cryogenic operation compared to 6T-SRAM and to more complex GC topologies. This is accomplished while considerably increasing DRT capability and reduced area occupation.

The rest of this article is organized as follows. Section II provides a brief review of GC-eDRAM technology, while Section III describes the MOS operating characteristics at cryogenic temperatures. Accordingly, Section IV presents best-practice design of 2T gain cells (GCs) under cryogenic conditions. This is followed by a comparison of 2T GC configurations against more complex topologies in Section V. Finally, Section VI summarizes the main conclusions of this work.

II. Background

GC-eDRAM is a fully logic-compatible embedded memory technology, which is implemented by two–four transistors, as opposed to the six transistors required for the ubiquitous single-ported static random access memory (SRAM) bitcell [16]. Over the past years, a large assortment of GC topologies have been proposed to provide different tradeoffs between area, power, and write/read performance [17]–[22]. All of these designs employ decoupled read and write ports, which provide inherent two-ported functionality and store their state as charge upon a parasitic capacitance.

Fig. 1 shows the 2T mixed pMOS–nMOS GC-eDRAM bitcell, which consists of a pMOS (PW) and an nMOS (NR) representing the write and read access ports, respectively. The writing operation is performed by turning on PW. As the write wordline (WWL) is asserted with a negative underdrive voltage (i.e., WWL $= -V_{\mathrm{NWL}}$), the data charged in the write bitline (i.e., WBL $=$ "0" or "1") is transferred to the storage node capacitance (C_{SN}), which primarily consists of the gate capacitance of NR and the junction capacitance of PW [22]. The read bitline (RBL) must be precharged (i.e., RBL $= V_{\mathrm{DD}}$) to start a read operation. When the read wordline (RWL) is enabled (RWL $= 0$ V), if the storage node (SN) is holding a "0", the RBL will remain at V_{DD}, while if a "1" is stored (i.e., SN $= V_{\mathrm{DD}}$), the RBL will be discharged down to ground. Thereafter, the RBL is compared to a reference voltage by a sense amplifier to produce the output data.

Since the memory state is stored as dynamic charge, which can leak away over time, GC-eDRAM suffers from limited DRT, and therefore, the data must periodically be refreshed. In order to reduce the refresh frequency, many of previous works [17]–[22] focus on the reduction of subthreshold conduction I_{SUBTH}, which at room temperature is the dominant leakage contribution affecting the GC data integrity. This has led to optimization efforts to reduce the leakage through the write port while improving the ON-current of the read port, which often limits the operating frequency. In this regard, the 2T mixed pMOS–nMOS topology of Fig. 1 was found to be a good candidate for low-power operation, as the pMOS write transistor offered low I_{SUBTH}, while the nMOS read transistor offered higher ON-current than its pMOS counterpart [22]. However, with the reduced subthreshold currents at cryogenic temperatures, the assumptions that led to these conclusions are invalid, leading to the need to reanalyze the GC design.

III. MOS Operation at Cryogenic Temperatures

Standard operating conditions for MOS technologies are typically considered from hot operation at 85 °C or 125 °C, down to cold operation at 0 °C or −40 °C. Accordingly, foundry-supplied process design kits (PDKs) generally provide silicon-calibrated and validated models for transistor simulation over this range [8]. Therefore, simulations performed outside the above temperature range lose accuracy and cannot be relied on for fine-grained design optimization tasks. The loss of accuracy is exacerbated below 200 K, where many of the effects of cryogenic temperature start to have a major impact [8], [23], [24].

For the purpose of this study, a 65-nm CMOS BSIM4.7-based transistor model, calibrated for cryogenic operation down to 77 K, was used. The model calibration was performed based on a fabricated test chip, cooled in a liquid nitrogen chamber, and measured to obtain transistor characteristics. The calibration procedure was done for typical–typical (TT), slow–slow (SS), and fast–fast (FF) corners in order to obtain accurate process deviations results. Likewise, the model considers a correct calibration of the parasitics (i.e., capacitance and resistances) for accurate post-layout simulations. Fig. 2 compares the foundry PDK model and the model used in this work of an nMOS device for $T = 300$ K and $T = 80$ K, respectively. While the simulation results are almost overlapped for $T = 300$ K, the adopted model predicts the experimental measures much more accurately at $T = 80$ K.

By reducing the temperature, important device physical properties are influenced: the threshold voltage increases, charge carrier mobility grows, and the saturation velocity is increased, mainly due to the reduction of scattering mechanism [25], [26]. Moreover, the cryogenic regime can assure further improvements in circuit performance by reducing both the power consumption and leakage current [25]. Therefore, cryogenic temperatures play a key role in the design of GC read and write ports.

In 90-nm nodes and below, leakage currents impact the data integrity of GCs [21]. To gain an insight on this, Fig. 3 shows the cross-section of an nMOS transistor by highlighting its leakage currents: the subthreshold conduction (I_{SUBTH}), the p-n-junction leakages (I_{diff}), gate-induced drain leakage (I_{GIDL}), and the gate tunnel current (I_{gate}), which includes edge-direct tunneling (I_{EDT}) [22]. Note that leakage

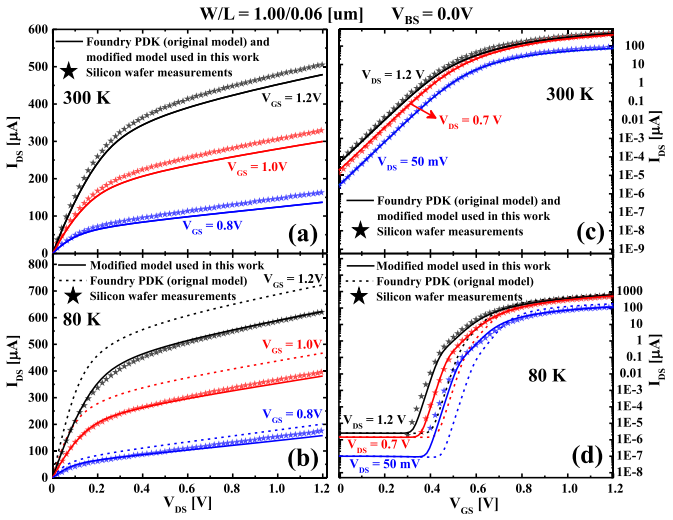


Fig. 2. (a) and (b) I_{DS} versus V_{DS} for different values of V_{GS} and (c) and (d) I_{DS} versus V_{GS} for different values of V_{DS} as extracted by the foundry model (original model), the modified modeling used in this work, and the silicon wafer experimental measures for $T = 300$ K and $T = 80$ K, respectively. An average error below 2% and less than 10% between the used model and the experimental data is observed at $T = 80$ K for I_{DS} versus V_{DS} with V_{GS} 1.2 V and I_{DS} versus V_{GS} with V_{DS} 1.2 V, respectively.

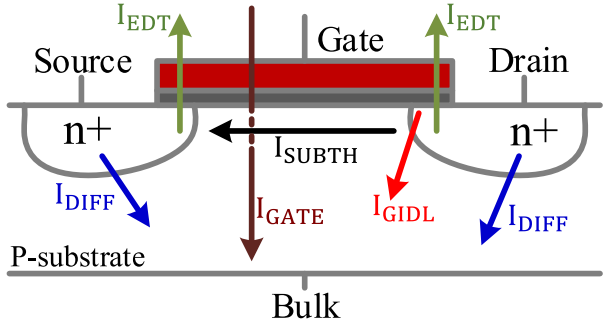


Fig. 3. Leakage components of the nMOS transistor.

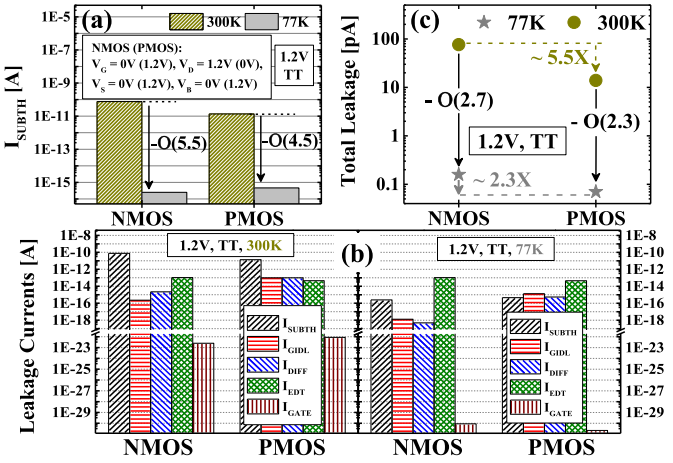


Fig. 4. (a) I_{SUBTH}, (b) leakage components that affect the SN, and (c) total leakage contribution of minimum size nMOS and pMOS transistors in 65-nm node at 300 K and 77 K.

components that have no impact on the SN have been omitted from the figure.

Fig. 4(a)–(c) shows the simulation results of leakage currents for minimum size nMOS and pMOS devices that in turn consider the influence of the SN bitcell in standby

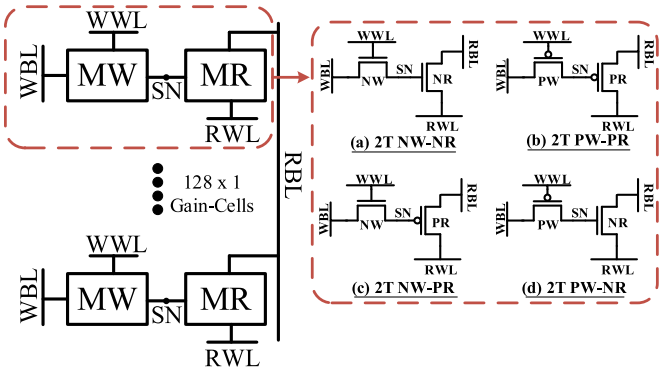


Fig. 5. 2T GC-eDRAM based on four GC topologies: (a) 2T NW-NR, (b) 2T PW-PR, (c) 2T NW-PR, and (d) 2T PW-NR.

mode. The plotted data are obtained at the nominal supply voltage (i.e., $V_{DD} = 1.2$ V) for both room temperature ($T = 300$ K) and cryogenic operation ($T = 77$ K). Compared with room temperature, cryogenic operation leads to a reduction of I_{SUBTH} by about 5.5 and 4.5 orders of magnitude for nMOS and pMOS transistors, respectively [see Fig. 4(a)]. Moreover, the magnitude of all the leakage components decreases at $T = 77$ K [Fig. 4(b)]. As expected, I_{SUBTH}, which was dominant at room temperature, is no longer the highest leakage factor under cryogenic conditions. Interestingly, the major leakage contributor affecting the SN under cryogenic operation turns out to be the I_{EDT}, as the gate-to-diffusion voltage difference is high under many bias conditions.

In summary, Fig. 4(c) shows that decreasing the temperature from 300 K down to 77 K allows the total leakage current to be reduced by about 2.7 and 2.3 orders of magnitude for nMOS and pMOS transistors, respectively. Furthermore, the difference in total leakage between nMOS and pMOS devices scales by a factor of 5.5× for $T = 300$ K to a factor 2.3× when $T = 77$ K. Hence, considering the results obtained from the above simulation study and the fact that I_{SUBTH} is no longer the dominant leakage component at 77 K, GCs can be properly redesigned to optimize DRT when working at cryogenic temperatures.

IV. Design of GC-eDRAM at Cryogenic Temperatures

Our design exploration at 77 K relies on the GC-eDRAM column shown in Fig. 5. To identify the best configuration of a 2T GC, we considered four bitcell options, each one composed of a write transistor (MW) and a read transistor (MR): the nMOS- and pMOS-only configurations of Fig. 5(a) and (b), and the mixed 2T NW-PR consisting of nMOS (NW) as port and pMOS (PR) as read port, and PW-NR configurations of Fig. 5(c) and (d), respectively. Note that for all the results presented in the remaining text, the array was evaluated in the worst case condition, where the WBL holds an opposite voltage level with respect to the SN, i.e., WBL = V_{DD} (GND) when SN = "0" ("1").

In its early stage, our exploration was aimed at the static analysis of the GC-eDRAM bitcells. Since the pMOS transistor was found to be less leaky than its nMOS counterpart, it is potentially a good candidate for the 2T GC-eDRAM bitcell implementation, in which the SN is strongly affected

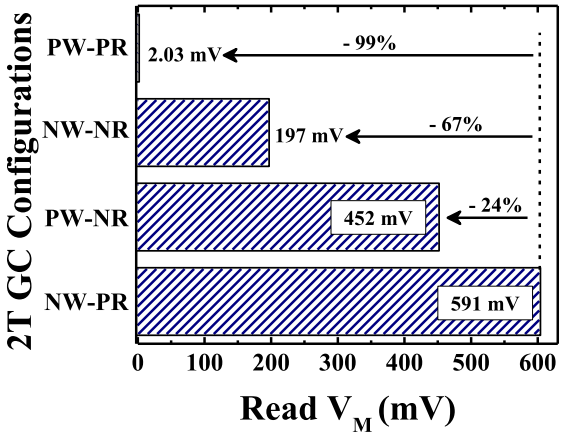


Fig. 6. 2T GC-eDRAM configurations versus read voltage margin (V_M).

by leakage. However, since I_{EDT} is the dominant leakage component, further exploration is necessary in terms of read/write port alternatives. Taking into consideration the write port of the GC bitcell, pMOS and nMOS devices write a weak "0" and "1", respectively. In order to overcome these limitations (i.e., the weak written values), boosted voltages (i.e., $-V_{NWL}$ for pMOS and V_{BOOST} for nMOS) are commonly applied to strengthen the weaker stored voltages. However, the use of boosted voltages incurs increased power consumption and system complexity. On the other hand, by looking into the read port, the most important metric is its read sensing capability that is directly linked to the read voltage margin (V_M), defined as the difference between the RBL voltage "1" and "0" (i.e., $V_M = V_{RBL("1")} - V_{RBL("0")}$).

A comparative evaluation in terms of V_M for the four possible 2T GC-eDRAM bitcell configurations is shown in Fig. 6. Here, V_M was evaluated for a read pulse of 1 ns applied 4 μs after writing into the SN under nominal simulation conditions and without any boosted voltage. From Fig. 6, the GC topology that assures the best read sensing margin is the 2T NW-PR. Compared to its counterparts, the 2T NW-PR-based GC-eDRAM cell allows V_M to be considerably increased (in the 24%–99% range). The above V_M analysis rules out the possibility of using pMOS- and nMOS-only configurations.

We extended our analysis on the 2T NW-PR-based GC-eDRAM cell to evaluate its voltage margins and data retention capabilities through Monte Carlo (MC) simulations for different corners (i.e., SS, TT, and FF). Fig. 7(a) shows the statistical distribution of V_{RBL} for both "1" (i.e., $V_{RBL("1")}$) and "0" (i.e., $V_{RBL("0")}$) states for $T = 77$ K.[1] The SS corner presents the larger variability (i.e., higher σ/μ). From the TT distributions, V_M is evaluated at 3σ and 6σ ($V_{M(TT),\,3\sigma}$ and $V_{M(TT),\,6\sigma}$), which still provides considerably higher margins than those reported in Fig. 6. Moreover, Fig. 7(b) shows the statistical distribution for the read V_M at $T = 77$ K, where for the sake of comparison, the room-temperature results were also considered. Here, we can observe that the array operating under cryogenic conditions achieves significant sensing margin

[1]Note that, as before, V_M is observed 4 μs after writing into the SN.

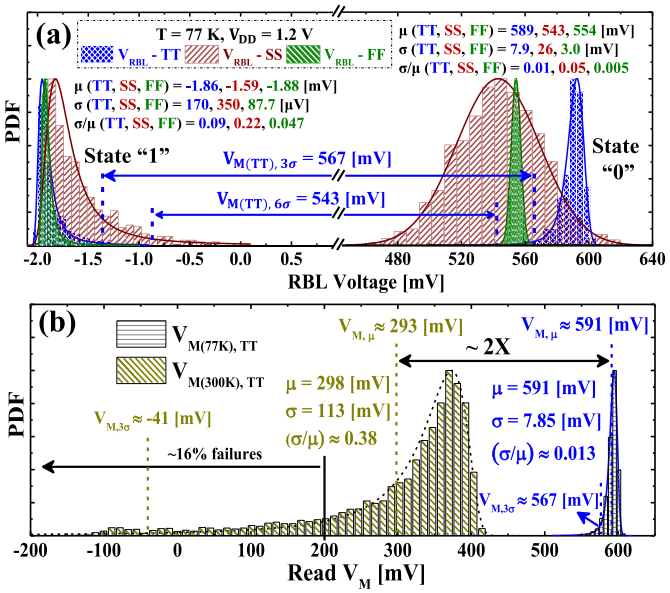


Fig. 7. (a) RBL voltage (V_{RBL}) statistical distributions for "1" ($V_{RBL("1")}$) and "0" ($V_{RBL("0")}$) states and different corners (TT, SS, and FF). (b) Read voltage margin (V_M) statistical distribution for 300 and 77 K for the TT corner.

(2×) and variability, i.e., σ/μ (29×), improvements with respect to room-temperature simulations due to the reduced leakage. Fig. 7(b) also shows that V_M at room temperature presents an increase of failures of about 16% if a minimum sensing margin of 200 mV is considered [22].

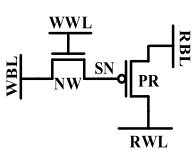
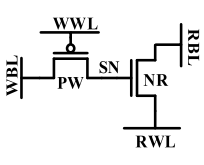
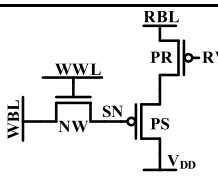
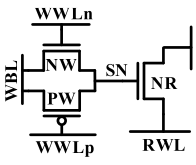
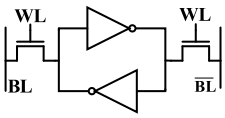
Regarding the data retention capabilities, the SN degradation and DRT are reported in Fig. 8(a) and (b), respectively, for TT, SS, and FF corners. From Fig. 8(a), the "1" and "0" decay is much slower at 77 K compared to room-temperature operating conditions [18], [22], due to the reduced leakage (see Fig. 4). This supports the prediction done in Section III, i.e., improvements in SN degradation and DRT capabilities. The simulations shown on Fig. 8(a) are used to calculate the DRT reported in Fig. 8(b), which is the time it takes for the difference between the SN voltages (i.e., "0" and "1" decay) to be 200 mV [22]. Here, for the sake of comparison, results at room temperature are also included. According to the reported results, 2T NW-PR GC-eDRAMs operating at cryogenic temperatures and different corners show improvements, on average, in terms of DRT (nominal value) and σ/μ by a factor of roughly 1070× and 51×, respectively, compared to room-temperature results. Moreover, when compared to the TT corner, the DRT of FF (SS) corner is reduced (increased) by a factor of 0.5× (2.2×).

V. Comparison Results and Best Practice of Cryogenic GC-eDRAM Design

The 2T GC topologies, analyzed in Sections II–IV, are the smallest of all GC options; however, previous publications have proposed larger cells (in terms of transistor count) to optimize various design specifications. In order to choose the best configuration for cryogenic operation, we have simulated the 2T bitcells, as well as the three-transistor (3T) [17] and 3T transmission gate (TG) GC [18] topologies. In addition,

TABLE I

FIGURES OF MERIT OF GC-eDRAM BASED ON DIFFERENT BITCELL TOPOLOGIES UNDER CRYOGENIC TEMPERATURES ($T = 77$ K) AND NOMINAL VOLTAGE ($V_{DD} = 1.2$ V) FOR A 128-WORD MEMORY AT TT CORNER

Parameter	2T Mixed GC NMOS-PMOS (2T NW-PR)	2T Mixed GC PMOS-NMOS (2T PW-NR)	3T GC	3T TG GC	6T-SRAM
					
Normalized Area	0.27X	0.27X	0.33X	0.43X	1X
$V_{M,4\,\mu s}$ [mV]	591	453	586.3	596.9	—
$V_{M,40\,ms}$ [mV]	250	8.26	1.717	31.59	—
DRT [ms]	23.3	19.9	12.14	19.17	Static
Read Energy/bit [fJ]	0.739	0.736	1.332	0.736	2.279
Write Energy/bit [fJ]	0.852	0.872	1.445	1.723	2.430
Refresh Energy/bit [fJ]	1.591	1.607	2.777	2.459	—
Leakage Power/bit [fW]	6.768	16.21	36.49	42.065	376.2
Static Retention Power/bit [pW]	0.080	0.102	0.164	0.201	0.376

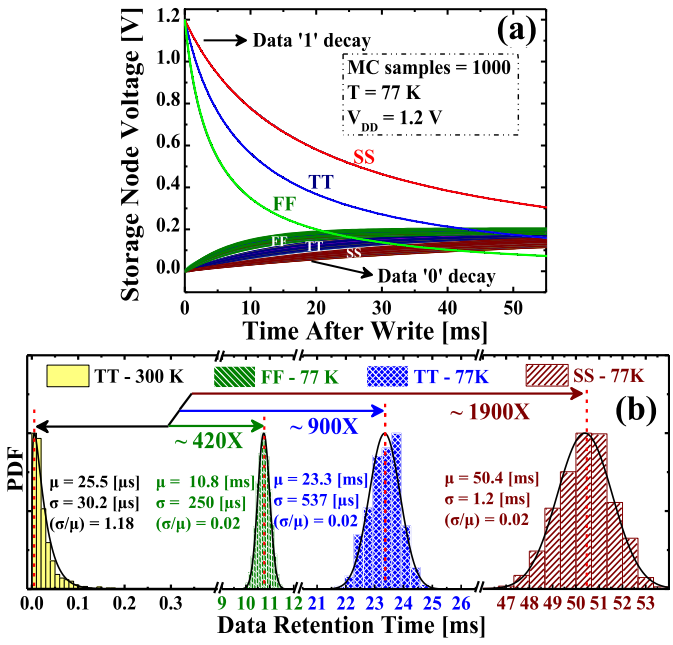


Fig. 8. (a) SN degradation at 77 K and nominal voltage. (b) DRT statistical distribution for 300 and 77 K.

we have compared our results to the state-of-the-art 6T-SRAM cell. Table I summarizes the simulation results for a 128-word memory, i.e., 128 × 1 array at 77 K under nominal V_{DD} in terms of sensing margins, DRT, and both power and energy consumption. Note the reported data consider a write/read pulse of 1 ns and post-layout capacitance parasitic extraction results for estimated per-bit power and energy calculations.

From Table I, the 2T mixed NW-PR configuration excels in every figure-of-merit while also providing a smaller area footprint. In particular, it is noteworthy that two read voltage margins were considered with a 1 ns read pulse: the first 4 μs after write and the second after 40 ms of standby (under worst case) operation. For the second metric (i.e., $V_{M,\ 40\,ms}$), only the 2T mixed NW-PR configuration provides a read sensing margin above 200 mV. Moreover, by looking into the data retention capabilities (i.e., the DRT), the 2T NW-PR achieves significant improvements of about +44%, on average, compared to the considered counterpart GC-eDRAM topologies. It is worth mentioning that, as shown in our previous leakage simulations (see Fig. 4) at 77 K, pMOS I_{SUBTH} (as well as I_{GIDL} and I_{diff}) is higher than nMOS, so lower data retention capabilities are observed when we use a pMOS device as MW. Furthermore, for the case of MR, leakage contributors affecting the SN are from the gate (I_{gate} and I_{EDT}), where nMOS I_{EDT} is higher [see Fig. 4(b)] than pMOS. Thus, when using an nMOS as MR, it will leak more.

Further advantages can be observed in terms of energy per operation and retention power. Overall, when compared to 3T GC-eDRAMs, 2T GC-eDRAMs exhibit refresh energy ($E_{refresh} = E_{read} + E_{write}$) and retention power ($P_{ret} = P_{leak} + P_{dyn}$) savings, on average, per bit, of −39% and −50%, respectively, mainly due to the smaller number of transistors and fewer leakage paths. It is also worth underlining that due to reduced variability at cryogenic temperatures (see Figs. 7 and 8), the read operation is more robust and higher read speed (e.g., 1 ns) can be achieved. This, in turn, reduces the dynamic power since V_{RBL} will discharge for a shorter time span. When compared to SRAM, in addition to the straightforward area reduction, the 2T GC-eDRAM also provides a low-power alternative, primarily due to the long DRT. The 6T-SRAM bitcell exhibits over 50× higher leakage than the 2T cell NW-PR cell such that the overall retention power of

GC solution is almost 80% lower than the static power of the SRAM. Equally important, it is worth noting that due to longer DRT at cryogenic temperatures, the refresh will not be needed for many applications, providing further power savings.

VI. Conclusion

In this work, the design of GC-eDRAM for cryogenic operation has been investigated. Our simulation analysis was performed in a standard CMOS 65-nm technology node, characterized for temperatures down to 77 K while considering mismatch and different corners. As a preliminary study, we analyzed the static characteristics of MOSFET devices by considering room and cryogenic temperatures. Results demonstrate that at very low temperatures, transistor devices exhibit a significant improvement in terms of leakage, where the subthreshold conduction is reduced by more than four orders of magnitude at 77 K, resulting in edge-direct tunneling becoming the dominant leakage contributor. Our study was then extended to the bitcell level for different 2T GC-eDRAM configurations. The obtained results show that at 77 K, the 2T mixed NW-PR-based GC-eDRAM proves to have better read sensing margins (+63%, on average), compared to its counterparts (i.e., 2T mixed PW-NR-based and 2T only pMOS- and nMOS-based GCs). Moreover, at cryogenic temperatures and different corners, 2T NW-PR-based GC-eDRAM provides better DRTs (+1070×, on average) while also assuring lower variability (−51×, on average) when compared to room-temperature results. Finally, our study was extended to also include 3T GC topologies and a 6T-SRAM in the comparison. Again, the 2T NW-PR-based GC-eDRAM is found to be superior in terms of read sensing margin (+60%, on average), DRT (+44%, on average), leakage power (−80%, on average), and retention power (−53%, on average). Overall comparative results demonstrate that due to the reduced operating temperature, the GC-eDRAMs, and especially the 2T mixed NW-PR GC-eDRAM, exhibit promising advantages in both power and DRT, proving that they are excellent candidates for low-power cryogenic memory applications. Future work includes the analysis of GC-eDRAM memory as part of a cryogenic operated imaging system and further analysis of the operation of dynamic memories down to liquid helium temperatures.

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